Sept, 1967

MEMO

To: A. L. Dean

From: J. H. Saltzer

Subj: EPS 156; GE 645 Model B System Clock, dated June 8, 1967

This EPS is very well written and involves a considerable improvement over the previous specifications for the system clock. Below are a variety of comments varying in importance from very significant to trivial. No particular order is given, although the following six points are perhaps particularly important:

1. The clock is capable of being driven by an external frequency source. For this source, specifications are not given.
2. As specified, there is no provision for power for the clock other than the usual system power.
3. The automatic testing strategy which is described does not appear to work under the conditions imposed by Multics.
4. There is some question as to whether the worst case delay in attempting to read the clock can cause a central processor to receive an operation-not-complete condition.
5. As proposed, a system with two clocks has some single electrical components shared between the clocks. Failure of a single component can thus down a fully duplexed system.
6. The system clock is providing one more (possibly unwanted) path by which the system may discover system power down.

These points will be covered in more detail in the extensive comments below. The remaining comments are presented in order of their appearance in the document.

In Section 1.11, on accuracy and resolution, the precision of the clock is not adequately specified. Two specifications should appear here. The first of these is what is the maximum long-term rate of departure from real time? (At adjustments

obtainable in the field.) Second, what is the maximum short-term drift from the average rate? The specification as given for long-term drift of no more than plus or minus 10 counts per million only approximates one of these two specifications. Also the specification on page 4 of plus or minus 10 counts per million conflicts with that on page 9 of plus or minus five counts per million.

In Section 2.1, in the last paragraph on sheet 7, a reference is made to the "I switch" with no definition or comment, and this switch is not referenced in the glossary.

In the last paragraph of Section 2.1, the third sentence should probably begin with "following" instead of "for". This section does not specify what happens if the alarm clock is set following a trouble interrupt. Reading between the lines, one would guess that the calendar clock has stopped counting and therefore, no interrupt could occur following the setting of the alarm clock. However, this possibility is not spelled out in the document.

In Section 2.4, it is mentioned that an external source may be used to drive the clock. No specification is given of the necessary source wave form, such as pulse height and width, etc. In this paragraph is found the contradictory statement that maximum drift is plus or minus 5 counts per million. In the fourth paragraph of 2.4, the sentence beginning "the strategy of the clock" does not make any sense unless both commas are removed.

In Section 2.6, a low bit counter failure fault is described in which counters are compared every 64 microseconds. It is not mentioned how the 64 microseconds are measured. If the interval is measured by reversal of the sixth bit of the calendar clock, failure of the calendar clock will not be detected. In the third paragraph

of 2.6, reference is made to the clock as a monitor of the system AC power supply. This particular reference comes as a surprise and perhaps should be mentioned in the specifications for GE 645 system itself. The problem of detecting system power down should be viewed as a system consideration, and care must be taken that not too many different uncoordinated detection paths exist. (E.g., processor power down fault, GIOC SCO, Drum trouble, and Clock trouble.)

In this discussion of the automatic test sequence, there is a comment made that the automatic test sequence is not done if the comparator is armed. Is the automatic test signal remembered and performed when the comparator becomes disarmed? This point is important because when Multics is operating normally, the alarm clock will be armed at all times except for brief instants following interrupts and before the time the alarm clock can be rearmed.

In Section 2.7.2, a common display panel for two clocks is described. No comment is made of what happens if display panel failure occurs. Are both clocks down? No engineering drawing of this display panel was included in my copy of the specifications. The design of the clock system in this area seems to be based on the assumption that all systems will use either one or two clocks. This is a potential problem for a customer interested in extreme reliability obtained by Triplexed equipment. In fact, in light of the rest of the design of the 645 system, it would seem completely inappropriate for two system clocks to share <u>any</u> electrical components. (I.e., if one Nixie tube burns out, is the whole system down?) At most, two clocks may happen to share a cabinet, but even that should not be required.

In Section 3.2, a consequence of the organization of auxilary storage and clock is that if the upper clock is down, the auxilary store is inaccessible to the system. This consequence is not spelled out in the specifications. At the end of the 3.5 section, it is carefully pointed out that only one wakeup interrupt can occur with-

out reloading the alarm clock. It is not stated whether or not several fault interrupts can occur in a row.

In Section 3.7, on programming considerations, the comment is made near the bottom of sheet 21 that the alarm clock can be set only in Master Mode. It is presumably also true that it can be set in absolute mode.

In Section 3.8.6, part 3, a method of setting the clock is described in which the 28 most significant bits of clock B are set in the octal panel switches. Please note that this requires setting 9 1/3 of the octal switches.

In Section 4.2 on clock commands, it is stated that the processor will make a check to insure that the LACL instruction is only executed in master mode and that the system controller will not check. This is not in parallel with other Memory Commands in which if the processor check fails, the system controller will reply with illegal action. It is not clear why this extra protection is not provided for the LACL. In the description of interface logic in Section 4.3.2, it is commented that core access in the auxilary store will be delayed by the clock/core switch. Reference is made to additional delay in the system controller. Where is the total delay specified, or is it known? In the same vein, back in Section 3.7, under programming considerations, the statement is made that the system clock is inaccessible for periods as long as three microseconds. This delay apparently does not include system controller cycle time. What is the maximum possible delay to the processor if system controller time is included?

Section 5 makes a reference to auxilary power. This is the only reference to auxilary power mentioned. It is not clear from this reference whether the originally stated objective that the system clock be powered from a source independent of the motor generator can be obtained. The prototype clock had a power supply strategy

which selected the better of either the local utility power or system MG set power. This allows the clock to continue running during periods of system shut-down, say for vacation, and also through momentary power failure. The comment about ground loops implies that grounding may be the reason for reluctance to use utility power. If that is the only problem, there should be some way of sorting it out, perhaps with an isolation transformer, because the objective of independent power to the clock, to allow system shut down, is considered quite important.

In Section 6.2.2, a note is in order only for future reference, since it would be difficult to change the design now. It would be very useful if the restriction of the LACL instruction to master mode only could be turned on and off by program in combination with the system clock test-enable switch, so that a system clock undergoing test and diagnostic could be turned over to a T and D program which is written entirely in slave mode. In the section on maintenance items under the automatic test description, it is not mentioned that automatic testing is disabled if the comparator is armed. In Appendix A, under the description of "special access", the comment is made that when special access occurs, the clock loads the calendar clock. This statement is only true when the test-enable switch is <u>on</u>.

The description of the clock automatic test sequence brings to mind the following question: Suppose the following worst case condition with 8 active devices occurs: The lowest priority CPU requests a clock cycle and finds that it must wait in line behind all seven of the other active devices. When the CPU does obtain its cycle, it is forced into a three microsecond delay because an automatic test sequence has just begun. During this delay, it is possible for all 7 other active devices to request usage of the system controller. Is the worst case concentration of these considerations capable of forcing operation-not-complete in the lowest priority CPU?

In the glossary, the description of "upper clock" contains the comment that only the upper clock detects power failure faults. The question immediately arises, what if the lower clock is in use and for some reason its power fails?

Under the description of "XIC", it is implied that execute interrupt cells may only be set by program or system clock. Of course, any active module may set an interrupt cell.

This completes the detailed comment on this specification. The specification is written much better than previous versions. In fact, it is quite well done. I have made in the margin of my own copy a few suggestions and comments on matters such as English, order of presentation, and similar points. You are welcome to borrow my copy if you feel these comments may be of value in improving the specification.

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