BB.1

Glossary

Glossary:

Process Concealed stack:

A stack, stored in the process data segment (q.v.) which is used to store the processor state on internal interrupts and faults; and to perform calls while handling internal interrupts and faults.

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Glossary

External Interrupt:

An interrupt which comes from an I/O device or other equipment attached to the system. (c/w Internal interrupt)

Internal Interrupt:

An interrupt triggered by the ~~operating system directly~~ traffic controller and directed at the process running on the interrupted processor.

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Glossary

Processor Stack:

A stack, stored in the processor data segment (q.v.) used to store the processor state on external interrupts, and to perform calls while handling internal interrupts.

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Glossary

Traffic Control:

A Term used to describe the operations of processor interrupt and fault management, scheduling, and dispatching.

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Glossary

Meter

A Term used to describe a core storage cell which is used to accumulate resource usage measurements.

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Glossary:

Inhibit:

A mode of processor operation in which interrupts (and some faults) are not ~~recognized~~ accepted; they are instead remembered until the processor leaves the inhibit mode.

Mask:

To place a temporary inhibition on selected interrupt sources. create a condition such that certain interrupts will be inhibited when they occur.

(See Inhibit.)

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Glossary:

Interrupt:

The response of a processor to an arbitrarily timed external signal. (cf. ~~cf.~~ fault)

Fault:

The response of a processor to a condition arising within the processor as a result of program execution. (c/w ~~fault~~ Interrupt)

(Note: On the GE-645 processor, certain interrupt conditions (connect and power down) are implemented using fault hardware; the processor manual describes these as faults.)

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Standards + Glossary

System Initialization:

Execution of a sequence of programs which load and initialize a complete running version of Multics, starting with a clear core memory. A system initialization may or may not include a secondary storage reload.

System Restart:

Execution of a sequence of programs which re-initialize a complete running version of Multics, starting with a loaded core memory. System restart may include an effort to salvage whatever information possible from the data bases stored in core memory. System restart may be an appropriate action, for example, following a transient hardware fault which causes the system to "hang up".

Standards Section

Processor Identification Number:

An 18-bit string which uniquely identifies the processor. It is composed of an 6-bit type code and a 12-bit serial number concatenated in that order. A 645 processor has type code 001. Other processors will be assigned type codes as necessary.

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Glossary

Processor Hardware tag:

A wired-in register which identifies the processor. Ideally, it contains the Processor Identification Number. On a 645 processor the Processor Hardware tag is a 3-bit register. ~~which~~

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Standards Section

Calendar Time:

A signed 64 bit (double-word) integer giving the number of microseconds since 0000 GMT, Jan. 1, 1901.

Calendar clock:

A centrally located hardware register which contains the current Calendar Time. It is incremented once per microsecond.

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Standards Section

Unique Binary Identifier:

A 70-bit string which, by virtue of its method of ~~creation~~ construction, is guaranteed to be different from every other 70-bit string so ~~created~~ constructed. It is composed of ~~the least~~ the 52 least significant bits of the current calendar time concatenated with the 18 bits of the current processor ~~number~~ identification number.

Standards Section

Unique ASCII Identifier:

An 11-character string which, by virtue of its method of construction, is guaranteed to be different from every other 11-character string so constructed. It is constructed by converting a unique binary identifier (q.v.) to an integer in the base 84. The 84 possible values of each digit will be represented by the 94 ASCII graphics, less the upper and lower case vowels A, E, I, O, and U, in their standard collating sequence (leaving out the vowels guarantees that no random obscenities will be generated.)

Remainder mod 84	ASCII graphic
0	!
1	"
2	#
etc.	

Glossary

Execution Meter:

A meter which counts the number of memory cycles used by a processor. A 24-bit hardware execution meter in each 6/45 processor measures the number of cycles used by the processor for all operations. This hardware timer is used by the supervisor to simulate a process execution meter for every process.

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