# Jim Sukha

CONTACT URL: http://people.csail.mit.edu/sukhaj INFORMATION

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32 Vassar Street

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RESEARCH **INTERESTS**  Parallel computing, algorithms, synchronization mechanisms, transactional memory, scheduling, work-stealing, dynamic multithreading, cache-oblivious algorithms.

**TEACHING INTERESTS** 

Parallel computing, algorithms and data structures, introductory courses in discrete mathematics, programming, and computer systems.

**EDUCATION Massachusetts Institute of Technology**  Cambridge, MA USA

Ph.D., Electrical Engineering and Computer Science

expected June 2011

• Thesis Topic: Composable Abstractions for Efficient Parallel Programming

• Advisor: Charles E. Leiserson • Cumulative GPA: 5.0/5.0

Master of Engineering, Electrical Engineering and Computer Science,

June 2005

• Thesis Topic: Memory-Mapped Transactions

• Advisors: Charles E. Leiserson and Bradley C. Kuszmaul

• Cumulative GPA: 5.0/5.0

Bachelor of Science, EECS and Mathematics,

June 2004

• Minor in Economics • Cumulative GPA: 5.0/5.0

RESEARCH EXPERIENCE

### **MIT Computer Science and Artificial Intelligence Lab**

Research Assistant in SuperTech research group.

January 2004 to present

Advisor: Charles E. Leiserson

I strive to design provably efficient algorithms and runtime systems that simplify the development of high-performance parallel programs. I have worked extensively with Cilk technology, a dynamic threading platform for multicore programming. My projects include:

• Developed **Nabbit**, a Cilk++ library for parallel execution of task graphs with arbitrary dependency edges in a fork-join language.

Available at http://people.csail.mit.edu/sukhaj/nabbit/.

- Designed **helper locks**, a synchronization abstraction that allows programmers to exploit nested parallelism inside locked critical sections. Implemented HELPER, a prototype of helper locks in MIT Cilk.
- Research on transactions and transactional memory (TM), focusing on extensions to ordinary TM semantics. Contributions include:

CWSTM: Designed a software TM that supports transactions with nested parallelism and nested transactions. The CWSTM design integrates into concurrency platforms that use a Cilk-style work-stealing scheduler.

**Ownership-Aware TM**: Explored semantics of TM and open-nested transactions. Designed ownership-aware TM, a TM system that aims to provide stronger and more intuitive semantics for open-nested transactions.

**Memory-Mapped Transactions**: Developed Libxac, a C library supporting TM semantics on memory-mapped files. Converted existing serial implementations of a B-tree and a cache-oblivious B-tree into concurrent versions using Libxac.

Available at http://people.csail.mit.edu/sukhaj/libxac/.

My ongoing research includes:

- Developing runtime support for confining nondeterminism in dynamic threaded programs.
   Specific goals include guaranteeing deterministic results for parallel psuedorandom number generation and floating point reductions.
- Investigating techniques for improving locality in dynamic threaded programs by using hierarchical work-stealing schedulers, i.e., schedulers that are aware of a system's cache hierarchy.

# TEACHING EXPERIENCE

# **Massachusetts Institute of Technology**

Cambridge, MA USA

#### **6.884** Concepts in Multicore Programming

Spring 2010

*Teaching Assistant*. Developed programming labs for the course. Spring 2010 was the first semester 6.884 was offered. Assisted students with labs and final projects.

## 6.046 Introduction to Algorithms

Fall 2005, Fall 2006

*Teaching Assistant*. Taught a weekly recitation section. Helped devise and grade problem sets and exams. Assisted students with problem sets or other material from class during homework-lab sessions.

# WORK EXPERIENCE

#### Advanced Micro Devices, RAD Lab,

Bellevue, WA USA

Internship

May 19, 2008 – Aug. 15, 2008

Coded a functional simulation for AMD's Lightweight Profiling specification, a proposal for extending the AMD64 architecture to allow user-mode processes to efficiently gather performance data about their execution. Utilized SimNow, AMD's full-system functional simulator.

Google

Mountain View, CA USA

Internship

Jan. 27, 2008 – May 15, 2008

Constructed tools for visualizing click data for ads on mobile devices, with the goal of detecting invalid clicks. Analyzed data using Sawzall, a programming language designed for parallel analysis of large data sets.

#### **Intel, Programming Systems Lab**

Cambridge, MA USA

Internship

May 30, 2006 - Sept. 1, 2006

Implemented Needle, a transparent software transactional memory system based on Pin, a tool for dynamically instrumenting program binaries. Also investigated MySQL's InnoDB storage engine to attempt to try to convert the code to use transactions.

### **MIT Undergraduate Research Opportunities Program**

Cambridge, MA USA

Undergraduate Research Opportunities Program (UROP) Student

• SuperTech Research Group June 2003 – December 2003 Compiler development for Cilk, a language for multithreaded parallel programming. Modified Cilk's source-to-source compiler to add support for atomic transactions.

- SuperTech Research Group June 2002 August 2002 Project studying cache-oblivious algorithms and data structures.
- Advisor: Louis L. Bucciarelli June 2001 August 2001, January 2002 May 2002
   Assembled and programmed an electrical system to collect and transmit data from a rooftop photovoltaic module. Responsible for maintaining both hardware and Java code for processing and displaying real-time data. Developed a photovoltaic module simulation applet. See http://pvbase.mit.edu.

#### **FELLOWSHIPS**

**Siebel Scholar, Class of 2005** — awarded annually for academic excellence and demonstrated leadership to 80 top students from the world's leading graduate schools.

**MIT Presidential Fellowship**, 2004-05 (sponsored by Akamai) — MIT established the Presidential Fellowship program in 1999 to recruit outstanding students worldwide to pursue graduate studies at MIT.

# CONFERENCE PUBLICATIONS

1. Executing Task Graphs Using Work-Stealing.

Kunal Agrawal, Charles E. Leiserson, and Jim Sukha. In *Proceedings of the 24th IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, Atlanta, GA, USA. April 21, 2010.

2. Helper Locks for Fork-Join Parallel Programming.

Kunal Agrawal, Charles E. Leiserson, and Jim Sukha. In *Proceedings of the 15th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP)*, Bangalore India, January 13, 2010.

Also appears as poster at the *Indo-US Workshop on Parallelism*, January 9–10, 2010. Bangalore, India.

3. Safe Open-Nested Transactions Through Ownership.

Kunal Agrawal, I-Ting Angelina Lee, and Jim Sukha. In *Proceedings of the 14th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP)* Raleigh, NC, USA. February 17, 2009.

Other versions of this work include a technical report *MIT-CSAIL-TR-2008-038*, and a brief announcement in SPAA 2008.

4. Nested Parallelism in Transactional Memory.

Kunal Agrawal, Jeremy T. Fineman, and Jim Sukha. In *Proceedings of the 13th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP)* Salt Lake City, UT, USA. February 20, 2008.

5. Memory Models for Open-Nested Transactions.

Kunal Agrawal, Charles E. Leiserson, and Jim Sukha. In *Proceedings of the ACM SIGPLAN Workshop on Memory Systems Performance and Correctness*. San Jose, CA, USA. October 22, 2006.

# Brief Announcements

1. Brief Announcement: Serial-Parallel Reciprocity in Dynamic Multithreaded Languages. Kunal Agrawal, I-Ting Angelina Lee, and Jim Sukha. In 22nd ACM Symposium on Parallelism in Algorithms and Architectures (SPAA). June 13 – 15, 2010. Santorini, Greece.

# 2. Brief Announcement: A Lower Bound for Depth-Restricted Work Stealing.

Jim Sukha. In *21st ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*. August 11–13, 2009. Calgary, Alberta, Canada.

#### **PRESENTATIONS**

1. Executing Task Graphs Using Work-Stealing

International Parallel and Distributed Processing Symposium April 21, 2010
Invited talk at Intel April 7, 2010

2. Helper Locks for Fork-Join Parallel Programming

Principles and Practice of Parallel Programming

Jan. 13, 2010

3. Brief Announcement: A Lower Bound for Depth-Restricted Work Stealing

Symposium on Parallelism in Algorithms and Architectures

Aug. 12, 2009

4. Nested Parallelism in Transactional Memory

Workshop on Transactional Computing

Aug. 16, 2007

5. Safe Open-Nested Transactions

Position paper at IBM Workshop on

Transactional Memory and Programming Technologies

March 5, 2007

6. Memory Models for Open-Nested Transactions

Workshop on Memory Systems Performance and Correctness

Oct. 22, 2006

7. Concurrent Cache-Oblivious B-Trees Using Transactional Memory

Workshop on Transactional Memory Workloads

June 10, 2006

# Professional Service

Reviewed papers the following conferences:

<ul> <li>Principles and Practice of Parallel Programming (PPoPP)</li> </ul>	2011
• International Parallel and Distributed Processing Symposium (IPDPS)	2010
• Symposium on Parallelism in Algorithms and Architectures (SPAA)	2010
• Symposium on Parallelism in Algorithms and Architectures (SPAA)	2009
Chair of Technical Committee, CSAIL Student Workshop	2007 and 2008
Webmaster for MIT EECS Graduate Students Association	Fall 2007
Treasurer for MIT EECS Graduate Students Association	2005-06

# AWARDS

- Winner of Best Paper Award at CSAIL Student Workshop 2009.
- Harry W. Poole Scholar (MIT financial aid award) (2002-03, 2003-04)
- Letters of Commendation for MIT subjects: 6.042 (one of top 5/154, Fall 00), 6.001 (top 17/336, Spring 01), 6.002 (top 10/337, Spring 01), 6.003 (Fall 01), and 6.011 (Spring 02).
- Member of Phi Beta Kappa (2004)
- Member of Eta Kappa Nu (2003)
- Interdisciplinary Contest in Modeling: Member of 2000 NCSSM team ranked Outstanding.
- National Merit Scholarship (2000)
- Robert C. Byrd Honor's Scholarship (2000)
- Siemens Award for Advanced Placement (1998)