Suvinay Subramanian

Massachusetts Institute of Technology

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Research Focus Computer Architecture, Parallel Programming, Computer and Interconnection Networks.

Education

Massachusetts Institute of Technology (MIT) — Cambridge, USA
S.M (Jun'13), Ph.D. in Electrical Engineering and Computer Science — September 2011 – Present
Advisors: Prof. Daniel Sanchez and Prof. Li-Shiuan Peh

Indian Institute of Technology (IIT) Madras — Chennai, India
B.Tech in Electrical Engineering — August 2007 – July 2011

Awards and Distinctions

- Finalist, Qualcomm Innovation Fellowship (2014)
- Institute Blues Award, IIT Madras for all round excellence. (2011)
- OP Jindal Engineering and Management Scholarship (OPJEMS). (2010)
- Honda Young Engineer and Scientist (YES) Award. (2009)
- Olympiad Achievements: (2007)
  - Gold medalist Indian National Chemistry Olympiad (INChO).
  - India Top 1% in Indian National Physics Olympiad (INPhO).
  - Ranked 31^{st} in India in National Science Olympiad (NSO).
- National Talent Search Scholar. 1^{st} rank in Karnataka state. (2005–11)

Publications

Fractal: An Execution Model for Fine-Grain Nested Speculative Parallelism
S. Subramanian, M.C. Jeffrey, M. Abeydeera, H.R. Lee, V.A. Ying, J. Emer, D. Sanchez, *ISCA 2017.*

Data-Centric Execution of Speculative Parallel Programs
M.C. Jeffrey, **S. Subramanian**, M. Abeydeera, J. Emer, D. Sanchez, *MICRO 2016.*

Programmable Packet Scheduling
A. Sivaraman, **S. Subramanian**, A. Agrawal, S. Chole, S.T. Chuang, T. Edsall, M. Alizadeh, S. Katti, N. McKeown, H. Balakrishnan, *SIGCOMM 2016.*

Unlocking Ordered Parallelism with the Swarm Architecture
M.C. Jeffrey, **S. Subramanian**, C. Yan, J. Emer, D. Sanchez, *IEEE Micro's Top Picks from the Computer Architecture Conferences 2016.*

A Scalable Architecture for Ordered Parallelism
M.C. Jeffrey, **S. Subramanian**, C. Yan, J. Emer, D. Sanchez, *MICRO 2015.*

Towards Programmable Packet Scheduling
A. Sivaraman, **S. Subramanian**, A. Agrawal, S. Chole, S.T. Chuang, T. Edsall, M. Alizadeh, S. Katti, N. McKeown, H. Balakrishnan, *HotNets 2015.*

SCORPIO: A 36-core Research Chip Prototype Demonstrating Snoopy Coherence on a Scalable Mesh NoC with In-Network Ordering
B.K. Daya, C.H.O. Chen, **S. Subramanian**, W.C. Kwon, S. Park, T. Krishna, J. Holt, A. Chandrakasan, L.S. Peh, *ISCA 2014.*

No Silver Bullet: Extending SDN to the Data Plane
A. Sivaraman, K. Winstein, **S. Subramanian**, H. Balakrishnan, *HotNets 2013.*

Single-Cycle Multihop Asynchronous Repeated Traversal: A SMART Future for Reconfigurable On-Chip Networks
T. Krishna, C.H.O. Chen, S. Park, W.C. Kwon, **S. Subramanian**, A. Chandrakasan, L.S. Peh, *IEEE Computer, October 2013.*

SMART: A Single-Cycle Reconfigurable NoC for SoC applications
C.H.O Chen, S. Park, T. Krishna, **S. Subramanian**, A. Chandrakasan, L.S. Peh, *DATE 2013.*

Computer Skills

Languages	C/C++, Python, Perl, System Verilog, SQL.
Operating Systems	Linux, Mac OS X, Windows.
Tools	Pin, MATLAB, SPICE, Cadence Virtuoso, Encounter, RTL Compiler, Synopsys DC, PrimePower, Tetramax, Nanosim.

Positions of Responsibility

- Cultural Chair, Indian Students Association, Sangam-MIT. (2012-13)
- EECS Graduate Student Council Representative, MIT. (2011-12)
- Alumni Affairs Secretary, Saraswathi Hostel, IIT Madras. (2009-10)
- Quality Management System Coordinator, Shaastra 2009, IIT Madras. (2009)
- Web Operations Coordinator, Shaastra 2008, IIT Madras. (2008)