An Energy Efficient CMOS Interface to Carbon Nanotube Sensor Arrays

by

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Abstract

A carbon nanotube is considered as a candidate for a next-generation chemical sensor. CNT sensors are attractive as they allow room-temperature sensing of chemicals. From the system perspective, this signifies that the sensor system does not require any micro hotplates, which are one of the major sources of power dissipation in other types of sensor systems.

Nevertheless, a poor control of the CNT resistance poses a constraint on the attainable energy efficiency of the sensor platform. An investigation on the CNT sensors shows that the dynamic range of the interface should be 17 bits, while the resolution at each base resistance should be 7 bits. The proposed CMOS interface extends upon the previously published work to optimize the energy performance through both the architecture and circuit level innovations. The 17-bit dynamic range is attained by distributing the requirement into a 10-bit Analog-to-Digital Converter (ADC) and a 8-bit Digital-to-Analog Converter (DAC). An extra 1-bit leaves room for any unaccounted subblock performance error.

Several system-level all-digital calibration schemes are proposed to account for DAC nonlinearity, ADC offset voltage, and a large variation in CNT base resistance. Circuit level techniques are employed to decrease the leakage current in the sensitive frontend node, to decrease the energy consumption of the ADC, and to efficiently control the DAC.

The interface circuit is fabricated in 0.18 μm CMOS technology, and can operate at 1.83 kS/s sampling rate at 32 μW worst case power. The resistance measurement error across the whole dynamic range is less than 1.34% after calibration. A functionality of the full chemical sensor system has been demonstrated to validate the concepts introduced in this thesis.

Thesis Supervisor: Anantha P. Chandrakasan
Title: Joseph F. and Nancy P. Keithley Professor of Electrical Engineering

Acknowledgments

Thinking back on my arrival at MIT, I am suddenly struck by how much I've learned from MIT, not just in an academic sense, but also in how to love my work, how to love my friends, and most importantly, how to love myself. In the middle of such enlightening experiences stand many people to whom I am indebted.

First, my stay at MIT wouldn't have been as exciting and fruitful without the unwavering support from my research advisor, Professor Anantha Chandrakasan. I really appreciate the fact that he respected every decision I made throughout the master's studies. Anantha taught me that research is not about reading, but about thinking. Without his patience, I would still be reading 10 papers everyday, and have no clue about what I am reading. I'd also like to thank Professor Jing Kong for giving me the opportunities to pursue an interesting research project for the master's thesis.

I've always been waiting for this opportunities to thank my parents, Han Yong and Young Sook, and my little brother, Woon Sang, for perseverance and support they've shown to me. I am so indebted to you all that filling up the whole thesis with gratitude wouldn't suffice to show my appreciation.

The past two years at MIT would have been colorless without the great Anantha group members. Jae, Tao and Fred, THE CNT Group homies, working with you guys have been great! Joyce and Yogesh, I am quite sure that we slowed down many people's graduation by relentless ranting. Denis, thanks for your help/insights/code during the tapeout. Dani and Viv, it would have been a lot of fun working on the H.26456789 project together. Brian, Dave and Naveen, thanks for your invaluable comments on the designed ADC and chip testing procedures. I would also like to thank Korean EECS Mafia (as Anantha puts them) for fruitful *research* discussions during beer nights.

And of course, I would like to thank Margaret for helping me with all the logistics, and also the smiles that kicked off my days.

A graduate student life at MIT is infamous for the loneliness and lack of connections with the world, but I've been so fortunate to have met Myung Jin. She's been

very supportive in whatever foolish mistakes I made, and patient enough to listen to my erratic reasonings when she was busy herself. Thanks Jin! I couldn't have lasted a single day at MIT without you.

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Chapter 1

Introduction

With the advances in communications and Radio-Frequency circuit, the dream of *Ubiquitous Computing* [7] is a step closer to realization. In the heart of ambience intelligence lies the sensors that allow the system to perceive its surrounding and react to it. While much research on sensors has been conducted, sensors suitable for ultra-low power applications attracted the attention of the research community only recently. In particular, chemical/biological sensors have attracted attention from both academia and industry. Several types of chemical sensors have been introduced in the past that can sense fatal chemical/biological agents even in harsh environments. These sensors are designed to be deployed in mass in a wireless sensor network system to make use of the existing computational infrastructure. To fully utilize the resources available from embedded DSP's and RF circuitries, sensors must exhibit high accuracy and reliability at low power consumption.

The objective of this research is to extend upon the state-of-the-art research to develop an energy efficient platform for chemical gas sensors to enable a low-power wireless chemical sensor system. There are several requirements that a battery-operated chemical sensor system must satisfy. Before delineating the specification for the stand-alone low-power CNT chemical sensor system, different types of sensors should be studied, and parcular attention should be paid in analyzing how CNT sensors perform compared with other state-of-the-art chemical sensors. In Section 1.1, different types of sensors will be studied, and different sensing mechanisms will be

explained.

1.1 Chemical Sensor Categorization and Analysis

The main thrust in the development of sensors is on designing, finding or fabricating new materials. The following discussion will focus primarily on the material-driven chemical sensor technologies. Broadly speaking, the material-driven chemical sensors can be categorized as either resistive or capacitive. As the name suggests, a resistive sensor changes resistance when exposed to a chemical of interest, whereas a capacitive sensor changes capacitance when exposed to a chemical of interest.

1.1.1 Capacitive Chemical Sensors

Many capacitive sensors have been published in literature [1] [8][9] and most of them rely on similar sensing mechanisms. The main component in capacitive sensors is a capacitor-structured platform for reaction with chemicals. In most cases, the platform is coated with a specific agent that will either attract or propel the chemical of interest through chemical bonding and/or electrical interactions, and such interactions will change the effective mass of the coated agent. Such a change in effective mass will change the capacitance of the sensing platform by changing the distance between the bottom and top plate of the structure. Since $C = \frac{\epsilon A}{d}$, where A is the area of the capacitive structure and d is the distance between the separated plates, C changes in response to d changes. Therefore, by reading out the value of C, we can measure the chemical concentration.

An apparent advantage of a capacitive chemical sensor is that the readout circuitry can be very simple. In the simplest design, by counting the oscillation frequency of a resonant RC oscillator, where C is formed by the sensor platform, the change in capacitance can be measured. Another advantage of these sensors is that most of them do not require micro hotplates to expedite the reaction rate between the chemical and sensor. This is a significant advantage from the system design perspective because the power consumed by the hotplate can be spared.

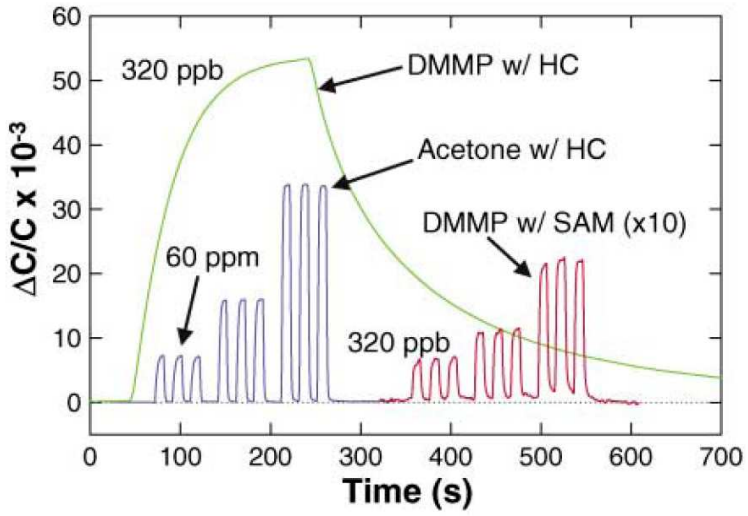


Figure 1-1: Transient response of a capacitive sensor when exposed to various chemicals [1]

The sensitivity of capacitive sensors can be very high, down to 5 ppb [1], and the response time has been demonstrated to be very short even at 50 ppb (< 4 s). However, information on the detection threshold or false positive rate is not given in any papers the author has come across, thus an accurate evaluation of performance is very hard.

One of the considerations for capacitive sensors is that the change in capacitance that needs to be resolved is very small. Usually, the ΔC is dependant on the base capacitance C_O, but C_O is usually small due to the sensor size contraints.

Another drawback of capacitive sensors is that they react with many types of chemicals, even with chemicals that do not interest the system. Many coating technologies have been developed to circumvent this problem, but an effective coating techniques are still under investigation. Figure 1-1 shows the the lack of selectivity and the small change of sensor signal.

1.1.2 Resistive Chemical Sensors

Resistive chemical sensors form another commonly used type of sensors [10][11][12]. The basic mechanism of resistive sensors may vary from one sensor to another, but

the first principle behind the mechanism is either chemical reaction or polarization. In transistor-like sensors, such as Ion-Sensitive FETs (ISFET) [13], a CMOS-like structure is used as a sensor. The difference between the CMOS and ISFET is that the gate of ISFET is coated with a polarized material that either react with or attract the chemical of interest. When the chemical is bound to the gate of the structure, the amount of inversion in the channel of the device changes due to the change in effective gate potential. This, in turn, results in the change of resistance. In non transistor-like resistive sensors, the chemical of interest directly forms a bond with the sensor, which triggers a transfer of excess charge carrier into the sensor. Such a transfer results in the change of resistance.

A sensitivity of resistive sensors may vary a lot from a sensor to sensor, but in general, the sensitivity can be very high ($\sim$ ppt [2]) when heated. Yet, because the statitical information on many sensors is not available in most papers, an accurate performance characterization of sensors is very hard to conduct. Because the sensor has to chemically react (unlike capacitive sensors) with the chemical, the response time is usually longer than that of the capacitive sensors. In most cases, the reaction time is around $1 \sim 10$ minutes, but this can also be reduced through heating and chemical coating.

A drawback of a broad class of resistive sensors is that the sensor's base resistance is hard to control. For example, in nanowire chemical sensors, the base resistance can vary from 1MΩ to 1GΩ [14][15]. Since the sensor signal ΔR is proportional to the base resistance R, the dynamic range of the sensor interface would have to be very wide. This poses a great challenge in power constrained applications.

So far, we have looked at two different types of chemical sensors: capacitive and resistive. A fair comparison among the sensor is very hard to conduct due to limited information provided by the published results. In the following section, carbon nanotube sensors is studied specifically in the context of building a low power chemical sensor system.

1.2 Carbon Nanotube Chemical Sensor

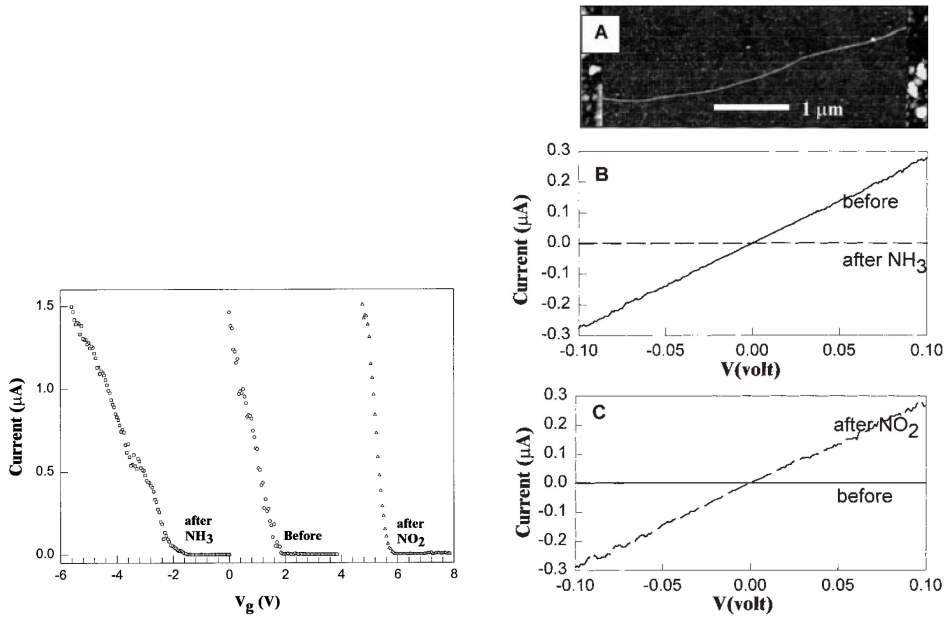
The discovery of carbon nanotubes (CNT) [16] opened up a whole new field of research dedicated to carbon nanotubes. Not only was a particularly queer one-dimensional structure intellectually interesting, but the fantastic ballistic transport property also intrigued many engineers. In the course of investigation, CNTs were shown to be a strong candidate for the next-generation chemical sensor, first introduced in the pioneering work by *Kong et al* [17]. In this chapter, CNTs chemical sensing characteristics will be studied based on the published result in literature, and a scheme to use CNT as a sensor in our system will be described. The chapter will conclude with some measurement results, which is on courtesy of Kyeong-jae Lee.

1.2.1 Carbon Nanotube as a Chemical Sensor

As mentioned, CNTs ability to sense chemicals was first demonstrated in [17]. Since then, many results were published on CNT sensors based on a bare CNT [2], a CNT transistor [10], and a film of CNTs [11]. Each type of CNT sensors has its own advantages, such as easy fabrication steps, high selectivity, high sensitivity and high yield. We have decided to use a bare CNT wire to sense the chemical for its easy fabrication steps, and the high sensitivity.

A bare CNT has shown its ability sense NH_3 and NO_2 as shown in Figure 1-2 [17]. As can be inferred from Figure 1-2(a), a CNT device is a P-type, and the shift of the voltage curve could be understood as the shift in the threshold voltage of the device (the gate in this device is the whole silicon wafer). From another point of view, if the gate voltage is fixed, as in Figure 1-2(b), for instance at V_{GS} of 4V, the CNTs response to the exposure of chemicals could effectively be interpreted as the resistance change of CNTs. Therefore, by reading out the resistance value of CNTs at a fixed gate bias, the concentration of specific gas could be inferred.

The response time, sensitivity, reproduciblity, and recovery time are the key metrics in gauging the performance of sensors. CNT sensors perform favorably compared to other chemical sensors in terms of sensitivity. Figure 1-3 shows that the nanotube



(a) (b)

Figure 1-2: (a) Change of I-V_{GS} curve for CNTs when exposed to NO_2 and NH_3 (b) Change of I-V_{DS} curve for CNTs when exposed to NO_2 and NH_3
J. Kong et al [17]

(when coated) can detect the order of 100 part-per-trillion change of chemical concentration. However, CNTs take more than 500 seconds to fully react with the chemicals in air at that concentration. When the concentration of gas increases, the response time decreases accordingly, as shown in Figure 1-3.

The response time can actually be decreased by applying coating on top of the CNT [18]. The coating increases the bonding sites for more chemical atoms, which in turn decreases the response time to $5 \sim 10$s. Figure 1-3 illustrates a very important characteristic of resistive CNT sensors: the resistance change is related to the base resistance. Therefore, to sense the introduction of 100ppt NO_2 with the sensor proposed in [2], the *relative* resistance change of 1% should be detectable from the interface.

Reproducibility is yet a problem in CNT sensors. Due to the poor process control over CNT fabrication, the base resistance of CNTs varies over a very wide range.

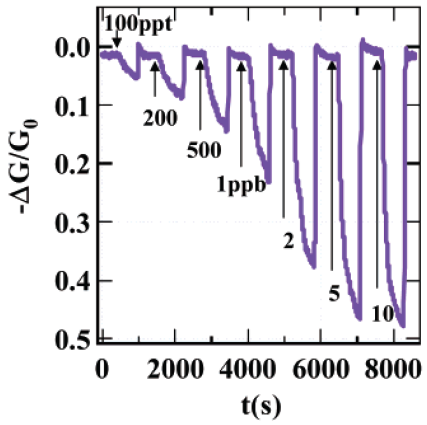


Figure 1-3: Response of CNT to the introduction of NO_2 [2]

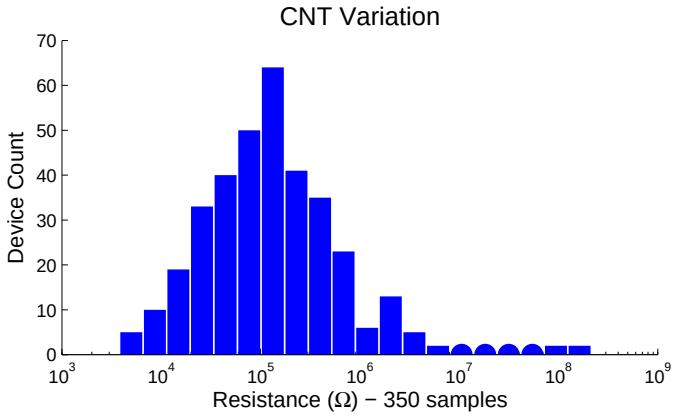


Figure 1-4: Local variation of CNT resistance due to poor process controls [3]

As shown in Figure 1-4, a local variation of CNT resistance takes on the form of log-normal distribution, and the base resistance can be as low as 10kΩ and as high as 10MΩ. Furthermore, the sensor characteristic varies drastically from one tube to another. Such a variation should be accounted for when designing an interface system.

We should revisit Figure 1-3 with Figure 1-4 in mind. In order to sense the change of 1% of resistance when the base resistance of the nanotube is 10kΩ, then the resolution of 100Ω is needed from the interface. The minimum resolvable resistance change from the interface is determined by the low-end of the CNT base resistance,

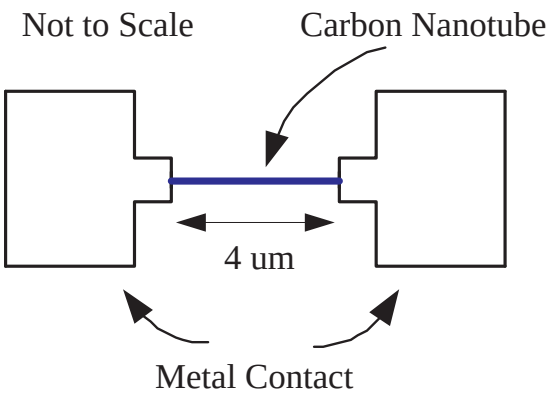


Figure 1-5: Simple CNT device with two metal contacts

not the high-end.

Another major drawback of nanotube sensors is that it takes a long time to recover to the original state (resistance) when the gas disappears. Without any processing on the sensor, it takes about 12 hours for CNTs to return to the original base resistance. Some papers tried to reduce the recovery period by applying UV light to CNTs [2], by heating the CNT to untie the bond between the sensor and chemical [17], or by coating the CNT with appropriate chemicals [18]. The recovery time after the sensor optimization is between 10s and 400s.

Kyeong-jae Lee has characterized the chemical-sensing capability of CNTs [3]. In the next section, the test structure of CNT devices will be introduced and measured results will be shown.

1.2.2 CNT Sensor Design and Measurement

Work introduced in this chapter is carried out by Kyeong-Jae Lee, a graduate student from the department of EECS at MIT, as a collaborative project.

A basic CNT device has been fabricated and electrically tested for functionality. Figure 1-5 shows the device used in the testing. The carbon nanotube is fabricated by the Chemical Vapor Decomposition (CVD) technique at 900 degrees Celcius, using a Fe/Mo-based catalyst. The catalyst is deposited at pre=patterned sites. The length

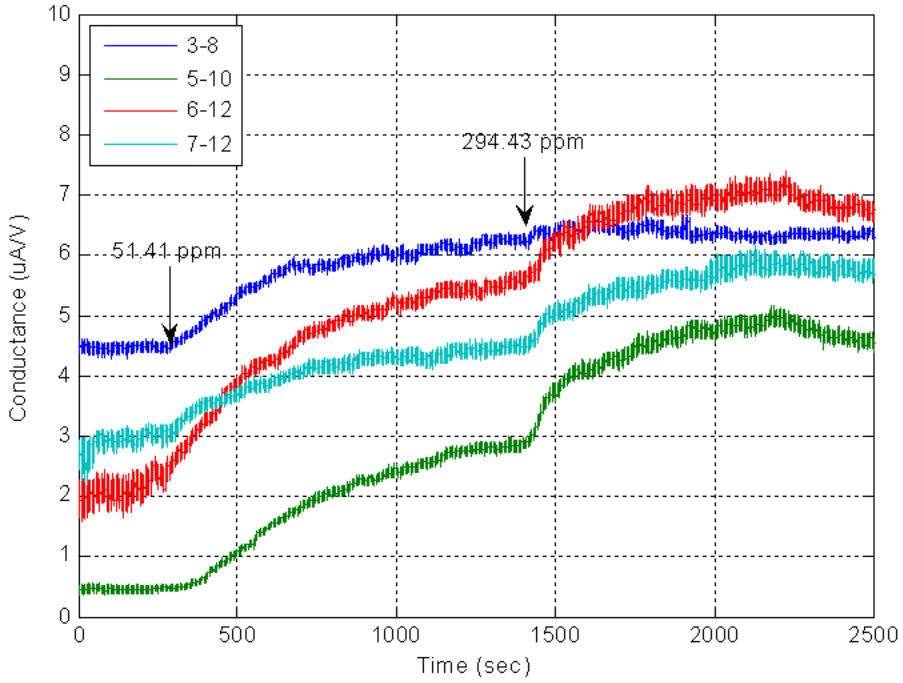


Figure 1-6: The transient response of the fabricated CNT sensors when exposed to NO_2 [3]

of the cahnnel is 4 μm and uses Cr/Au contacts. A comprehensive study on the fabrication of CNT can be found in [19].

We apply no bias to the bulk of the silicon wafer (as is done in back-gated CNT transistors) because the sensor operation does not rely on the transistor characteristic of the nanotube. Thus, the bulk of the wafer is floating in potential.

The initial prototype of the sensor does not have any coating on the nanotube; chemicals that we can sense with bare CNT are NH_3 and NO_2. Figure 1-6 shows the resistance of different CNT devices when exposed to NO_2. As can be seen at t = 0s, the base resistance of each nanotube differs from tube to tube due to poor control over process variations. When 51.41ppm of NO_2 is introduced, the conductance of CNTs increases in a correlated fashion. This is consistent with the information given by [17]. However, the resistance of some tubes changed more than the resistance of other tubes. To correlate the change in resistance to the base resistance, the transfer curve of sensors with different R_{base} is shown in Figure 1-7. The fitted data suggests

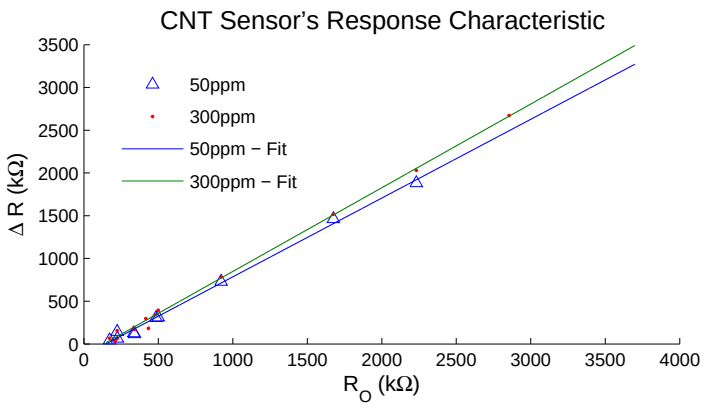


Figure 1-7: The sensor characteristic showing the proportionality of ΔR to R_{base} [3]

that the ΔR is proportional to R_{base}. Furthermore, different concentration of chemical gives rise to a differing slope. Therefore, the slope information can be used to infer the gas concentration.

Although the response time of CNT sensors is fast, the recovery time of the CNT sensors is quite slow. To see that the CNT sensors still retain the sensing capability after the sensing operation, nanotubes that were already exposed to the chemicals were left to oxidize in air for 5 days. Then the CNT sensors were re-exposed to the chemicals, and the transient response was observed. From the experiment, we could see that the CNT sensors exhibit good sensitivity after the oxidation procedure. Thus, as long as the CNTs are given enough time to recover from previous sensing operation, the CNT sensors are reusable.

Detailed analysis on sensors used in this system is available in [3].

1.3 Thesis Contribution and Organization

The focus of this thesis is on developing the chemical sensor system shown in Figure 1-8. A chemical sensor system is composed of a chemical sensor (could be an array of chemical sensors), an analog frontend to interface the sensor, and the digital backend signal processing unit. To minimize the delay through the sensor system, the response time of the sensor should be short, and the readout rate of the interface circuitry must

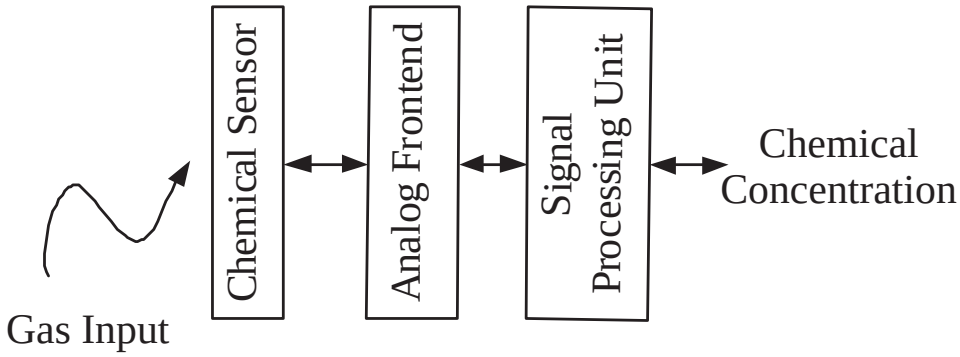


Figure 1-8: Abstract illustration of the stand-alone chemical sensor system

be high. Furthermore, to attain high accuracy of the sensor system, not only does sensor need to have high accuracy, but also the interface system. If the system in Figure 1-8 is to be implemented for the sensor network, the stringent power budget on the sensor platform should be taken into account along with other constraints.

This thesis proposes an energy efficient CMOS interface circuitry to resistive chemical sensors. A carbon nanotube (CNT) has been chosen for the chemical sensor considering a number of outstanding characteristics. In Chapter 2, an energy efficient architecture to accomodate a wide dynamic range will be described. A number of architectural optimizations will be performed to minimize the energy consumption per resistance readout operation. In Chapter 3, circuit optimizations on each circuit block will be described, and simulation results will be shown. In Chapter 4, the chip measurement result will be discussed. The effect of each calibration schemes described will be studied, and possible sources of performance degradation will be studied. The designed interface will be connected to the CNT sensor arrays, and the performance of the full system will be described. In Chapter 5, the contribution of the thesis will be described, and possible future research directions will be studied.

Chapter 2

CMOS Interface Circuitry - Architecture

As mentioned earlier, a large variation in the CNT base resistance and the requirement imposed on the minimum resolvable resistance change translate into a wide dynamic range specification for the CMOS interface circuitry. In this chapter, CNT sensors' characteristics will be analyzed to formally define an adequate specification for the CMOS interface, and explore the opportunities to optimize at the architecture level. In the course of architecture development and optimization, previous work in literature will be delved into to study how the wide dynamic range requirement is met for different sensor applications, and how the dynamic range and power trade off with varying specifications. At the end of the chapter, a new energy efficient architecture will be proposed that accomodates both the wide dynamic range and low power consumption.

2.1 CNT Sensor Interface Specifications

From the CNT sensor characteristics, a number of specifications for the interface circuitry can be determined. As was mentioned in the previous chapter, the minimum resistance change in CNTs when exposed to a reasonable amount of chemicals ($\sim$ 100ppt) is about 1% relative to the base resistance [20][2]. Thus, by being able to

resolve a 1% change in resistance, the effective chemical concentration can be inferred from the CNT resistance measurements. If the nanotube base resistance does not vary much from tube to tube, the minimum resolution requirement on the interface would be 7-bits. However, due to the poor control in carbon nanotube fabrication steps, the base resistance actually varies from 10kΩ to 10MΩ in a log-normal fashion, as introduced in the previous chapter.

To determine the effective dynamic range required in the presence of base resistance variation, consider the smallest resistance change that needs to be resolved. The smallest change could be when a CNT with 10 KΩ base resistance reacts with the chemicals to change its resistance by 100 Ω. Thus, by denoting a 100 Ω as the LSB of the resistance output word, the dynamic range requirement translates into 17 bits. It's interesting to notice that while the dynamic range requirement is 17 bits, the resolution requirement is only 7 bits at each base resistance level. This property could be exploited to reduce the power consumption of the circuit.

Since a carbon nanotube exhibits a statistical variation in its characteristics (such as base resistance, maximum current drive, metallic/semiconducting), the sensor characteristics may vary from a tube to tube in a similar fashion. As can be reasoned from the law of large numbers, by increasing the number of sensor cells in the system, the reliability of the sensor system can be enhanced. Thus, an interface circuitry that can accomodate an array of sensor cells should be developed. The ability to accomodate an array of sensor cells should not come at a large overhead on the interface side. The useful functionality, mainly the analog frontend, of the interface should be reusable among many sensor cells. Therefore the interface is designed to time-multiplex the existing analog frontend resources. This may increase the readout rate requirement on the interface, but such an increase in the readout rate is tolerable since the reaction rate for each sensor is very low.

Another restriction on the interface circuitry is the maximum current through the nanotube sensor cell. The nanotube can only withstand upto 30 μA of current [21]; above 30 μA of current drive, the tube breaks. Since most of the sensor cells will be composed of a single nanotube, the maximum current supplied to each sensor cell

should be constrained to be less than 30 μA.

On top of all these requirements, the limited power budget allocated to a sensor system should also be taken into account when designing the interface. The ultimate goal of this system is to operate from the energy derived from an energy-scavenging circuitry [22], which could deliver upto tens of microwatts. Thus, the power consumption of the circuit should be constrained to be below tens of microwatts. These specifications are summarized below in Table 2.1.

Table 2.1: Required Performance Specifications for the Interface Circuitry

Resolution	$\sim$ 1% change from the base resistance
Dynamic Range	10kΩ $\sim$ 9MΩ (17 bits)
Readout Rate	$\sim$ 1 sec / tube
Maximum Current	$\sim$ 30 μA / Sensor Cell
Power Budget	$\leq$ 50 μW
Number of Sensors on a System	More than 10 sensor cells

2.2 Previous Work

Several papers on CMOS interface to resistive gas sensors have been published in the past. An interesting thing to notice is that the large dynamic requirement is common to most resistive sensor interfaces. The work by Grassi [4] achieves a dynamic range upto 27 bits by controlling the gain in the amplifier stage according to the sensor resistance, as shown in Figure 2-1. The interface generates a reference voltage across the sensor with a low-impedance-output digital-to-analog converter (DAC), which sets a constant potential across a sensor cell. The voltage across the sensor induces a current through the sensor, and the generated current gets converted into voltage by an adaptive gain amplifier stage. The voltage at the output of the gain stage is then read off by a high precision ADC to determine the resistance of the sensor. By interleaving detection ranges and calibrating the circuitry off-chip, the linearity error between gain settings is minimized.

In another implementation of the resistive gas sensor interface [5], an OPAMP

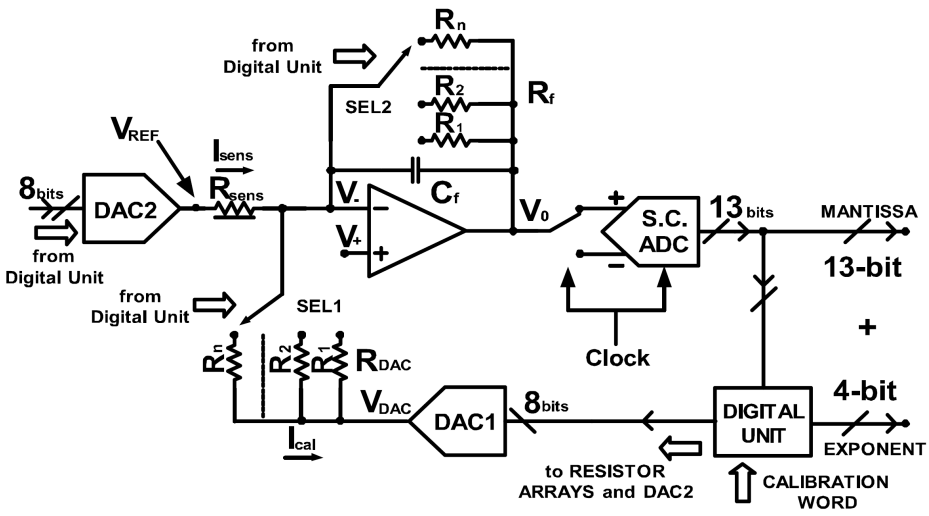


Figure 2-1: Circuit architecture introduced in [4] to attain wide dynamic range.

is wrapped around a NMOS as shown in Figure 2-2 to generate a constant voltage bias across the sensor, which generates a constant current based on the value of the resistor. The generated current is integrated on a known capacitor, and by measuring how long it takes to charge and discharge the capacitor of a known value, the current is converted into a digital word. This concept stems from a time-to-digital converter. When the current is known, the resistance value is easily calculated by taking the ratio of voltage and current. This implementation attains the dynamic range upto 18 bits with an off-chip calibration scheme and the resistance range selection with different capacitors in the integrator.

An interface circuitry specifically targetting the CNT gas sensor application has also been introduced [23]. This circuitry incorporates the concept of sensor array in the sensor system, and the relatively simple circuitry doesn't seem to require high power to operate.

The previously published work all focus on different domains of applications; in our design, we will focus on constraining the power consumption of the interface.

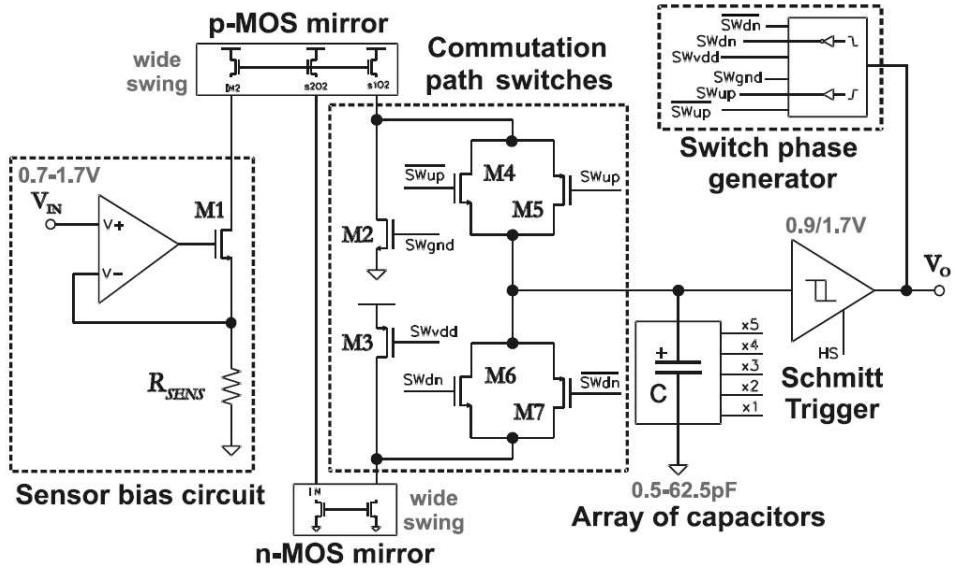


Figure 2-2: Interface architecture to readout the resistance with a Time-to-Digital Converter [5]

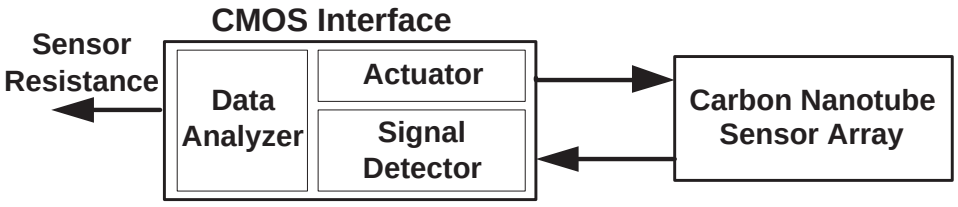


Figure 2-3: General concept of a sensor interface chip

2.3 Proposed Architecture

Fundamentally, every sensor interface should have an actuator, which excites the sensor to be tested, a signal detector, which detects the signal, and a data analyzer, which analyzes the signal from the detector. These components can be visualized in a block diagram as shown in Figure 2-3.

The systems that were studied in Section 2.2 can be viewed from a different perspective in light of Figure 2-3. The interfaces introduced in [4] and [5] both actuates the sensor with a voltage source, and measures the voltage signal from the sensor. In our design, we opt to actuate the directly with a variable current source,

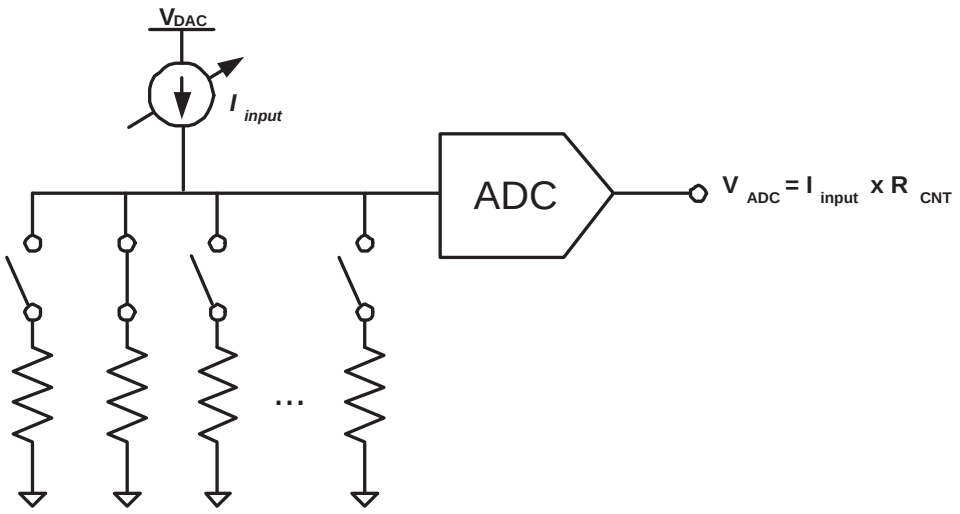


Figure 2-4: Basic idea of the proposed architecture

and measure the voltage from the sensors.

2.3.1 Idea Behind the Proposed Architecture

The main idea behind the proposed architecture is that the interface can directly actuate the sensor with a current source, and measure the voltage to calculate the resistance of the sensor cell, as shown in Figure 2-4. By doing so, the need for an OPAMP to generate a virtual ground, or the need for an OPAMP to generate a constant voltage across the sensor can be eliminated.

Interestingly, this idea sheds light on the possibility to attain 17-bit dynamic range with analog blocks of smaller dynamic range. By intelligently controlling the current input to different resistors, the voltage at the input of the ADC can be constrained to be less than the supply voltage across a wide resistance range.

Another interesting feature of this idea is that it provides a coarse absolute resolution in the high-resistance range, and a fine absolute resolution in the low-resistance range. Since $R_{LSB} = \frac{V_{LSB}}{I_{Input}}$, as the input current is increased, the minimum resolvable resistance change will decrease. Yet, current cannot arbitrarily be increased; in order to keep the output voltage within the supply rail, there exists a maximum current that can be supplied to a certain resistor. This maximum value is small for large resistors

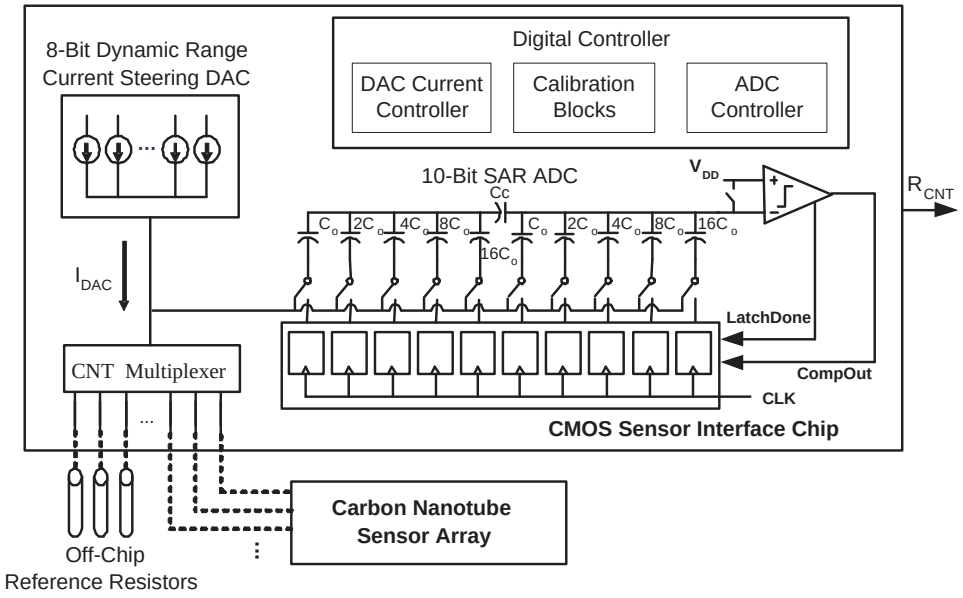


Figure 2-5: The proposed system architecture

and large for small resistors, which results in the varying absolute resolution feature just described. The interface should be designed such that whatever the absolute resolution is at each resistance level, the 7-bit resolution requirement is met across the whole dynamic range. In effect, the current source sets the minimum resolvable resistance and the operating range of the interface.

Extending this idea to the system-level, the proposed architecture is shown in Figure 2-5. Analog blocks in the interface operates at the supply voltage of 1.2V and the signal processing unit operates at the supply voltage of 0.5V.

The current source is not implemented as a voltage-to-current converter, but rather as a current-steering digital-to-analog converter (DAC). By doing so, the input word to the DAC itself is the digital representation of the current the interface sources the sensor cells. The minimum current (I_{LSB}) in the DAC is 100nA. The ADC is implemented in a successive approximation register (SAR) scheme, which has a good energy performance in moderate resolution, moderate speed applications [6]. The sensor system employs 24 CNT sensor cells; 7 ports to the 32-to-1 multiplexer are used for a calibration purpose that will be described later in this chapter, and the remaining 1 port is used for the ADC testing purpose. Figure 2-5 also illustrates

other blocks that will be explored more in depth in the upcoming chapters.

2.3.2 Architecture Optimization

In order to achieve 17 bits of dynamic range, it's necessary that the sum of the dynamic range in ADC and DAC should exceed 17 bits. In this work, the system will target 18 bits of dynamic range in order to account for the non-ideal characteristics of circuit blocks. In the course of the reasoning thus far, a metric to break down the dynamic range requirement into two sub-blocks is missing. Thus, a new constraint is posed, which is set by optimizing the energy performance of the system.

$$E_{SYSTEM} = P_{ADC} \times T_{ADC} + P_{DAC} \times T_{DAC} + E_{DIGITAL} \tag{2.1}$$

Conceptually, it can be shown that there exists an optimal number of bits that should be allocated to the ADC, with the given dynamic range requirement.

The above equation assumes that the digital signal processing is done in background and the time it takes to calculate the resistance is not in the critical path of the interface system: the time it takes to calculate the resistance based on the measurement result is much shorter than the time it takes to complete the analog operations. Equation 2.1 further assumes that the interface is designed to turn on only one analog block at a time. In other words, the time it takes to readout a resistance value is $T_{sense} = T_{ADC} + T_{DAC}$ and the operation of the DAC and ADC is mutually exclusive. This assumption is valid because ADC doesn't need to operate while the DAC needs to generate the output voltage; the DAC doesn't need to sustain the input voltage while the ADC converts the input voltage into a digital word. ADC internally samples the input voltage with the capacitive DAC, thus the DAC can safely be turned off during the ADC operation.

At this point, let's consider a typical value of P_{ADC} and P_{DAC} to get a brief idea of how much energy each system block consumes. The maximum current that the DAC can provide the nanotube is 30 μA from Table 2.1, thus the DAC power with V_{DD} of 1.2V is on the order of 40 μW when the DAC is fully turned on. The worst

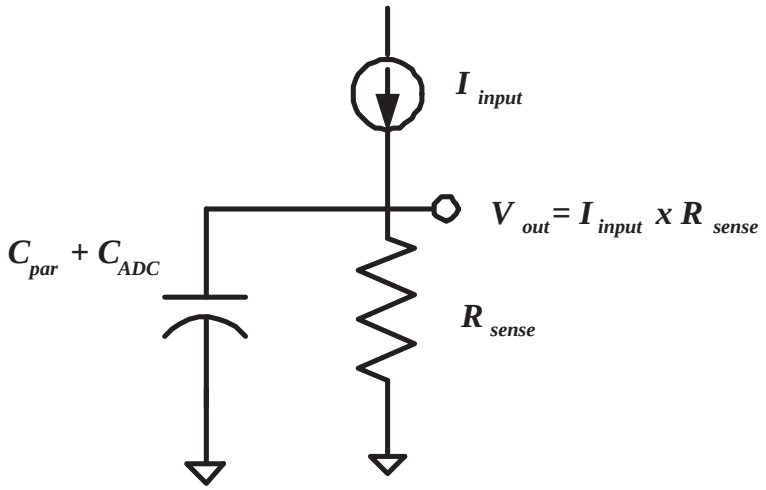


Figure 2-6: Basic concept of this architecture with an illustration of the parasitic capacitance at the input Node

case ADC power can be deduced from the figure of merit (FOM): the state-of-the-art moderate resolution moderate speed ADC's attain a FOM of 125 fJ/Conversion step at the time of this writing. Assuming that the performance this ADC targets is 25kS/s, 10-bit resolution, and the FOM of about 250 fJ/Conversion step, the ADC power is on the order of 6.5 μW. From this back-of-the-envelop calculation, it is clear that it'd be better to operate ADC longer than the DAC given the T_{sense}.

Yet, as shown in Figure 2-6, there exists a large capacitor at the input of the ADC. This large capacitor results from an off-chip wiring of the CMOS Interface and CNT sensors, capacitance from the PAD, drain capacitance from the CNT multiplexer, drain capacitances from the DAC, and *the input capacitance of the SAR ADC*. Due to a large capacitor at the input of the ADC, the on-time of the DAC is much larger (due to the RC settling of the voltage) than the on-time of the ADC, which counters our previous preference.

What's interesting to note is that the on-time of the DAC and the on-time of the ADC both increase with the number of bits allocated in the ADC. While the increase in T_{ADC} is clear, the increase in T_{DAC} is due to the fact that as the resolution of the SAR ADC increases, the number of capacitors in the capacitive DAC within the SAR ADC also increases. Because the capacitive DAC serves as the input to the SAR

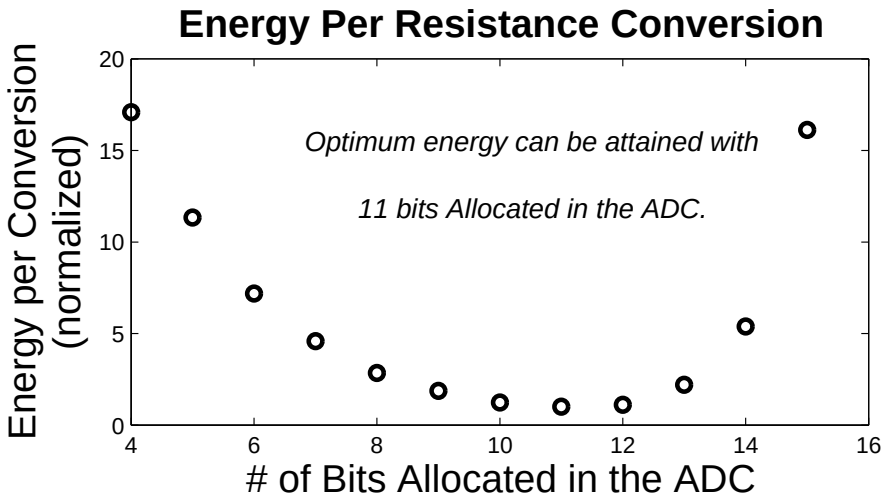


Figure 2-7: Energy consumed by analog circuit blocks per resistance conversion

ADC, the RC time constant at the input node increases as the number of capacitors, thus the ADC resolution, increases. This, in turn, results in the increase of T_{DAC}.

On the other hand, the maximum power in the DAC decreases as the number of bits allocated in the ADC increases. Thus, there is a trade off subjected to minimizing the energy consumption of the system to increase the resolution of the ADC in order to decrease the maximum power in the DAC at the expense of longer T_{DAC}, longer T_{ADC} and higher P_{ADC}. In order to determine the optimum number of bits to allocate in the ADC and DAC, a careful modeling of the voltage settling time (T_{DAC}), on-time of the ADC (T_{ADC}), and the power consumed by each block (P_{ADC}, P_{DAC}) is called for. The detailed procedure of the architecture optimization process is given in Appendix A.

2.4 Energy Optimization Simulation Results

Models derived in Appendix A is used to calculate the energy consumption of the system as the ADC resolution varies. Since $E_{DIGITAL}$ is a constant term, only the analog blocks' energy consumption is considered. As shown in Figure 2-7, the energy consumed by the system is minimized when 11 bits of dynamic range is allocated to the ADC and 7 bits to the DAC. Notice that the optimum is quite shallow around 10

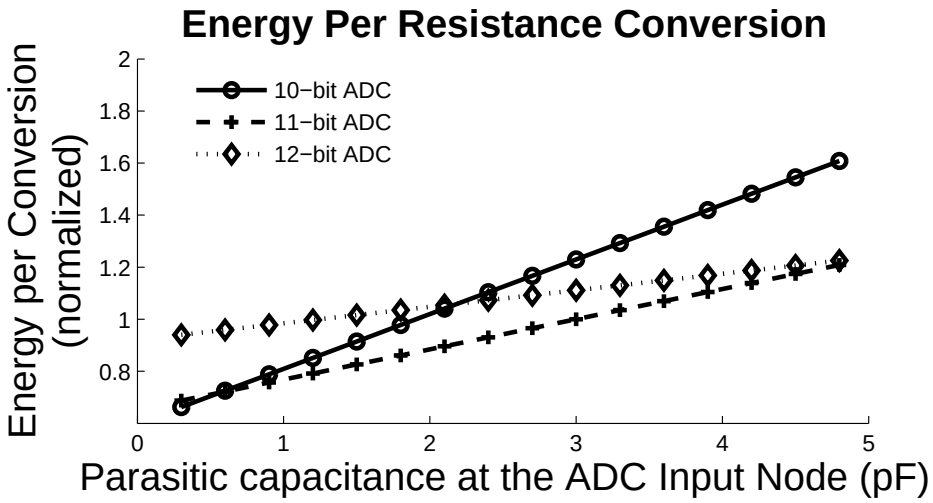


Figure 2-8: Energy changes in each ADC setting due to $C_{PARASITIC}$ variation

to 12.

In developing the model, the value of $C_{PARASITIC}$ was assumed to be 3pF. To validate the optimization result, for configurations in which 10, 11, and 12 bits are allocated to ADC, the parasitic capacitance value is varied to see how the energy consumed by the analog blocks varies (Figure 2-8). Interestingly, 10-bit ADC and 8-bit DAC pair performs the best when the parasitic capacitance is very small, while the 12-bit ADc and 6-bit DAC pair performs the best when the parasitic capacitance is large. However, in most cases, 11-bit ADC performs the best across the C_{PAR} values of interest.

To see how the sensing rate varies as the ADC resolution changes, f_{RATE} is defined as

$$f_{RATE} = 1/(T_{DAC} + T_{ADC}) \tag{2.2}$$

Figure 2-9 shows how the readout rate of the interface varies as the ADC resolution changes. It's interesting to observe that as more bits are allocated to the high-resolution ADC's, the readout rate decreases more rapidly than the case where the resolution is increased in the low-resolution ADC's. This is due to the fact that the input capacitance of the ADC starts to dominate the parasitic capacitance, which is assumed to be 3pF.

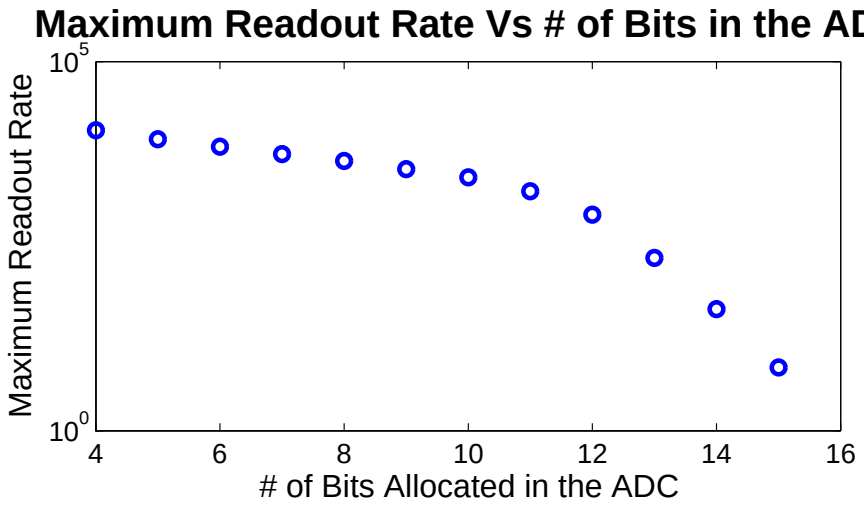


Figure 2-9: Sensing rate changes as ADC resolution varies

To decide on how many bits to allocate in the ADC, both the energy and rate have been considered. As the number of bits in the ADC exceeds 10 bits, the maximum readout rate decreases more rapidly. Although the readout rate is not critical when the number of sensors in the system is not too large, in order to have a very large array of sensors, it's desirable to have as high a readout rate as possible. Best trade-off in terms of rate can be attained with 10-bit ADC in the system, as shown in Figure 2-9. With 10-bit ADC and 8-bit DAC pair, the ADC input capacitance just starts to dominate over the parasitic capacitance. In other words, we are getting the most out of the increased ADC resolution to decrease the P_{DAC} when 10-bit ADC is used.

As mentioned, the optimal energy performance is attained with 11-bit ADC, but **we used a 10-bit ADC and a 8-bit DAC in our implementation.**

2.4.1 DAC Current Control Scheme

Determination of DAC Current In The Resistance Readout Mode

During the readout mode, the interface must first determine how much current is to be sourced to the sensor. From the former discussions, the purpose of the DAC is to set the range of operation for the interface. If the interface allows 2^8 combination of current levels, many combinations of the DAC current and the ADC output could

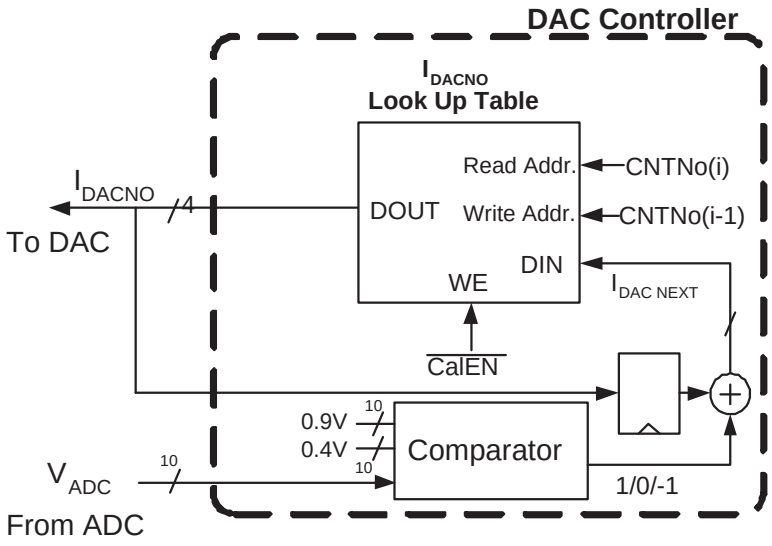


Figure 2-10: DAC current for the subsequent measurement is stored in the look-up table.

result in the same resistance.

A system-level control to deal with such an overlap in the operational range would be very complicated. Thus, two constraints are introduced to simplify the DAC current control.

1. For a given sensor, largest current is sourced while meeting the voltage headroom constraint from the DAC. This will be studied more in depth in the next chapter.

2. DAC can only provide binary multiples of I_{LSB} current (100nA, 200nA, 400nA, 800nA etc...)

Note that the first constraint assumes that the interface has a knowledge of what the resistance of the sensor roughly is. To get around this problem, for the given CNT, the resistance measurement from the i^{th} trial is used to determine the DAC current for the $i + 1^{th}$ measurement. This is justifiable since during the readout mode, when the sampling rate is high enough, the current CNT resistance value will closely track the CNT resistance value from the previous measurement. This guarantees that the circuit can track the resistance of each CNT sensor in real time operation, providing appropriate current even when the resistance changes.

The first constraint is implemented as shown in Figure 2-10. The look up table

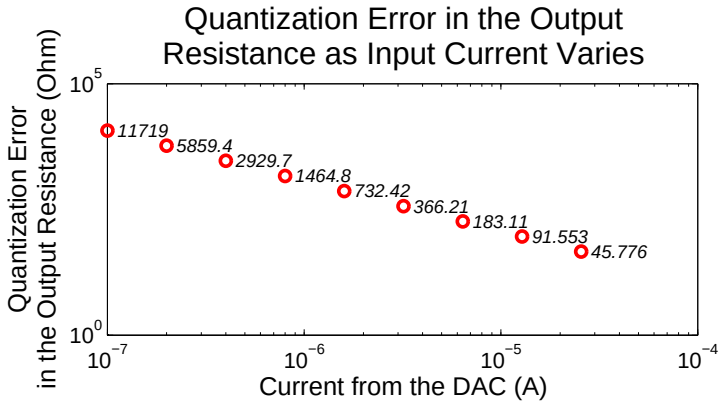


Figure 2-11: Absolute quantization error arising from the quantized nature of the ADC and the DAC

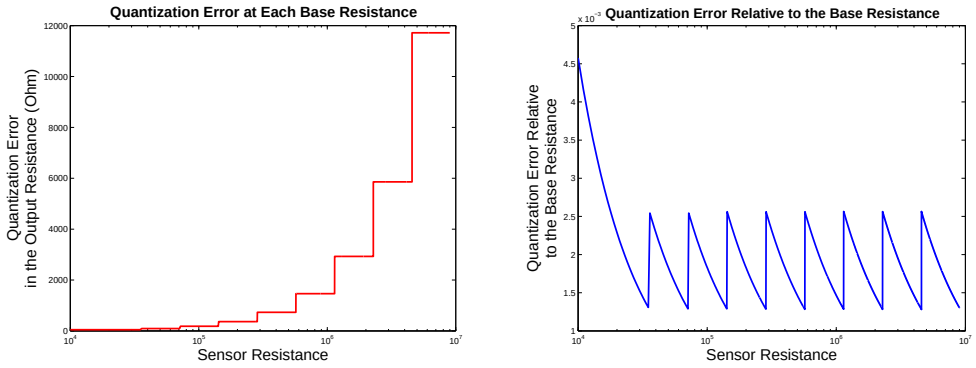
has entries that are the current to be sourced in subsequent resistance measurement for each CNT's. Therefore, each nanotube has an entry in this look up table. The entry is determined as the following: for a given CNT, say CNTNo 7, during the current resistance measurement, the voltage from the CNTNo 7 is compared with 0.4V and 0.9V with the comparator. If the voltage is smaller than 0.4V, the current is increased by two-folds since the voltage from that sensor will still be less than 0.9V; if the voltage is larger than 0.9V, the current is decreased by two-folds to constrain the voltage to be below 0.9V.

Based on the above current control scheme, a quantization error that arises at each current setting can be characterized from Equation 2.3.

$$R_{Quantization} = \frac{V_{LSB}}{I_{DAC}} \tag{2.3}$$

$R_{Quantization}$ is the minimum resolvable resistance value at a given I_{DAC} setting. Figure 2-11 shows how $R_{Quantization}$ varies as the DAC current is varied. Note that the y-axis is in a log scale.

Furthermore, it's a straight forward task to calculate the quantization error at a certain base resistance, and what the portion of the quantization error is relative to the base resistance. Figure 2-12 shows the calculation result. Note that the quantization error is below 0.5% across the measurement range, which meet our specification of



(a) (b)

Figure 2-12: Figure 2-12(a) shows the absolute quantization error at each resistance level, and Figure 2-12(b) shows the quantization error relative to each resistance level

1% accuracy.

Determination of DAC Current At Power Up

We have implicitly assumed that the nanotube resistance is approximately known when determining the DAC current in the resistance readout mode. However, such an assumption does not hold when the interface is just turned on. Furthermore, some of the nanotubes may not be usable for the developed sensor interface because the base resistance may be out of the detection range. When the nanotubes are not usable, they should be discarded from further resistance measurements to increase the energy efficiency of the system. Therefore, a scheme to bin the usable and non-usable nanotubes, and to set the initial DAC current for each of the usable tubes is necessary. In fact, the above specification can be met by estimating the R_{CNT} for each tube before the interface enters the readout mode.

To formally justify an extra step to bin the nanotubes, consider the following scenario. When R_{CNT} is 1MΩ, 25.6μA of current input will ideally result in 25.6V, which is much higher than the supply voltage. On the other hand, when R_{CNT} is 10kΩ and the input current is 100nA, the output voltage is only 1mV, which is smaller than the V_{LSB} of the ADC. Therefore, we need to have a rough estimate of what the

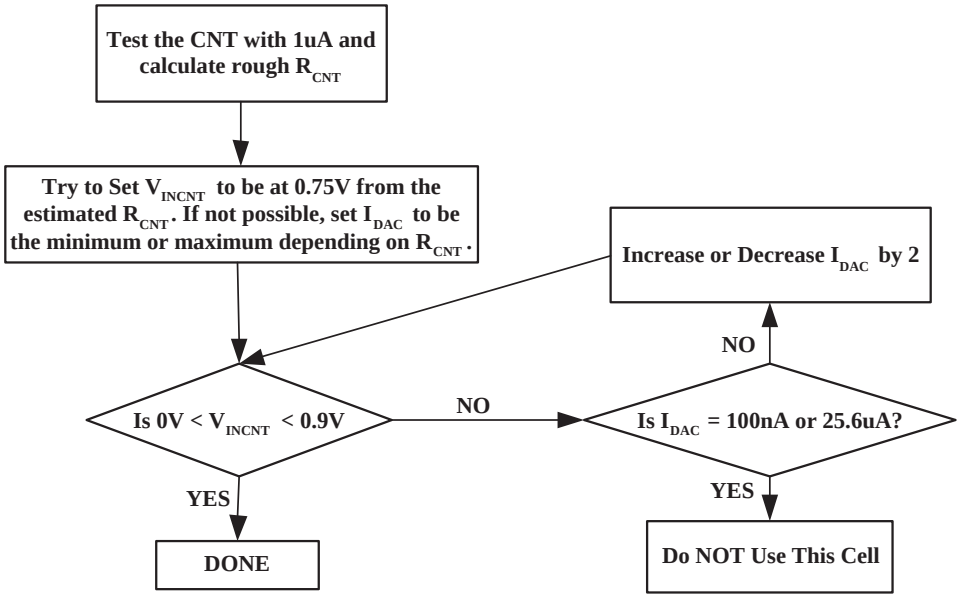


Figure 2-13: Current adaptation scheme to ensure the proper functionality of the system

R_{CNT} is before the readout operation begins. The current adaptation scheme is carried out after the DAC calibration step (explained in the next section), but they can be switched in sequence if needed because the current adaptation scheme does not depend on the absolute value of I_{DAC}.

Figure 2-13 shows the flow chart for the employed current adaptation scheme. As the current adaptation loop starts, a CNT is tested with 1μA to calculate the rough estimate of R_{CNT}. Note that the resistance calculated here is rough because R_{CNT} could be greater than 1MΩ, which would then result in V_{INCNT} greater than 1V. As we mentioned earlier, the voltage swing is constrained to be 0.9V due to the voltage headroom constraint in current sources, and any resistance measurement with voltage higher than 0.9V is inaccurate.

From the estimated resistance, the interface circuit first tries to set the sensor output voltage to be 0.75V. If a certain DAC current can generate V_{INCNT} of about 0.75V from the estimated R_{CNT}, the current adaptation scheme proceeds with that current setting. If R_{CNT} is too small or large such that 0.75V is not attainable even at maximum or minimum DAC current, the interface sets the DAC current to be the

maximum and minimum, respectively. After setting the DAC current, the adaptation scheme carries out another resistance measurement on the same CNT to check that V_{INCNT} is within the detection range. If V_{INCNT} is either 0V or greater than 0.9V and I_{DAC} is neither minimum nor maximum, the current is increased or decreased by a factor of 2, respectively. With the new I_{DAC}, the system checks again whether the input voltage is within the operational range. The loop will continue until V_{INCNT} is within 0 and 0.9V, and the DAC current for the sensor cell is determined to be the current setting at that trial. If V_{INCNT} is 0 at the maximum DAC current, the nanotube is characterized as a short (could be a metallic tube) and it is not used further in detecting the chemical. If V_{INCNT} is above 0.9V at them minimum DAC current, the nanotube has a resistance greater than 9MΩ, and is not used further in chemical detection.

Such an adaptation scheme is carried out for all nanotube sensors individually, and the determined DAC setting for each tube is stored in the system. The adaptation scheme can be thought of as successively approximating the right I_{DAC} on a binary scale. The binning of the tubes, which accompanies the current adaptation for usable tubes, is of great importance in the presence of defects on CNTs.

2.5 Circuit Optimization at the System Level

So far, we have ignored how the sub-block's nonideal characteristics affect the total system's behavior. In this section, we will study how the performance degradation in ADC, DAC and multiplexer affect the dynamic range and resolution of the interface, and devise system level calibration schemes to overcome the limitations posed by these blocks.

2.5.1 Digital-To-Analog Converter Calibration Logic

In this section, several nonidealities in the current-steering DAC will be studied and a digital calibration scheme to overcome such nonidealities will be described. Because the current from the DAC is a known value to the system, it's critical that the functionality of the DAC is the same as what the system expects from it. As a matter of fact, there is only one thing that the system expects from the DAC: the current provided by the DAC is the same as what the system wants to actuate the sensors with. Any deviation of the current from the DAC results in degradation of both the resolution and dynamic range of the interface.

Types of Error in the DAC and Their Impact

Consider the I_{LSB} of the DAC. We have assumed throughout the previous discussions that I_{LSB} is 100nA. However, if I_{LSB} differs from 100nA, performance degradation arises in numerous ways. When I_{LSB} is greater than 100nA, the maximum resistance that the interface can sense goes down. This is a direct consequence of the fact that the maximum voltage at the input of the ADC is constrained to be 900mV. When the sensor resistance is large, I_{LSB} is used to measure the resistance. However, when I_{LSB} is greater than 100nA, 900mV is reached with smaller resistance value. Therefore, the dynamic range at the high-end of the resistance is decreased. When I_{LSB} is smaller than 100nA, the current level at every DAC word will be smaller than the predefined value assuming that the DAC current is linear to the DAC input word. Such a decrease in current results in lower resolution because the minimum resolvable

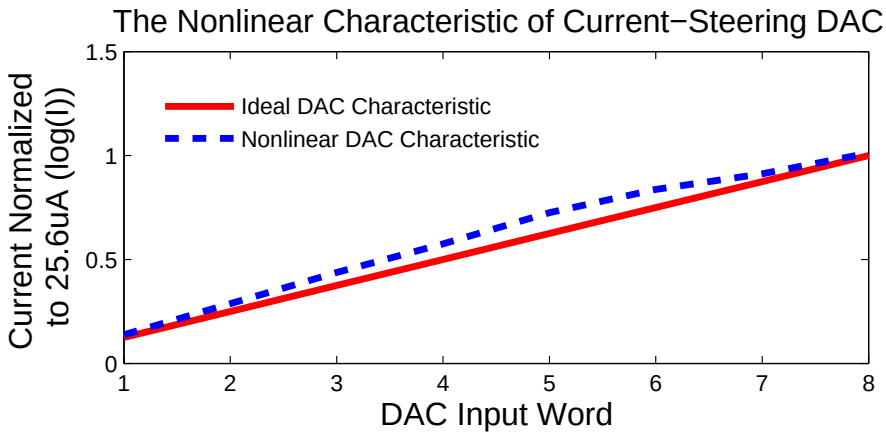


Figure 2-14: An illustration of the nonlinear characteristic of current-steering DAC

resistance can be expressed as $\frac{V_{LSB}}{I_{DAC}}$. Since I_{DAC} is decreased for every DAC word, the minimum resolvable resistance at every DAC configuration is reduced.

The deviation of I_{LSB} from 100nA could solely result from the global process variation. For a same voltage bias, the current from a DAC cell varies over 200nA as process corner is varied (simulated result based on the model provided by the fabrication facility). Such a current difference is definitely not acceptable for our application. The global process variation is exacerbated by the local random process variation.

Until now, we've been quite optimistic. The current variation is exacerbated when I_{DAC} is nonlinear to the DAC word. Figure 2-14 illustrates this problem. If the DAC has a nonlinear characteristic, the definite current value for a given DAC word cannot be determined without Figure 2-14. Such a nonlinearity is caused from the random process variation and the limited output resistance of the DAC current cells. The threshold voltage variation is especially troublesome in our application because in a weak inversion regime, current has an exponential dependence on the threshold voltage, which results in a large current deviation from the expected value. In fact, 10mV change in the input-referred bias voltage causes 20nA of current change in the designed DAC cell, which is 20% of the I_{LSB} in this system. The leakage current in the ESD protection circuitry further aggravates the linearity of the DAC: the diode leakage in the PAD cell amounts to 30nA. Interestingly, the leakage from the PAD

cell is approximately constant over the voltage of our interest, and can be treated as an offset to every DAC configuration.

Consider how the DAC nonlinearity and offset appear in the measured resistance. Since

$$R_{CNT} = \frac{V_{MEASURED}}{I_{DAC}} \tag{2.4}$$

when I_{DAC} is smaller than the expected value, R_{CNT} will be overestimated, while when I_{DAC} is greater than the expected value, R_{CNT} will be underestimated. Therefore, both the offset and nonlinearity of DAC causes a linearity error in the measured R_{CNT}.

System-level DAC Error Compensation Schemes

To circumvent the performance limitation posed by the DAC nonidealities, several techniques have been employed on this interface. First of all, an off-chip voltage source is used to bias the DAC to have more flexibility in setting I_{LSB}. Although a manual tuning of the bias voltage is not desirable for sensor node applications, the 200nA of current difference from the global process variation alone is not acceptable.

In order to address the nonlinearity of DAC, an on-chip calibration scheme is used. Several calibrations schemes have already been introduced in literature to enhance the linearity of a current-steering DAC [24][25], and these schemes corrected the *amount* of current supplied by the DAC. The basic operation of these calibration schemes rely on first characterizing the DAC performance using an ADC, and adding or subtracting extra current with a calibration DAC. For our interface architecture, an ADC is provided for free, which significantly reduces the overhead of DAC calibration. Furthermore, we don't need to correct the amount of current. As long as the system can measure exactly how much current is provided by the DAC, it can calculate what the resistance is from Equation 2.4. Therefore, the calibration problem for this interface becomes measuring how much current is output for each DAC word. Fortunately, there are only 9 different current levels for the DAC, which implies that the DAC can be fully characterized with 9 calibration words (CAL_N).

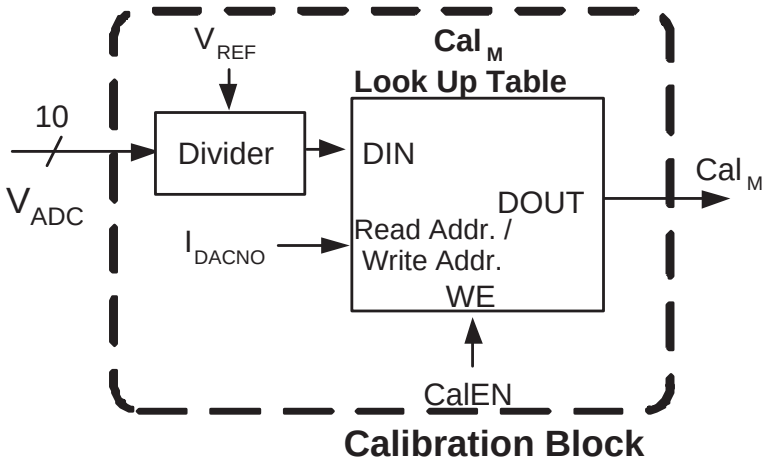


Figure 2-15: Calibration words are stored in the look-up table.

The proposed calibration scheme is summarized in Figure 2-15. The digital controller has a separate calibration mode during which it updates the calibration word look-up table. Calibration words can be calculated through the following relation.

$$R_{CNT} = \frac{V_{MEASURED}}{I_{REAL}} \equiv \frac{V_{MEASURED}}{I_{IDEAL}} \times CAL_N \tag{2.5}$$

where I_{IDEAL} is the predefined current level (ideal current) and I_{REAL} is the actual current delivered by the DAC. In fact, CAL_N can easily be determined from the following observation.

$$CAL_N = \frac{I_{IDEAL}}{I_{REAL}} = \frac{V_{REFERENCE}}{V_{MEASURED}} \tag{2.6}$$

where $R_{REFERENCE}$ is a known reference resistance, $V_{REFERENCE}$ is the voltage that would be measured by the system if the DAC current is the same as the predefined current, and $V_{MEASURED}$ is the actual voltage measured by the ADC. What Equation 2.6 tells us is that the calibration word can easily be calculated by measuring the voltage generated from a known resistor at a certain DAC configuration. Note that $V_{REFERENCE}$, $R_{REFERENCE}$ and I_{IDEAL} are already stored in the system memory.

In order to achieve the desired accuracy, the resolution of CAL_N in Equation 2.6 should be determined accordingly. The goal of the DAC calibration scheme is to

Table 2.2: $R_{REFERENCE}$ for Different Current Setting

DAC Current	$R_{REFERENCE}$
100nA	3.76MΩ
200nA	1.88MΩ
400nA	940KΩ
800nA	470kΩ
1.6μA	470kΩ
3.2μA	237KΩ
6.4μA	118kΩ
12.8μA	30kΩ
25.6μA	30kΩ

attain a linearity error less than 0.01 I_{LSB} for the 8-bit DAC. Assuming a fixed-point arithmetic operation, the first 2 bits of CAL_N are used for representing integers, and the bits from MSB-2 to LSB are used for decimal points. Limiting the integer bits to 2 does not limit the performance in our application because the ratio of $V_{REFERENCE}$ and $V_{MEASURED}$ will not exceed 4 with very high probability.

To attain 1% accuracy in DAC, 8 bits are needed to represent the decimal points in CAL_N. Therefore, 10-bit representation of the CAL_N would suffice the resolution requirement for the interface (if all other parts operate ideally). However, considering that the ADC will also contribute some error to the calibration scheme, CAL_N is represented with 12 bits, opening up the possibility of attaining error less than 0.1%. $R_{REFERENCE}$ used is shown in Table 2.2.

So far, we haven't considered the error from $R_{REFERENCE}$. If the error from $R_{REFERENCE}$ overwhelms the accuracy goal of our calibration, the whole scheme would not work. Fortunately, off-the-shelf resistors can attain accuracy down to 0.05% [26], which is more than a factor of 6 smaller than the error we are trying to calibrate. Thus, the accuracy of ΔI is not constrained by the error in $R_{REFERENCE}$. The effect that ADC non-linearity has on the proposed DAC calibration scheme is studied in Appendix B.

2.6 Digital Controller

Figure 2-16 shows the full digital controller written in verilog. The whole digital controller operates at 0.5V to enhance the energy performance of the system. As soon as the chip is turned on, the DAC calibration block is enabled to calculate the DAC calibration words (CAL_N) for each DAC configuration. When the DAC calibration is done on every DAC word, DAC current adaptation block is enabled to estimate the R_{CNT} of each nanotube. The Next DAC word for each nanotube is stored in the Next DAC Word Generator, which also performs the DAC word calculation during the readout mode.

The simulated power consumption for the digital block is about 1.2μW.

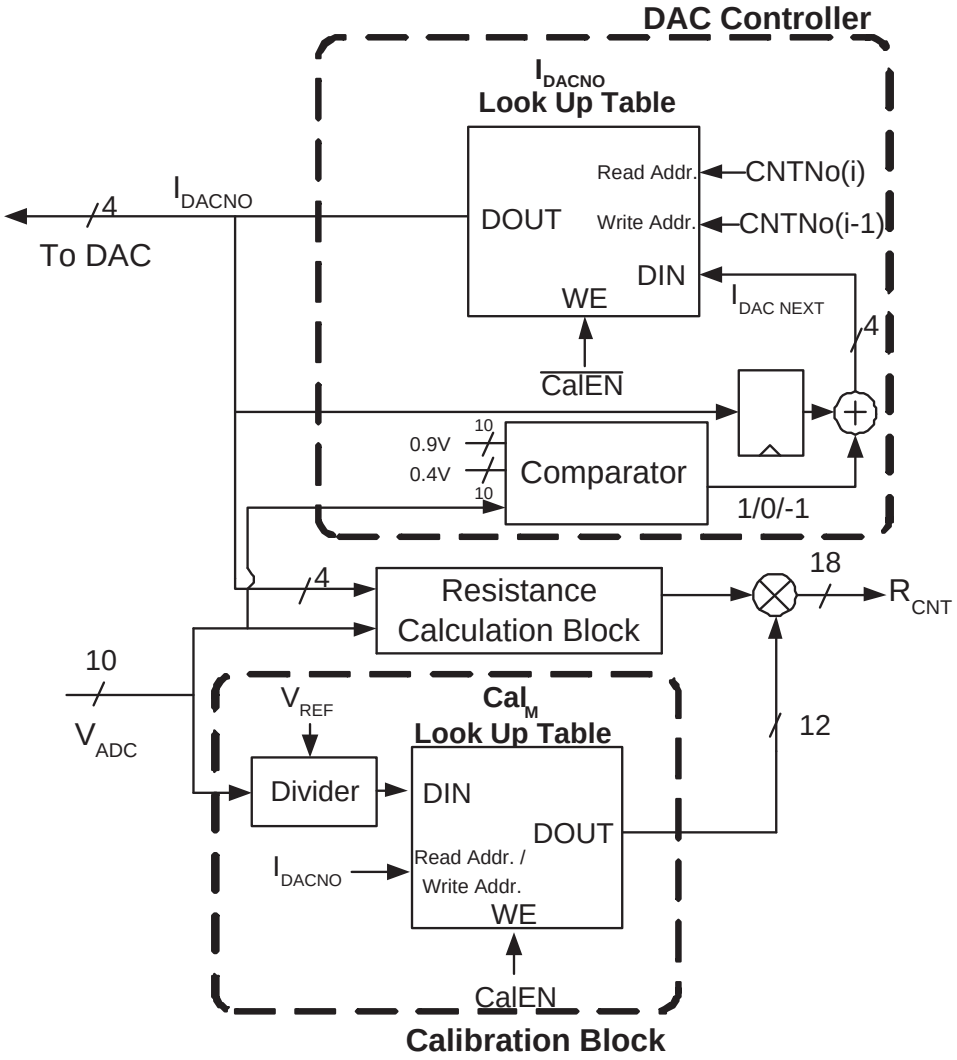


Figure 2-16: The block diagram for the digital controller integrated on the system

Chapter 3

CMOS Interface Circuitry - Circuit Design

Chapter 3 will discuss enabling circuit blocks for the proposed interface. In Section 3.1, the implemented control scheme to duty-cycle the ADC will be introduced. In Section 3.2, the bit-cell structure for the current steering DAC will be discussed, and the performance will be characterized. In the developed sensor array interface, the on-resistance of the multiplexer should be minimized to get a good linearity in the measurement. In Section 3.3, a scheme to multiplex nanotube sensors will be studied.

3.1 Analog-to-Digital Converter

Low energy ADC is one of the most important blocks for the developed interface system. ADC effectively performs the function of signal detector in the interface model introduced in Figure 2-3. While the conversion rate is not critical, the energy needed per voltage sample conversion is an important parameter to enable the low energy sensing of the resistance. As introduced earlier, Successive Approximation Register (SAR) scheme was chosen in light of this requirement, because SAR scheme is one of the most energy efficient ADC architecture for medium resolution medium conversion rate applications [6].

The static linearity is a critical measure for this application; SAR ADC attains

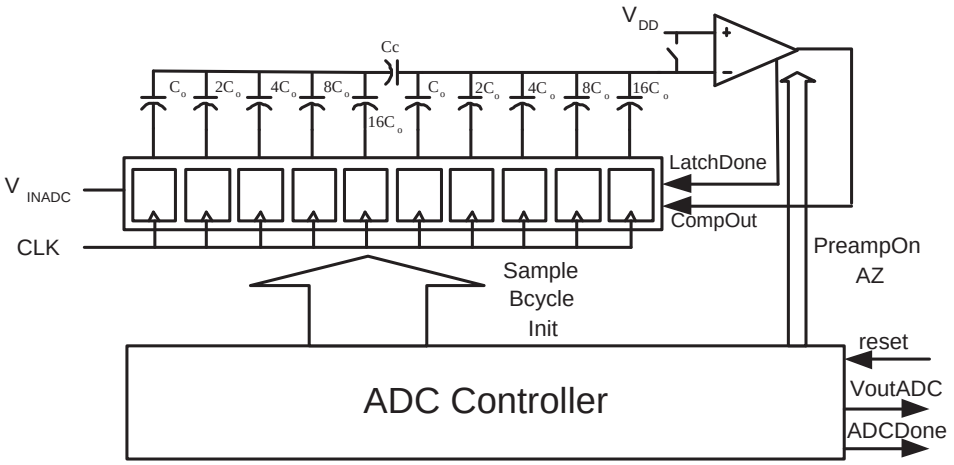


Figure 3-1: Successive approximation register ADC implemented in this interface

a good static linearity performance since the linearity is primarily determined by the matching of the input capacitive DAC. With poly-poly capacitors in modern processes, precise matching of capacitors upto 13-14 bits can be attained([27]).

For this interface, 30kS/s, 10-bit single-ended SAR ADC is designed for this interface. This ADC implements two features: duty-cycling to reduce power consumption; variable sampling period to accomodate a large variation of parasitic capacitance.

3.1.1 SAR ADC Fundamentals and the Control Scheme

The full SAR architecture used in this interface is shown in Figure 3-1. Fundamentally, the SAR converter conducts a binary search to determine the digital word for the input voltage. In doing so, a capacitive DAC is used to perform the binary search. A resistive DAC could also be used, but it would result in a high static power dissipation and large die area. V_{DD} is used as the reference voltage to decrease the design complexity at the cost of possible power supply noise injection.

An attractive property of the SAR converter is the simple control sequence: only needed signals are *initialization, sample, bit-cycle*. These signals are usually complemented with new signals to improve performance. As mentioned in the previous chapter, the sampling period for the ADC can be long. To save energy during that time frame, the analog blocks in the ADC should be turned off while sampling the

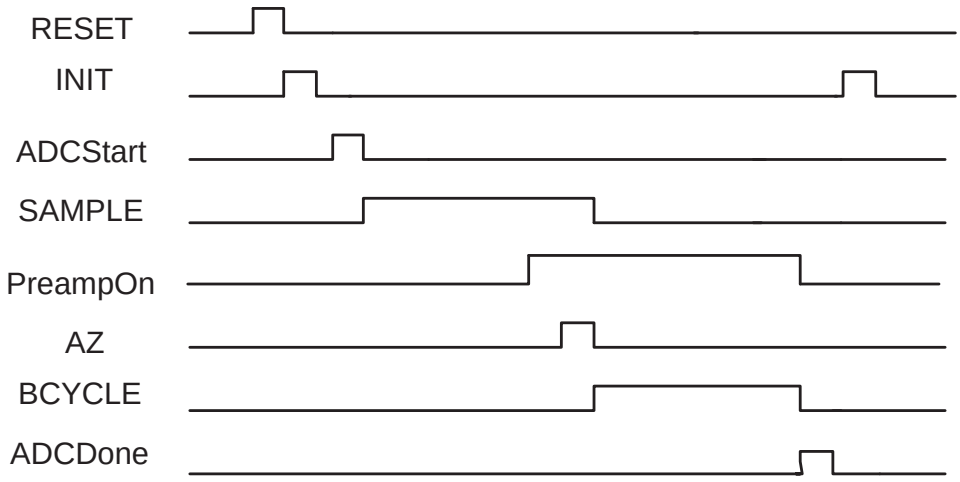


Figure 3-2: Control sequence for the designed SAR ADC

input. PreampOn signal is introduced to duty-cycle the comparator, which results in an energy saving proportional to the off-period of the comparator. PreampOn signal will also be used to turn off the comparator if the operational readout rate of the interface is low. In addition to duty-cycling, an auto-zeroing (signal AZ) is implemented to reduce the effect of offset error in the comparator.

The main control signals among ADC controller, successive approximation register arrays and the comparator are illustrated in Figure 3-2 for one conversion cycle. These signals are also annotated inFigure 3-1. INIT is an internal signal for the ADC to reset itself, while RESET is the global reset signal for the whole system. Note that the comparator is turned on slightly earlier than the start of the bit-cycle to settle the bias current in the pre-amplifier.

Within one conversion cycle, the bit-cycle operation proceeds from the MSB bit to the LSB bit. To trigger the start of the lower bit bit-cycling, a self-resetting scheme is used in this ADC [28]. This scheme starts the next bit-cycling operation as soon as the comparator resolves the input voltage difference. LatchDone signal, generated by the comparator, is introduced to flag the end of the previous cycle and start of the new bit-cycling period.

In the following sections, several circuit blocks in the ADC will be introduced. For each block, the functionality, major challenges, and the solution will be presented

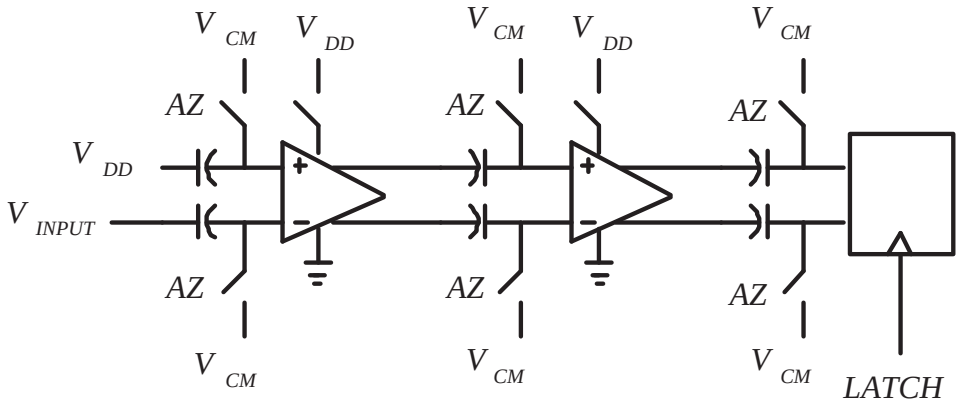


Figure 3-3: The topology of the comparator used in the SAR converter

and evaluated through simulations.

3.1.2 Comparator

In order to achieve 10-bit resolution at 1.2V, the comparator should be able to resolve 1.17 mV. The comparator is sized appropriately such that a gain of 10 from the preamplifier stages would be sufficient for a low-offset operation of the ADC. To attain low power and reasonable bandwidth, a two-stage preamplifier, each with $3 \sim 4$ of gain, is used. The topology of the comparator is shown in Figure 3-3. When the input of the comparator is near 1.2V, the input NMOS transistors are in the linear region, which degrades the gain. An AC- coupling approach is used to increase the gain of the first stage preamplifier, as shown in Figure 3-3.

During the auto-zeroing phase, the input of the first stage preamplifier is reset to the common mode voltage, and the input voltage of the preamplifier fluctuates around the common-mode voltage during the successive bit-cycle operations. The common-mode voltage is generated from the ratioed transistors, and is about 0.55V. The use of AC-coupling capacitors may introduced some gain reduction due to the bottom plate parasitic capacitance, but the benefit gained from the higher gain in the first preamplifier stage is greater.

Figure 3-3 also illustrates how the power-down mode is implemented. By having

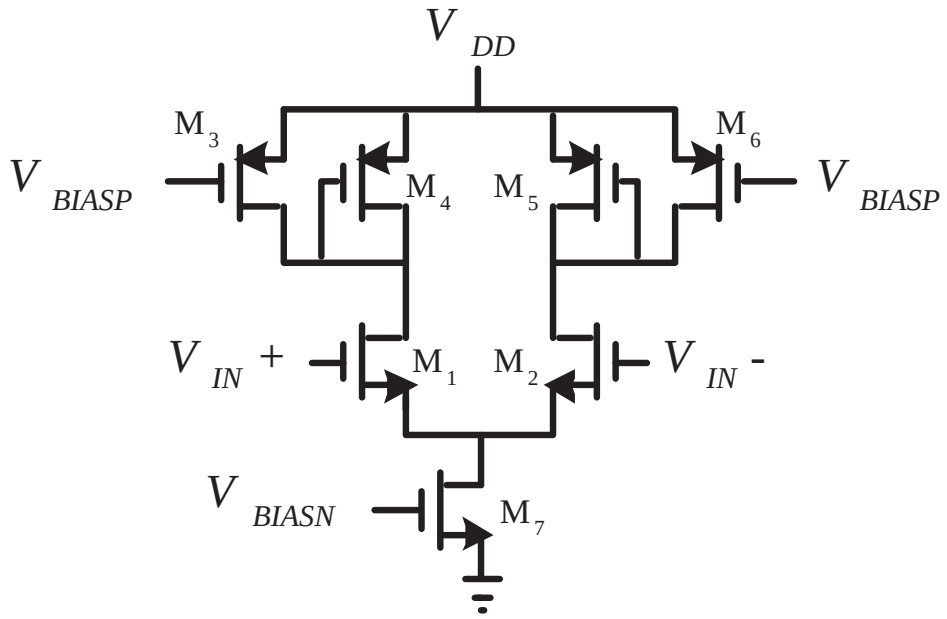


Figure 3-4: The preamplifier used in the comparator

a power-gating transistor between the power supply and the *virtual power supply* of the preamplifiers, the analog bias through the preamplifier can be turned off [6]. The sizing of this power transistor is also of an issue because the virtual power supply should be very close to V_{DD} and should be very clean. A large transistor could be used to powergate the preamplifiers, but that would incur more overhead in turning the power transistor on and off [29]. The sizing was determined through a number of simulations to take the peak current requirement into account.

Figure 3-4 shows how each preamp stage is implemented. The preamplifier has four PMOS load transistors ($M_3 \sim M_6$). In an ordinary amplifier, M_4 and M_5 would be missing to take advantange of the large impedance looking into the current source. However, this would degrade the bandwidth of the amplifier due to the large effective resistance at the output node. In order to reduce the gain and set a known voltage at the output node, a low impedance path to the supply voltage is created by diode-connected PMOS transistors (M_4 and M_5). The PMOS loads not only enhance the stability of the amplifier by setting a fixed DC bias at the output node, but also increases the bandwidth even with the extra capacitance that might incur.

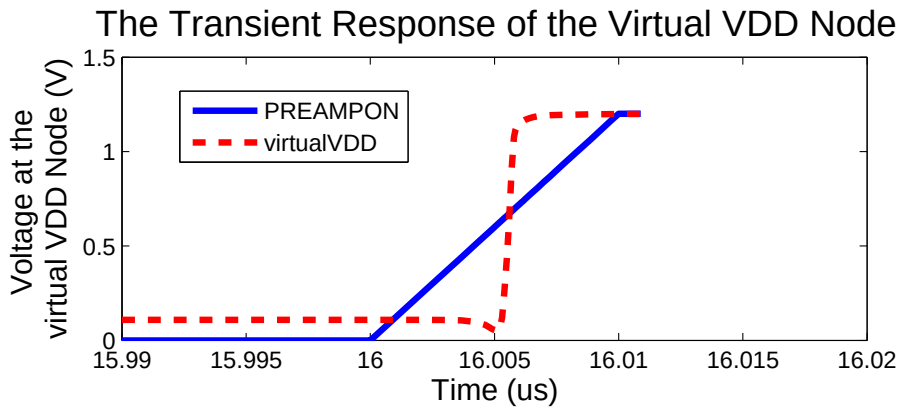


Figure 3-5: The transient response at the virtual supply rail when the preamplifiers are turned on

In the implemented ADC, the preamplifiers are designed to consume about 400nA of current in the active mode. The current bias in the second preamplification stage was designed to be the same as the first preamplifier stage to have adequate bandwidth in the preamplification stage, and also to ensure the correct operation of the amplifier.

In order to assure the functionality of the preamplifiers in the presence of power gating, the transient response of the voltage at the virtual supply rail node is characterized (Figure 3-5). Figure 3-5 shows the response at the virtual V_{DD} node when the preampOn signal has a risetime of 10ns. 10ns is a conservative estimate of the risetime of signals within the chip. As is evident, the virtual VDD node turns on very rapidly, thus there is no delay penalty in power gating the preamplifiers. In the actual implementation, however, one clock cycle was dedicated for preamplifier bias settling to ensure the correct behavior of the preamplifier.

The preamplifiers need two analog voltage references, V_{BIASP} and V_{BIASN}, to generate the constant bias current, as shown in Figure 3-4. These signals are generated by the bias generator shown in Figure 3-6. M_1 is degenerated by an external resistor (of size 190 KΩ) to generate a constant current, and the current mirror circuitries are used to generate the bias voltages. The bias generator is also turned off through PreampOnB signal whenver the preamplifiers are turned off. This is to save the static power consumed in the bias generator during the turn-off period. Furthermore, this bias generator permits the interface to have an external voltage bias for better

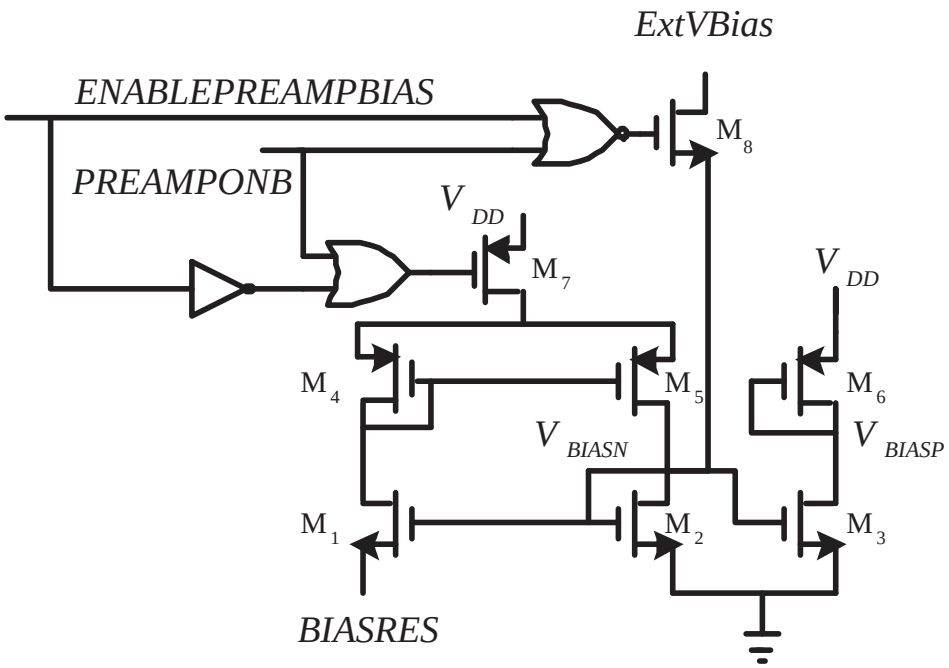


Figure 3-6: Voltage reference generator for preamplifier bias voltages

testability. When ENABLEPREAMPBIAS signal is asserted, the bias generator runs off the internal bias circuitry; when ENABLEPREAMPBIAS signal is grounded, then the external voltage bias is used to bias the preamplifiers. Instead of a full transmission gate configuration, only one NMOS (M_8) is used; a PMOS is not needed because the external bias voltage is likely to be smaller than 0.6V, and M_8 will be in the linear region.

The final stage in the comparator is a simple latch shown in Figure 3-7. The two output ports are precharged to V_{DD} when the LATCH signal is low, and the LATCH signal is high, the input is latched by the cross-coupled inverters. The cross-coupled inverters are degenerated by NMOS transistors (M_2 and M_4) to limit the current drive available based on the input voltage. The purpose of M_3 is to balance the voltage at intermediate nodes as well to further enhance the symmetry. Since the latch is clocked, there is no static power dissipation, and the energy consumed per voltage conversion predominantly depends on the parasitic capacitance at the output node.

Figure 3-8 shows the transient response of the latch in the ADC. As you can see,

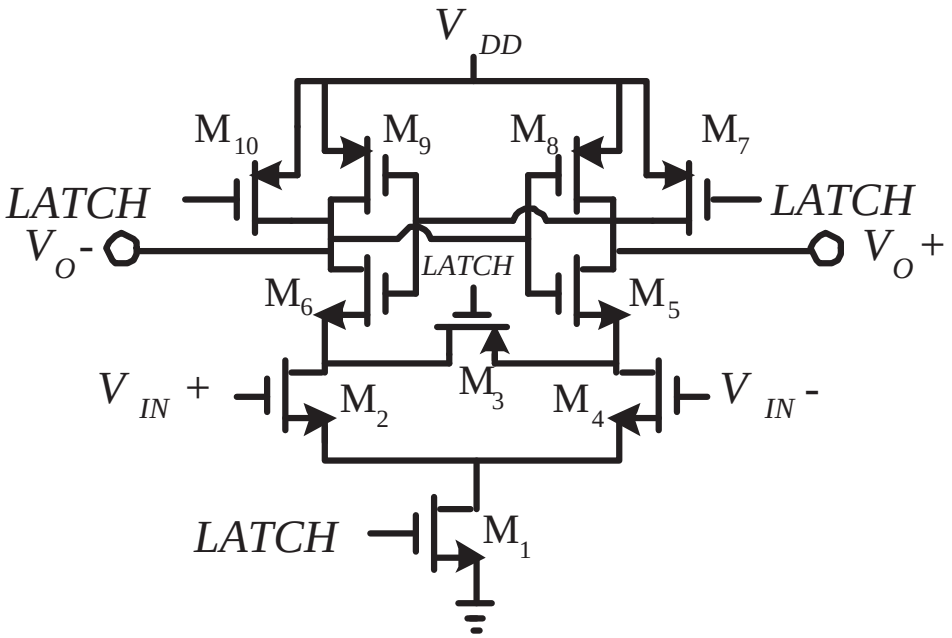


Figure 3-7: Latch implemented in the comparator

the latch resolves within 4ns even with a small differential voltage at the input. The bottom figure in Figure 3-8 shows the operation of the comparator when the input of the ADC varies by an LSB. This is an extracted simulation of the comparator circuitry. As is evident, the comparator can correctly resolve the difference of 1mV without any offset. As soon as the comparator resolves, the bit-cycle operation starts immediately. LatchDone signal for the self-resetting SAR is generated by a modified NAND circuitry Figure 3-9. If one of the comparator outputs is grounded, the NAND circuit flags high to signal the completion of the comparison operation.

3.1.3 Capacitor DAC Design

The Digital-to-Analog converter within the SAR converter plays a critical role in realizing a good static linearity of the system. A sub-DAC implementation reduces the input capacitance of the ADC a great deal, and also significantly reduces the area for the capacitor array. The functionality of a sub-DAC from the voltage level generation stand point can be understood as interpolating between voltage levels

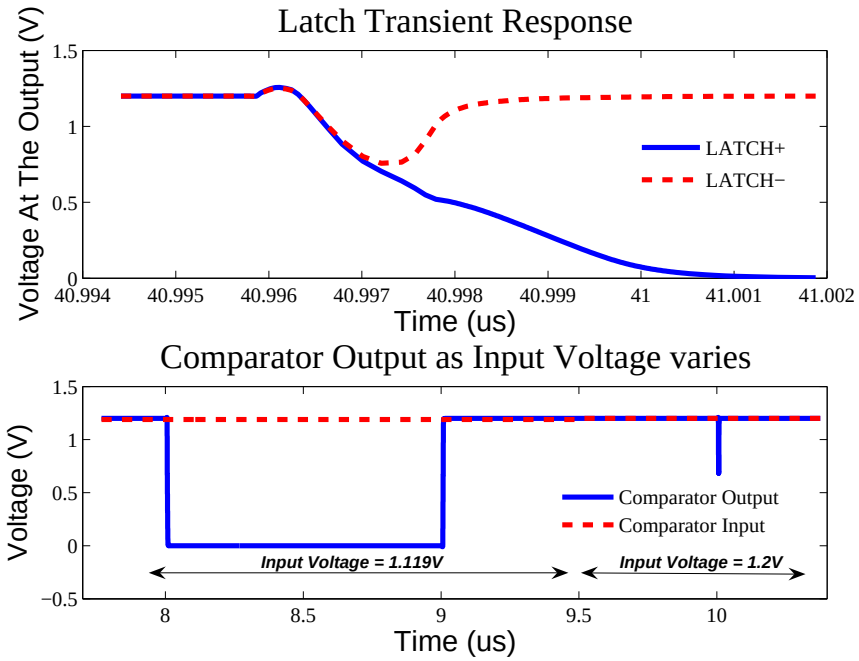


Figure 3-8: The transient response of the latch and comparator used in this ADC

generated by coarse MAINDAC. Figure 3-10 shows the capacitive DAC implemented in this ADC.

So far, we have ignored the contribution of top plate parasitic capacitance in the capacitive DACmodel, and it could give rise to a severe performance degradation of the ADC. The top plate parasitic capacitance arises from the fringing field from the capacitor array to neighboring circuit elements. In a conventional capacitive DAC design, the top plate parasitic capacitance only manifests itself as a gain error. However, when the sub-DAC is implemented, the top plate parasitic from the sub-DAC can cause linearity error [6] since the interpolated voltage levels may not fit in or may not be enough to fill the V_{LSB} from the MAINDAC. In other words, the top plate capacitance from the sub-DAC reduces the gain of the sub-DAC *within* the two voltage levels that the sub-DAC interpolates, thus creating linearity error between voltage levels. Therefore, the coupling capacitor has to be sized properly to take the forward transmission reduction from the sub-DAC into account. Figure 3-10 shows how the top plate parasitic capacitance is theoretically modelled in the capacitive

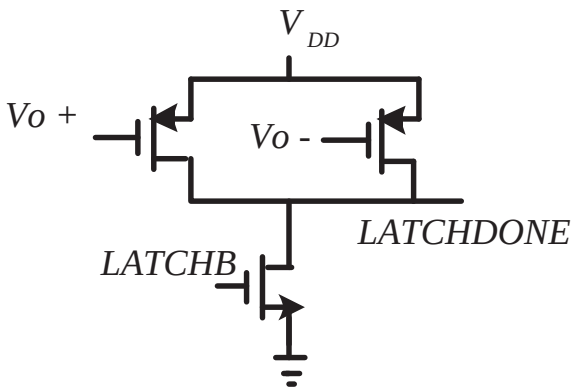


Figure 3-9: The LatchDone signal generator

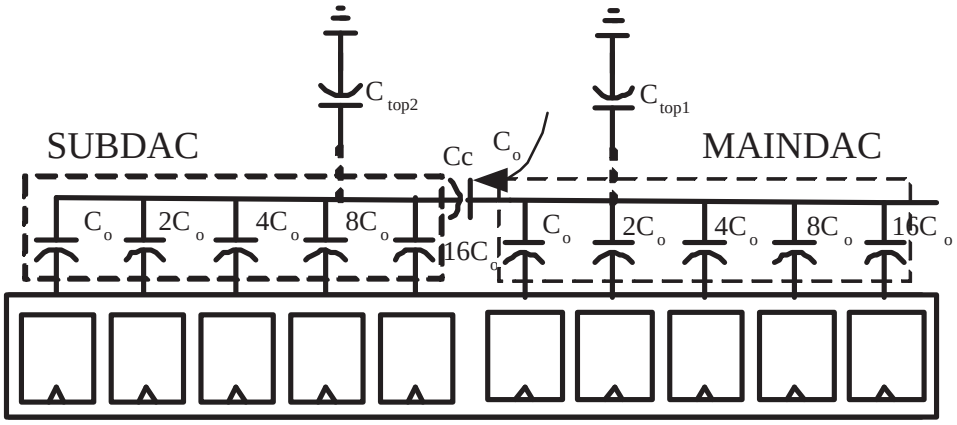


Figure 3-10: The configuration of capacitive DAC implemented for the ADC. Note the illustration of the top plate parasitics.

DAC.

As mentioned, to combat the transmission gain reduction from the sub-DAC, the value of the coupling capacitor is reduced to increase the transmission gain accordingly. A simple Thevenin equivalent model for the capacitive DAC was used to simulate the effect of the top plate parasitics, and the integral linearity error was characterized for different values of coupling capacitor in the presence of the top plate parasitics. Assuming parasitic capacitance of about C_0 (43 fF) on both the SUBDAC and MAINDAC, the value of a coupling capacitor that minimizes the INL error was determined through simulation. After a number of MATLAB simulations, C_C of 46fF was determined to be the best option.

Since the capacitor DAC is a very sensitive analog node, a metal shield is used to cover the entire capacitor array. A metal shield may increase the parasitic capacitance, but the linearity error from the additional parasitic capacitance can be taken care of by adjusting the coupling capacitor. Common-centroid layout technique [27] was used to decrease the possible mismatch of the capacitors, and dummy capacitors were also included in the array to further enhance the symmetry within the array.

An important point has to be made on the signal swing at the top plate of capacitor DAC. Since the top plate voltage can vary between 0.6V and 1.8V, the gate input to the top plate switch should be bootstrapped during bit cycling to reduce charge loss. Furthermore, the bulk of the PMOS should also be connected to a boosted potential in order to keep the diode (the connection between P-diffusion and N-well forms a diode) off all the time. The boosted potential for the bulk is generated by the charge pump and the ripple of this charge pump is minimized to prevent the coupling of charge pump signal onto the capacitor array.

3.1.4 ADC Simulation Result

In this section, simulation plots for one ADC conversion cycle will be shown. Figure 3-11 shows the propagation of control signals from one state to another. When the ADC is initialized through the global RESET signal, INIT signal will trigger to reset the state machine and the ADC controller. With the onset of ADCStart signal (which is not shown in the figure), SAMPLE operation will start. In this case, the STOP word, which determines the sampling period of the ADC, is set to 6, and it corresponds to 12μs of sampling period. Once the sampling operation is done, BCYCLE signal will be triggered. As the simulation result shows, the bit-cycle operation takes 24 μs, after which ADCDone signal is triggered. When the ADCDone signal is received by the controller, INIT signal will be set to initialize the ADC for next conversion. Note that when the sampling period is set to be 2μs, the voltage conversion takes 30μs, which corresponds to the maximum conversion rate of 33KS/s.

The power consumption of each circuit blocks were also noted from the simulation. The analog circuit blocks consume 1.4μW, and the digital blocks consume 1.1 μW at

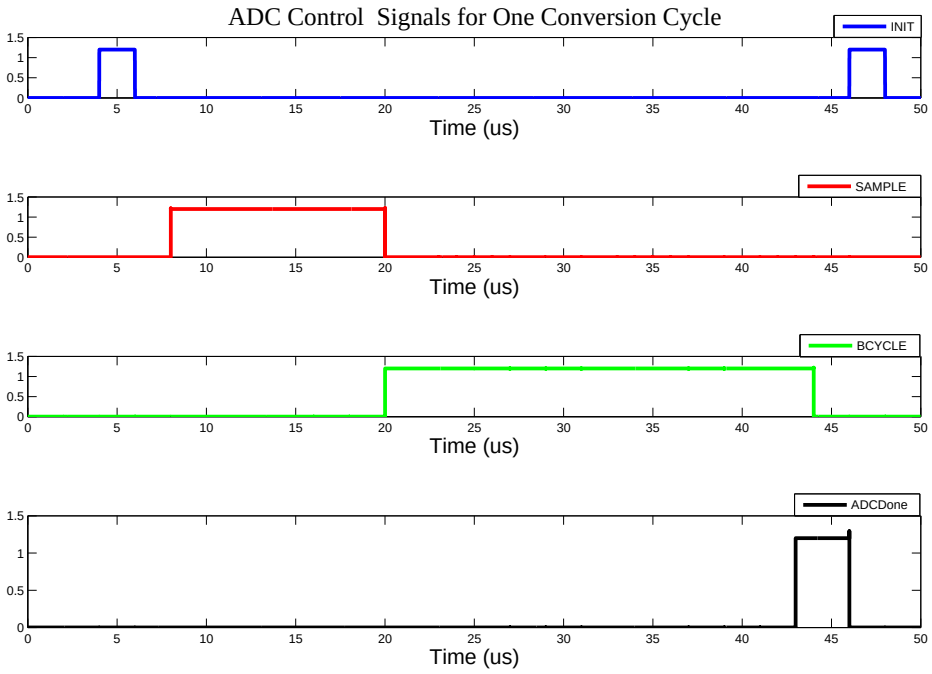


Figure 3-11: A sequence of ADC control signals during one conversion cycle

maximum conversion rate.

3.2 Current-Steering Digital-to-Analog Converter

The advantage of sourcing current to the CNTs is that the current through the CNT can be directly controlled. This is of great importance because the maximum current drive in CNT should be limited to less than 30μA; the maximum current from the DAC is 25.6μA.

3.2.1 Proposed DAC Cell and the Simulation Results

The DAC operates from a 1.2V power supply, and this results in a limited voltage headroom for each DAC cell. In many current-steering DACs, the limited voltage headroom and the finite output resistance of DAC cells leads to nonlinear characteristics. The voltage headroom concern is somewhat relieved for this application, however, because the DAC cells operate in the subthreshold regime (unit current is only 100nA). Equation 3.1 shows how the the current drive of transistors depends on V_{GS} and V_{DS} when biased in the subthreshold region.

$$I_{DS} = I_o exp(\frac{V_{GS} - V_{th}}{n\phi_{th}})(1 - exp(-\frac{V_{DS}}{\phi_{th}})) \tag{3.1}$$

where n is a subthreshold slope constant and ϕ_{th} is the thermal voltage ($\sim$26mV). Interestingly, the current depends very little on V_{DS} in subthreshold regime if the V_{DS} is greater than ϕ_{th} by approximately a factor of 4. In other words, once V_{DS} is sufficiently large, we can ensure a current value quite independent of V_{DS}.

Even though the current variation is not too large, the current accuracy plays a critical role in the attainable resistance linearity. A new DAC cell is proposed to increase the robustness.

Figure 3-12 shows the proposed DAC cells. To understand the purpose of each transistors, let's focus on the unit DAC cell. In order to increase the output resistance of the DAC cell, M_2 is added in series with M_1. M_2 also functions as a switch that performs the multiplexing. When this cell is turned off, V_b and V_c are pulled down to zero. This floats the internal node from which the leakage current from the DAC cell varies. Thus, M_3 is added to hold the internal node to a reference voltage of 0.36V

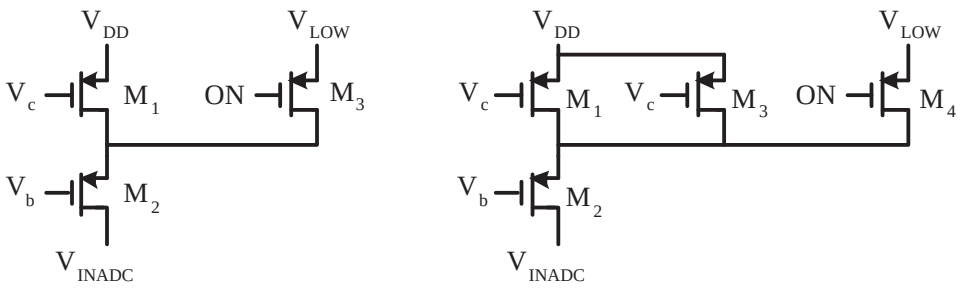


Figure 3-12: Proposed current-steering DAC cells

when the DAC cell is turned off. V_{LOW} is generated with diode-connected transistors.

Figure 3-13 shows the current supplied by the unit DAC cell as the V_{INADC} is varied. As you can see, the output current does not change until V_{INADC} becomes greater than 1V. In fact, the current changes by 89pA when V_{INADC} is swept from 0V to 0.9V. The stacked transistor may result in the degraded transient response due to larger parasitic capacitance, but it's not critical for this application.

Figure 3-13 also shows how the leakage current for a unit cell varies as V_{INADC} is swept. Note that as long as V_{INADC} is below 0.9V, the leakage current is less than 5pA. In fact, when V_{INADC} is smaller than V_{LOW}, which is generated from resistively divided transistors, the subthreshold leakage current is provided by the DAC into the output node. However, when V_{INADC} is larger than V_{LOW}, the leakage current actually enters the unit cell. Such a characteristic helps the DAC to attain small absolute difference from supposed unit DAC current value.

Added transistors increases the area of the DAC cell. In order to reduce the overhead of extra transistors in the DAC cell, a new topology of the DAC cell is introduced. Since the DAC only provides binary multiples of the minimum current, the current from the DAC will always be in the form of $(2^M)I_{LSB}$. When M is 0, $1I_{LSB}$ is generated from the unit DAC cell, and for the rest of the configurations, the double DAC cell is used.

Based on these simulation results, the maximum V_{INADC} swing is set conservatively to be 900mV. If V_{INADC} is greater than 900mV, different DAC configuration

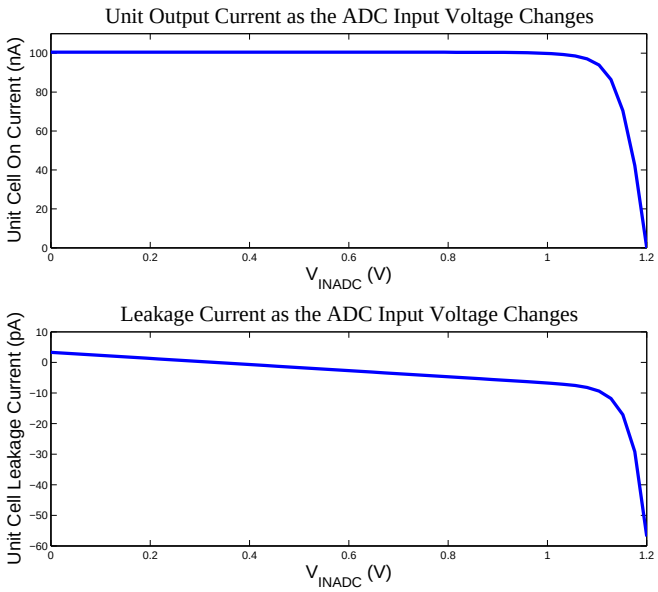


Figure 3-13: The figure shows the I_{ON} and I_{LEAK} characteristic of a Unit DAC cell as the drain voltage (V_{INADC}) varies

with smaller current is chosen for that sensor in the next sensing operation. A detailed outline of the current control scheme is introduced in Section 2.4.1.

3.3 Multiplexer for CNT sensors

3.3.1 Conventional Multiplexer Blocks

To interface the CNT sensors, the current from the DAC passes through a multiplexer. One possible candidate of a multiplexer is the tree-structured transmission gate. By organizing the transmission gates in a tree-structure, a separate decoder is not needed. The problem of having a tree-structured transmission gate multiplexer is that the on-resistance is be too large, and that the resistance is actually nonlinearly dependent on the input voltage. The maximum on-resistance of the transmission gate is more than 20KΩ, and the value varies a lot as the input voltage varies. An evident peak in resistance exists because neither NMOS nor PMOS are strongly turned on around the mid-rail. The problem of a large on-resistance is clear if we consider the fact that the current passes through 5 stages of transmission gates. In some cases, the voltage built up at the input of ADC could immediately hit the supply rail regardless of the sensor's resistance.

To attain lower on-resistance (thus proportionally less non-linearity), the width of the transmission gates should be increased. However, the width of the transistors cannot be increased indefinitely for two reasons. First of all, if the width is too wide, the large gate capacitance may require the usage of drivers to turn on and off the transistor. This causes not only the increase in energy dissipated from charging and discharging the large gate capacitance, but also to turn on and off the large drivers. Secondly, when the width of a transistor increases, the leakage current also increases proportionally. To overcome these issues, a new multiplexer cell is introduced for this interface.

3.3.2 Proposed Multiplexer Cells

Figure 3-14 shows how the multiplexer is implemented. A PMOS in the transmission gate is eliminated, and two NMOS transistors are placed in stack to reduce the leakage. A 5-bit decoder generates CNTEN signal, which turns on the multiplexer.

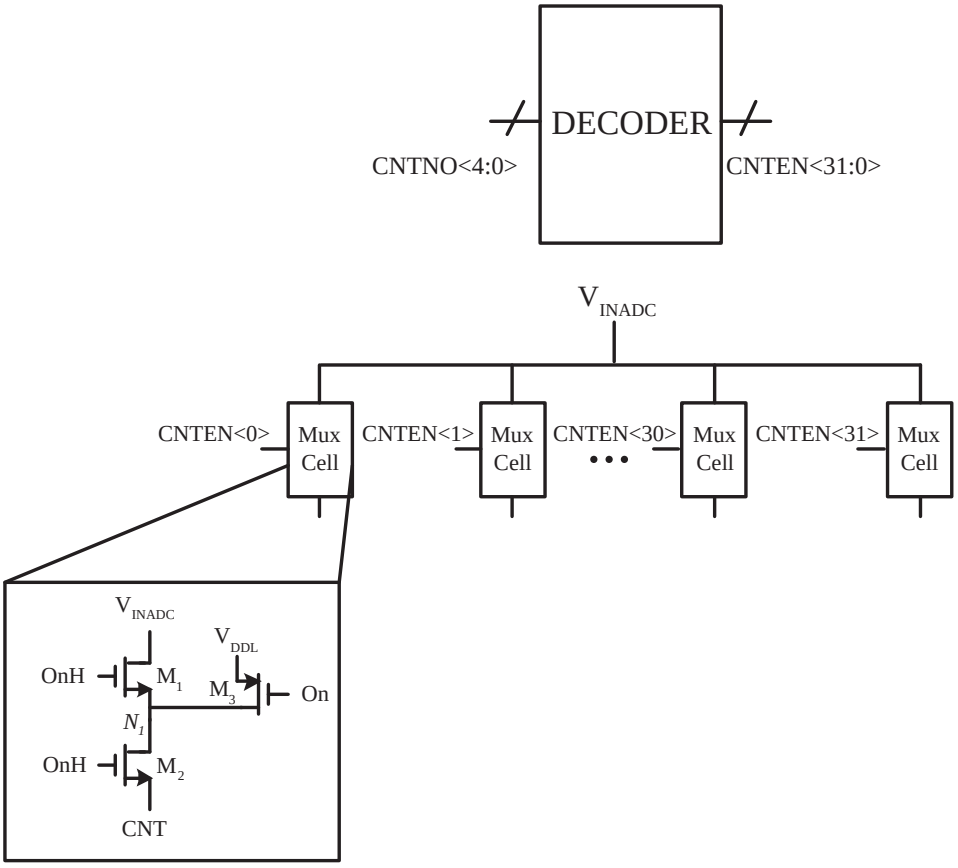


Figure 3-14: Proposed multiplexer structure to minimize the effect of resistance and leakage from the multiplexer

On signal is fed by CNTEN signal, and *OnH* is a boosted version on *On*. The boosting circuit will be explored in the next section. The leakage in the multiplexer is further reduced by introducing a negative V_{GS} for M_1 whenever the cell is turned off. V_{DDL} is at 0.5V, for which the power supply of the digital blocks is used to minimize the overhead from the voltage reference generator. This may introduce some noise feedthrough from the digital circuit, but because the transistors M_1 and M_2 are large, the intermediate node N_1 can effectively low-pass filter the noise with the parasitic capacitance.

While stacking M_1 and M_2 is beneficial for reducing the leakage current from the ADC input node to unselected sensors, it introduces extra resistance for the ON multiplexer cell. In order to reduce the resistance, the widths of M_1 and M_2 are

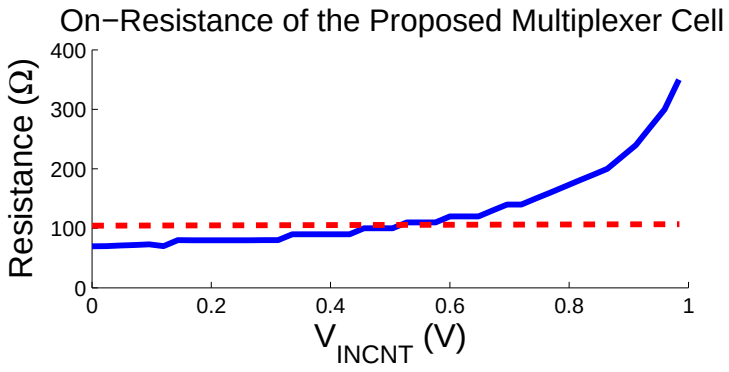


Figure 3-15: The On-resistance of the proposed multiplexer cell as the V_{INADC} is varied.

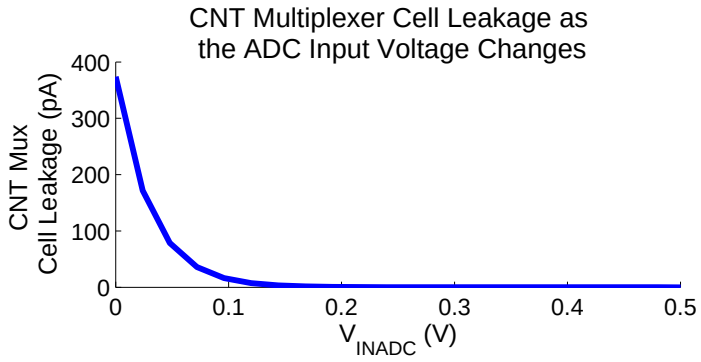


Figure 3-16: The leakage characteristic of a multiplexer cell as the V_{INADC} is varied.

sized 16.64 μm and 28.8 μm respectively. Furthermore, the NMOS transistors are gate-boosted when the mux cell is turned on to further reduce the on-resistance. The boosted gate voltage allows the NMOS to pass the voltage upto $V_{BOOSTED}$ - V_T. When the input voltage is much less than $V_{BOOSTED}$ - V_T, the resistance from the NMOS alone closely matches that of a normal transmission gate.

Figure 3-15 and Figure 3-16 show the on-resistance and leakage characteristic of the proposed multiplexer cell as V_{INADC} is varied. The gate of the proposed multiplexer cell is boostrapped to 1.7V not to overstress the gate oxide (the nominal supply voltage for this process is 1.8V).

A number of points should be stressed. First of all, the on-resistance of a mux cell is greater than 100Ω, which is our minimum resolution requirement. In fact,

the on-resistance is 70Ω when V_{INADC} is 0V, and 234 Ω when V_{INADC} is 0.9V. The difference in the on-resistance is actually more than 100 Ω and one may think this circuitry may not be able to achieve the required resolution. However, when we are sensing a nanotube with 10KΩ of resistance (at which we need to get the resolution of 100 Ω), DAC word would be 8 (25.6 μA). Thus, the corresponding V_{INADC} is 256mV, and the on-resistance of the multiplexer cell is 80 Ω, which is below the resolution requirement. Furthermore, the linearity error due to the nonlinear resistance occurs only due to the *difference* of the on-resistance at two different V_{INADC}. When we sense the change of 100 Ω in the nanotube, the voltage would change by $2\times V_{LSB}$, which is about 2.3mV. Clearly, the on-resistance of a mux cell does not change more than 10Ω with such a V_{INADC} transition. Therefore, the front-end circuitry safely meets the resolution requirement at each resistance level.

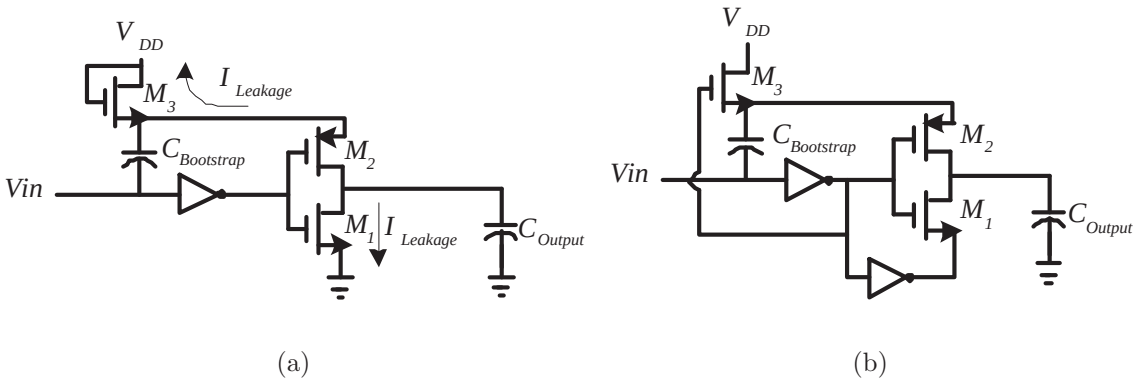
3.3.3 Low Leakage Bootstrap Circuit

Figure 3-17(a) shows the conventional bootstrap circuitry that takes advantage of a diode connected NMOS transistor M_3. When Vin is low, M_3 charges the top plate of $C_{Bootstrap}$ to $V_{DD} - V_T$. When Vin goes high, the top plate of the $C_{Bootstrap}$ goes upto $2V_{DD} - V_T$, and M_2 is turned on to deliver the boosted voltage to the output. When M_2 turns on, however, a charge-sharing phenomenon occurs between $C_{Bootstrap}$ and C_{OUTPUT}. The boosted voltage is decreased depending on the size of the output capacitance. The relationship can be expressed as

$$C_{Bootstrap} \times (2V_{DD} - V_T) = V_{FINAL} \times (C_{Bootstrap} + C_{OUTPUT}) \tag{3.2}$$

In other words, $C_{Bootstrap}$ can be adjusted according to what the desired output voltage is, and the value of C_{OUTPUT}.

The conventional boostrap circuit cannot be used for this interface because the boosted voltage has to be held for a long time (up to 1ms). The leakage paths shown in Figure 3-17(a) reduces the boosted voltage over time, as shown in Figure 3-18. The voltage droop for 1ms turn-on is 269mV in this case. The voltage droop can



(a) (b)

Figure 3-17: (a) Conventional bootstrap circuit (b) Proposed boostrap circuit to prolong the on-time of the boosted voltage.

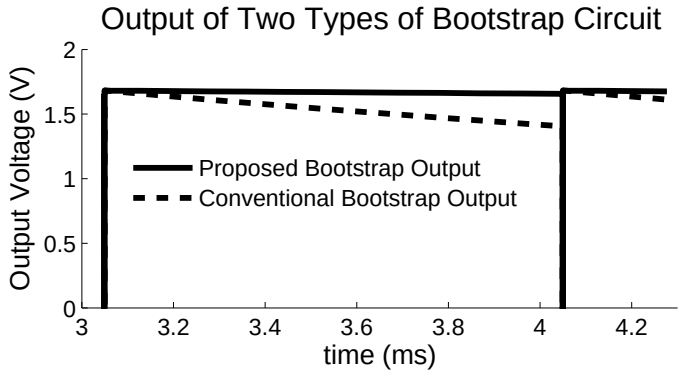


Figure 3-18: Output of two types of bootstrap circuits introduced in this section

be reduced simply by enlarging the size of $C_{Bootstrap}$, but the output voltage would actually be higher according to Equation 3.2. For the transmission gate, a droop in the boosted voltage results in the change of on-resistance as a function of time. A new leakage bootstrap circuit to mitigate these issues has been developed.

Compared to the circuit in Figure 3-17(a), the proposed bootstrap circuit (Figure 3-17(b)) uses an extra inverter. The basic operation of the proposed circuit is the same as the conventional bootstrap circuit, but the inverters actively applies a negative V_{GS} on M_1 and M_3 to reduce the subthreshold leakage. Applying negative V_{GS} reduces the voltage droop from 269mV to 18.1mV for the same turn-on period (Figure 3-18).

Chapter 4

CMOS Interface Circuitry - Measurement

The designed interface was fabricated in a $0.18\mu m$ CMOS process Figure 4-1. In this chapter, a thorough chip measurement result will be presented, and possible sources of performance degradation will be studied.

4.1 ADC Measurement

Since the dynamic performance of the ADC does not affect the performance of the system, only the static performance of ADC has been characterized. The measurement setup, and INL/DNL measurement procedures followed the protocols described in [6].

The code density test was conducted with a full-swing sinusoidal signal of 111.381Hz, at 20kS/s of sampling rate. Roughly 4 milion samples were taken to generate the code density histogram, from which the INL and DNL are calculated.

The measured offset voltage of ADC is approximately $1.1V_{LSB}$ in this ADC. Higher gain at the preamplifier stages, as well as larger input transistors at the first preamplifier stage, would have resulted in a lower offset voltage. The maximum INL of the ADC is +1.34LSB/-1.2LSB, while the maximum DNL of the ADC is +0.46LSB/-0.22LSB. Figure 4-2 shows the INL/DNL characteristic for the whole input code

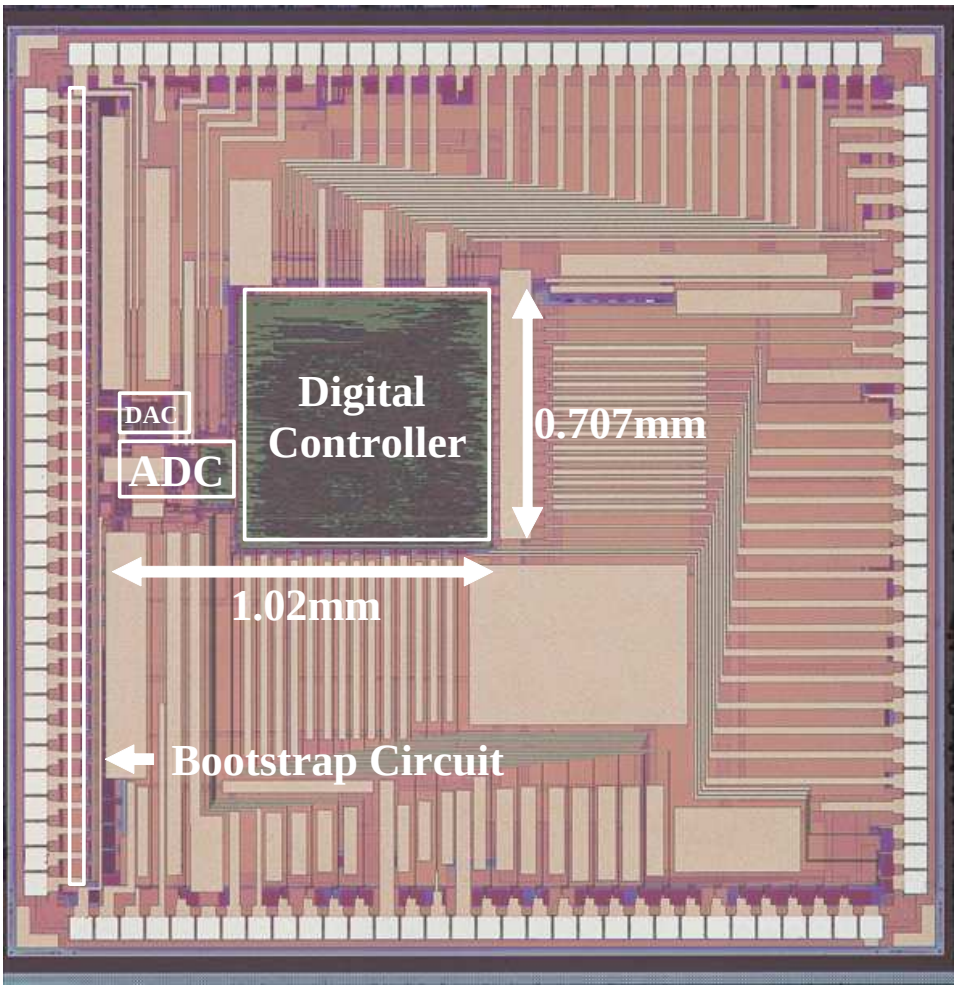
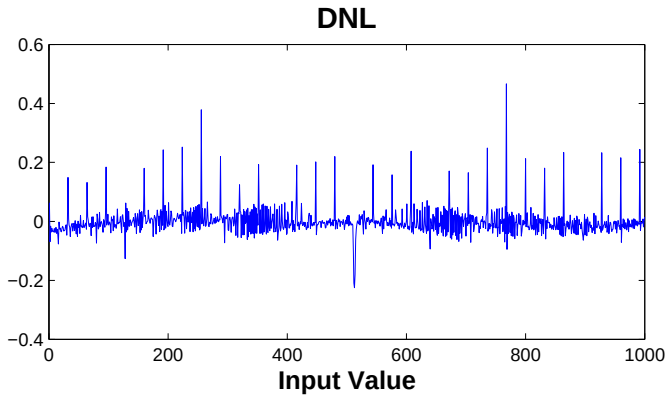


Figure 4-1: The designed interface was fabricated in a 0.18μm CMOS Process

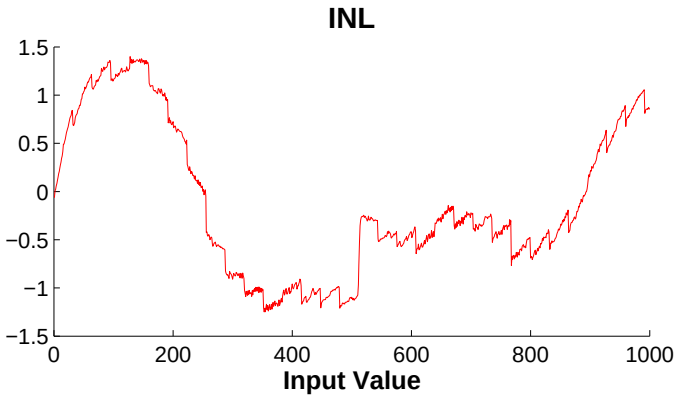
range. The saw-tooth pattern present in the INL is a manifestation of the fact that the capacitor DAC in the ADC uses the sub-DAC configuration. Note that the MSB transition causes quite a large INL error. This is due to the capacitor mismatch in the capacitor DAC. Note that the DNL is kept below 0.5LSB, thus we can safely conclude that there aren't any missing codes.

4.2 DAC Measurement

In this section, the DAC measurement result is presented. Measuring 100nA of current with high accuracy is not an easy task: the current measurement fluctuates with



(a)

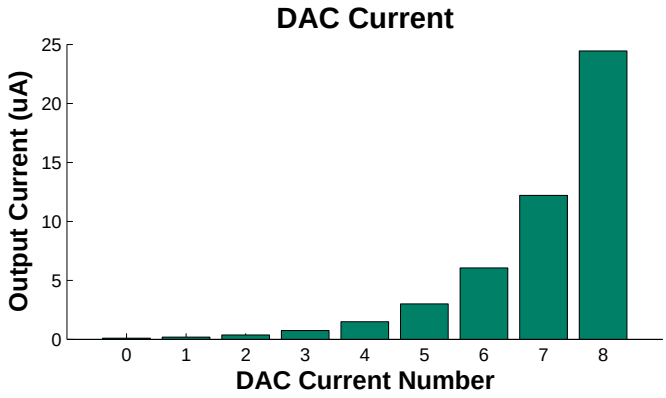


(b)

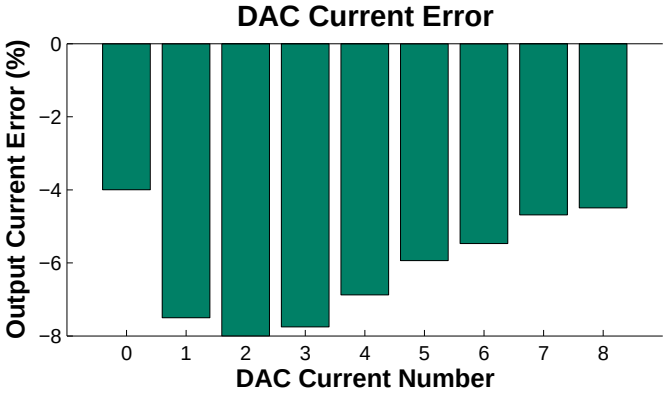
Figure 4-2: (a) Measured DNL of the 10-bit SAR ADC (b) Measured INL of the 10-bit SAR ADC

amplitude larger than the desired accuracy due to the noise in the ammeter. Thus, to measure the current accurately, the current was integrated over time, and was divided by the length of the integration time. Effectively, an average current from the DAC is calculated. The GPIB was connected to the Keithley Sourcemeter, and the PC received the current values in function of time. Figure 4-3 shows the current measurement result.

As can be seen from Figure 4-3(a), the measured current follows the 2's power of I_{LSB}. Figure 4-3(b) shows the error that results at every DAC word. Note that the error can be upto 8%, which will result in resistance error greater than 8%. This



(a)

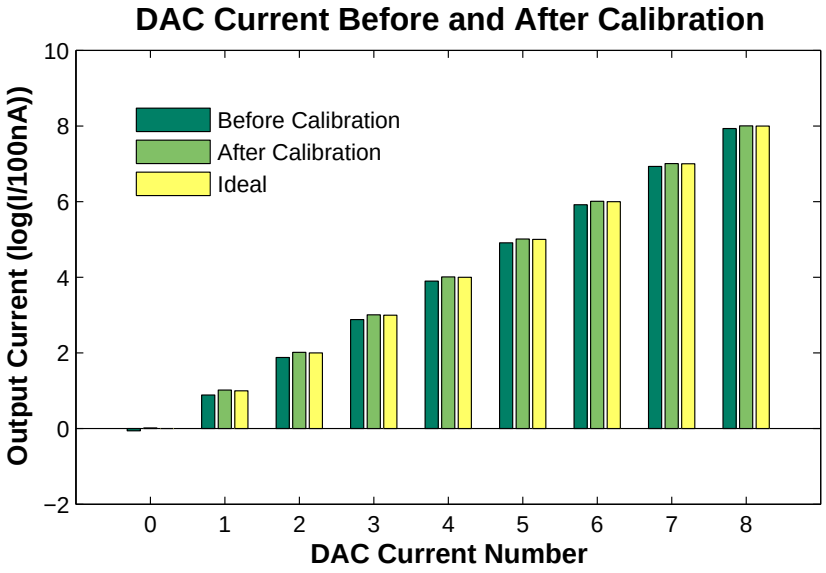


(b)

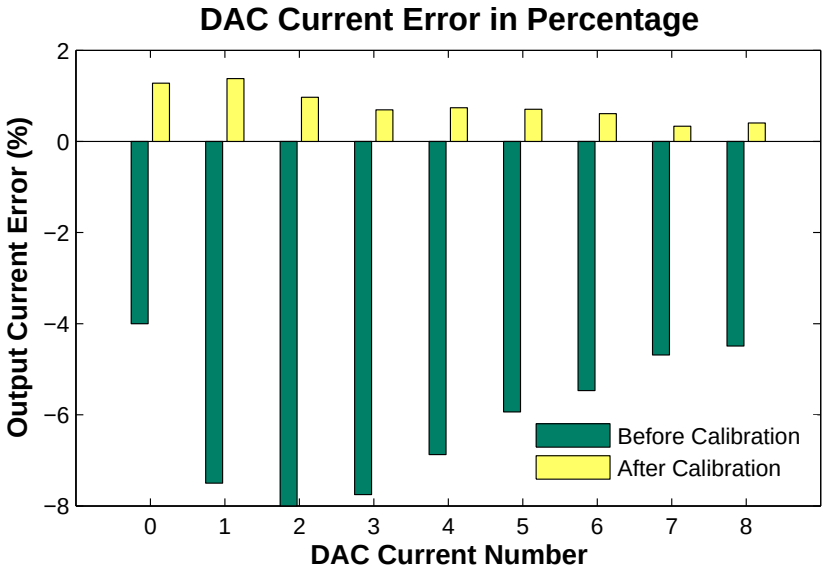
Figure 4-3: (a) Measured current (b) Current error at a given DAC word

error is to be calibrated with the implemented digital calibration scheme.

To characterize the performance of the proposed all-digital calibration, effective current before and after the calibration is compared in Figure 4-4. Note that the current error upto 8% is calibrated to lie below 1.2%. The possible sources of current error is the inaccuracy of reference resistors. The accuracy of the $R_{REFERECE}$ for DAC word 0 and 1 is worse than that of other DAC numbers (the accuracy of commercial resistors at 2-3MΩ range is worse than that of lower resistances). If the accuracy of $R_{REFERENCE}$ gets better in that regime, the interface performance will improve accordingly. Figure 4-5 shows the corresponding calibration words for this set of measurements. The DAC word wtih larger error results in a larger calibration word.



(a)



(b)

Figure 4-4: (a) Current before/after calibration, compared with the ideal current (b) Current error before/after calibration at a given DAC word

To check whether the accuracy limitation of the proposed calibration is mainly due to the reference resistors, another chip was tested. The DAC bias was kept the same as the previous chip to see the effect of chip-to-chip process variation. The

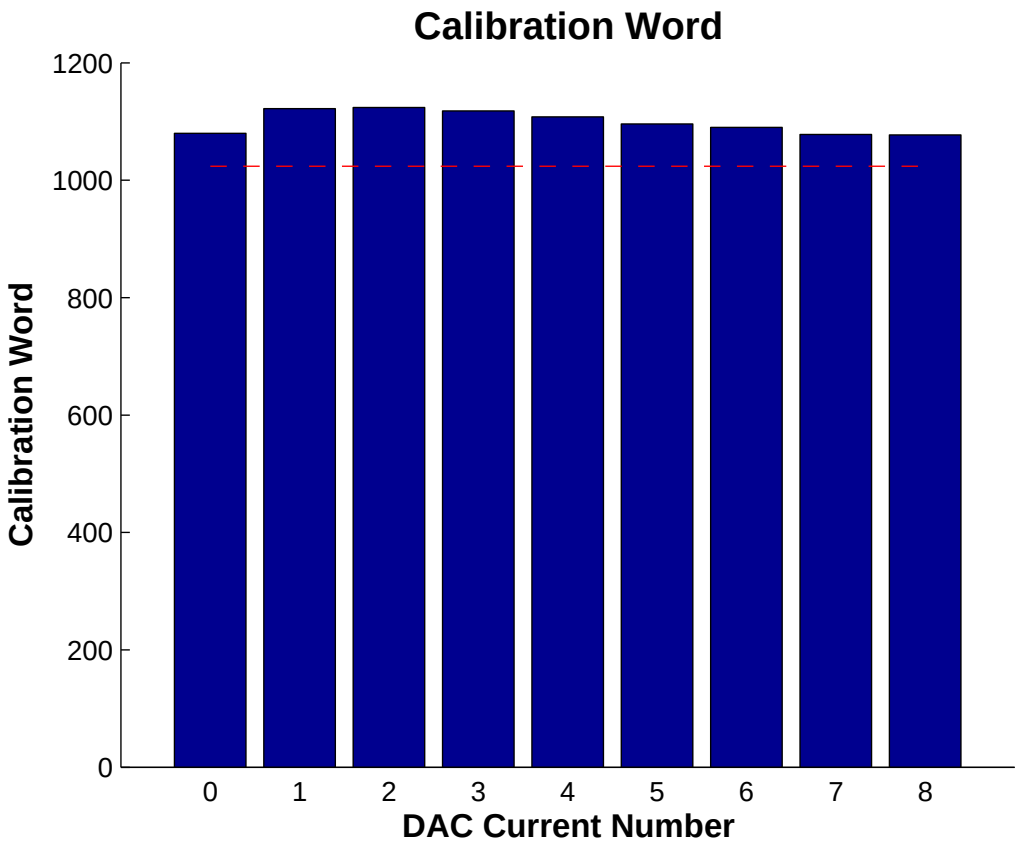
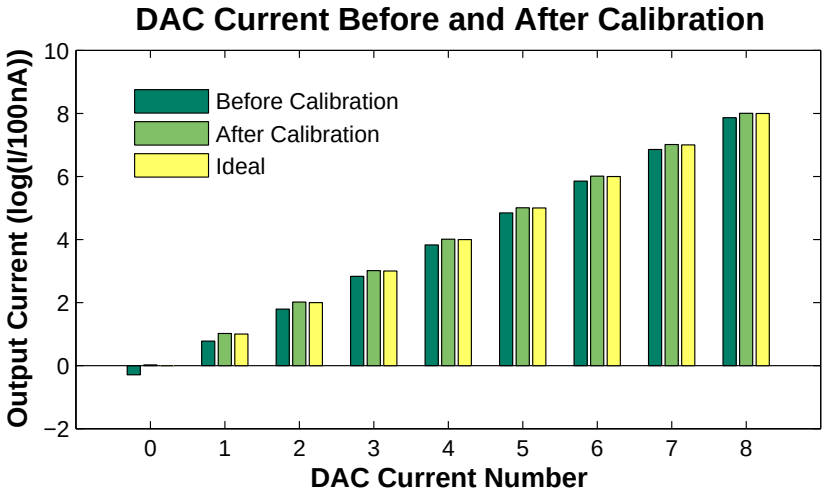


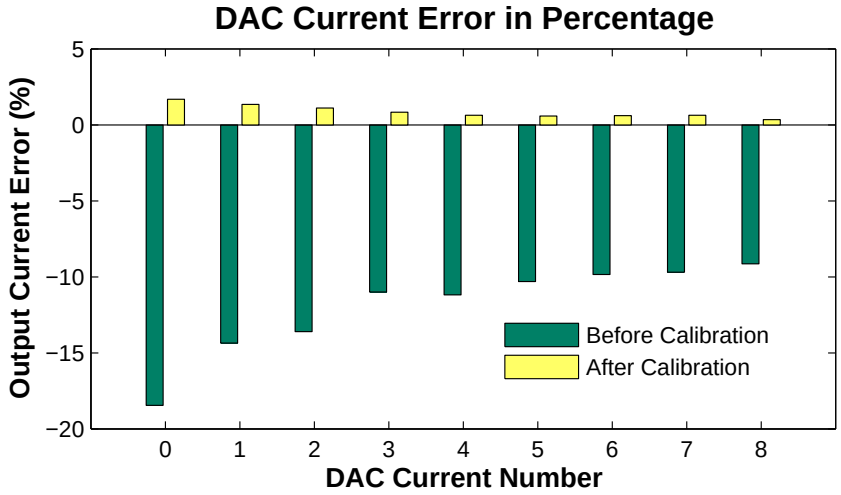
Figure 4-5: Calibration words for the given measurements. The red line denotes the unity gain points

measured current error, as well as the calibration words for the new chip is shown in Figure 4-6.

As can be seen in Figure 4-6(b), the measured current error is much greater than the previous chip. This shows that a moderate chip-to-chip variation results in a large difference in current when the transistors are biased in the subthreshold regime. After calibration, a current error up to 18 % is calibrated down to 1.2%, as can be seen in Figure 4-6(b). This shows the effectiveness of the calibration scheme. Also, the pattern of the residual error resembles the characteristic of previous chip. This confirms our conjecture that the residual error of the calibration scheme is from the inaccuracy of reference resistors. Figure 4-7 shows the corresponding calibration words.



(a)



(b)

Figure 4-6: (a) Current before/after calibration, compared with the ideal current (b) Current error before/after calibration at a given DAC word

4.3 Resistance Measurement Performance

To measure the resistance with the desired accuracy, the time needed to settle the signal at the input of ADC should be found. After a number of trials, T_{DAC} of 512μs, was found to be sufficient. Since T_{SENSE} is $T_{DAC} + T_{ADC}$, the maximum sampling rate of the interface with given T_{DAC} is 1.83kS/s. If the parasitic capacitances are

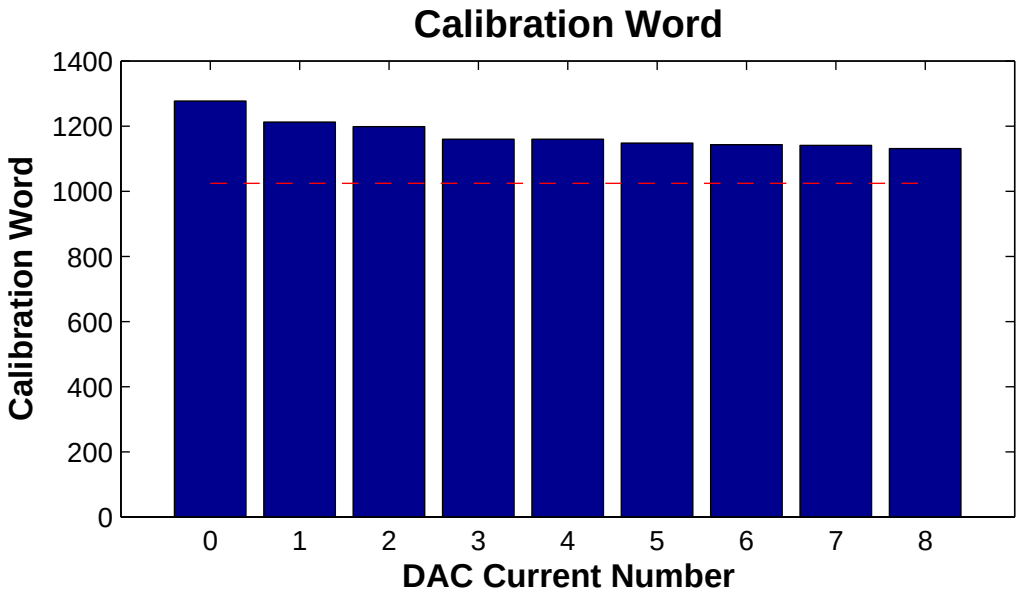


Figure 4-7: Calibration words for another set of measurements

decreased, the sampling rate can be increased acccordingly.

The measurement accuracy of this interface is shown in Figure 4-8. The saw tooth pattern of this plot is from the saw tooth pattern in the ADC linearity plot. The MSB transistion in the ADC results in sharp edges in the resistance measurement error.

Note that the maximum measurement error is kept below 1.34%. The maximum occurs when the DAC current is 200nA. This is due to the fact that the current error for 200nA DAC current is about 1.2%. Additional error is coming from both the offset voltage and the resistance quantization. As mentioned in the earlier section, the interface accuracy can be increased by using more accurate reference resistors.

4.4 Power Scaling

The designed system needs to be duty-cycled when the required sampling rate is low. This interface achieves duty-cycling through signal *OPGATING*. The sampling operation continues when *OPGATING* is high, while the sampling operation stops when *OPGATING* is low. Duty-cycling is effective in reducing the power consumption

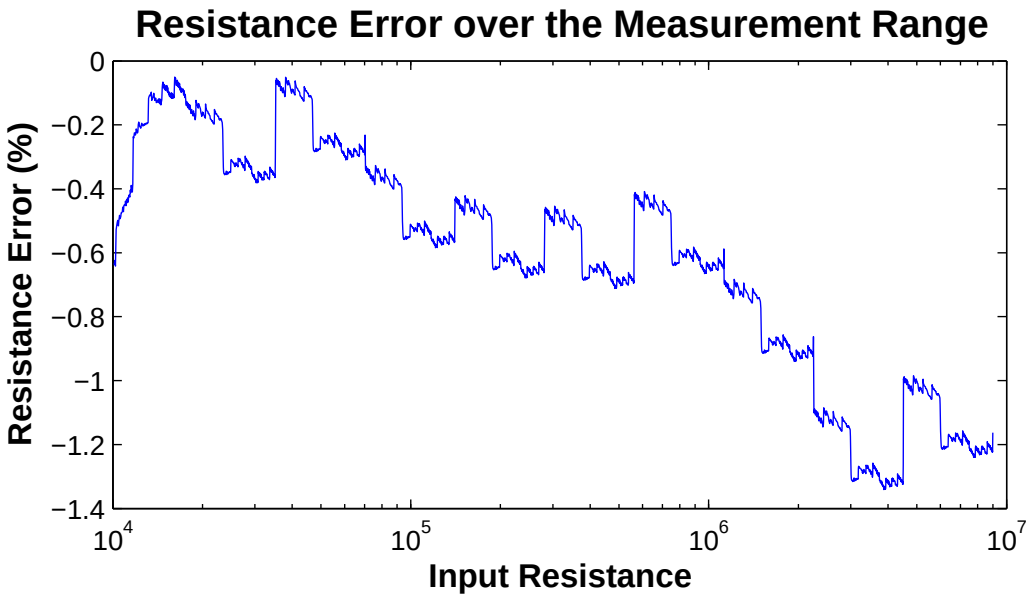


Figure 4-8: Resistance measurement error over the whole dynamic range

if the power is scalable with sampling rate. This feature is particularly useful for CNT sensors because the reaction rate of CNT sensors is very slow (in the order of 1∼2 minutes). Figure 4-9 shows that the power consumption scales linearly with the sampling rate. Note that the worst case power consumption of this interface occurs when the DAC sources $25.6\mu A$ at maximum sampling rate. This occurs when the CNT sensors in the array all have low resistances. In this case, the measured power consumption is $32\mu W$.

It's hard to compare the power efficiency of the designed interface with those already published since the dynamic range and accuracy specification in each interface differs a lot. Yet, $32\mu W$ operation allows one to use this interface, thus the CNT chemical sensor system, in sensor network applications.

4.5 Chemical Sensor System - Measurement

To verify the functionality of CNT chemical sensor system, CNT sensors were integrated at PCB-level in collaboration with Kyeong-Jae Lee. The measurement setup for the sensor system testing is shown in Figure 4-10. The CNT sensors are con-

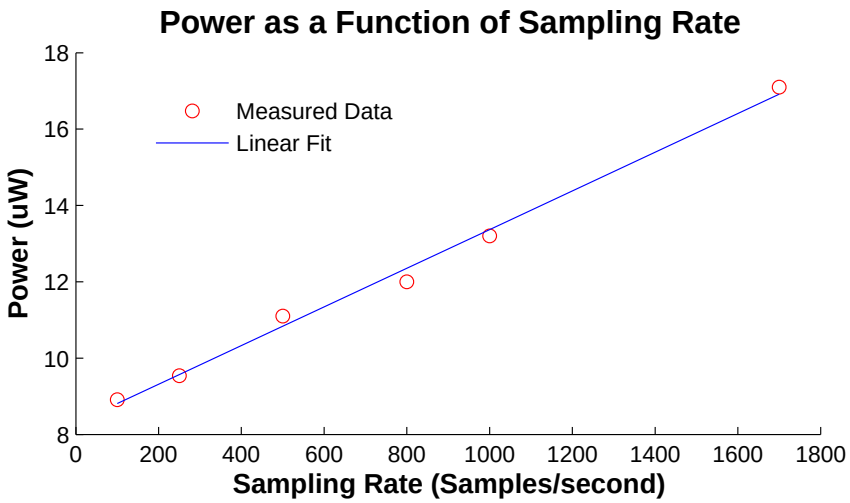


Figure 4-9: Power consumption of the interface scales linearly with the sampling rate

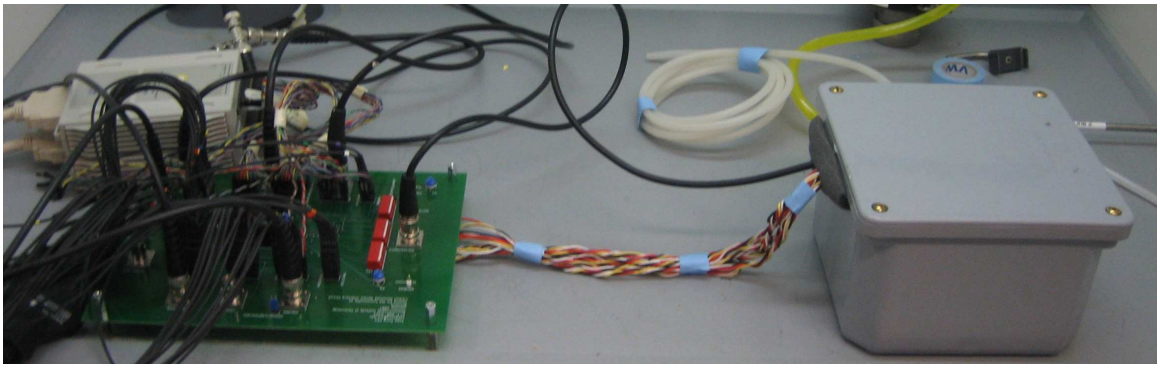


Figure 4-10: A setup to test the functionality of the chemical sensor system

nected to the interface chip through a wire, and the interface chip is connected to the logic analyzer and the pattern generator to gather the large amount of time-varying resistance data.

The CNT sensors inside the chamber is shown in Figure 4-11. As shown in Figure 4-11, the CNTs are directly exposed to a slow flow of NO_2 gas through a pipe. This is to reduce the time needed to fill up the large gas chamber with relatively small amount of gas.

When CNT chemical sensors were exposed to various concentrations of NO_2, we could see that the measured resistance changes accordingly. Figure 4-12 shows the output of the sensor system. This figure shows that the real-time monitoring of

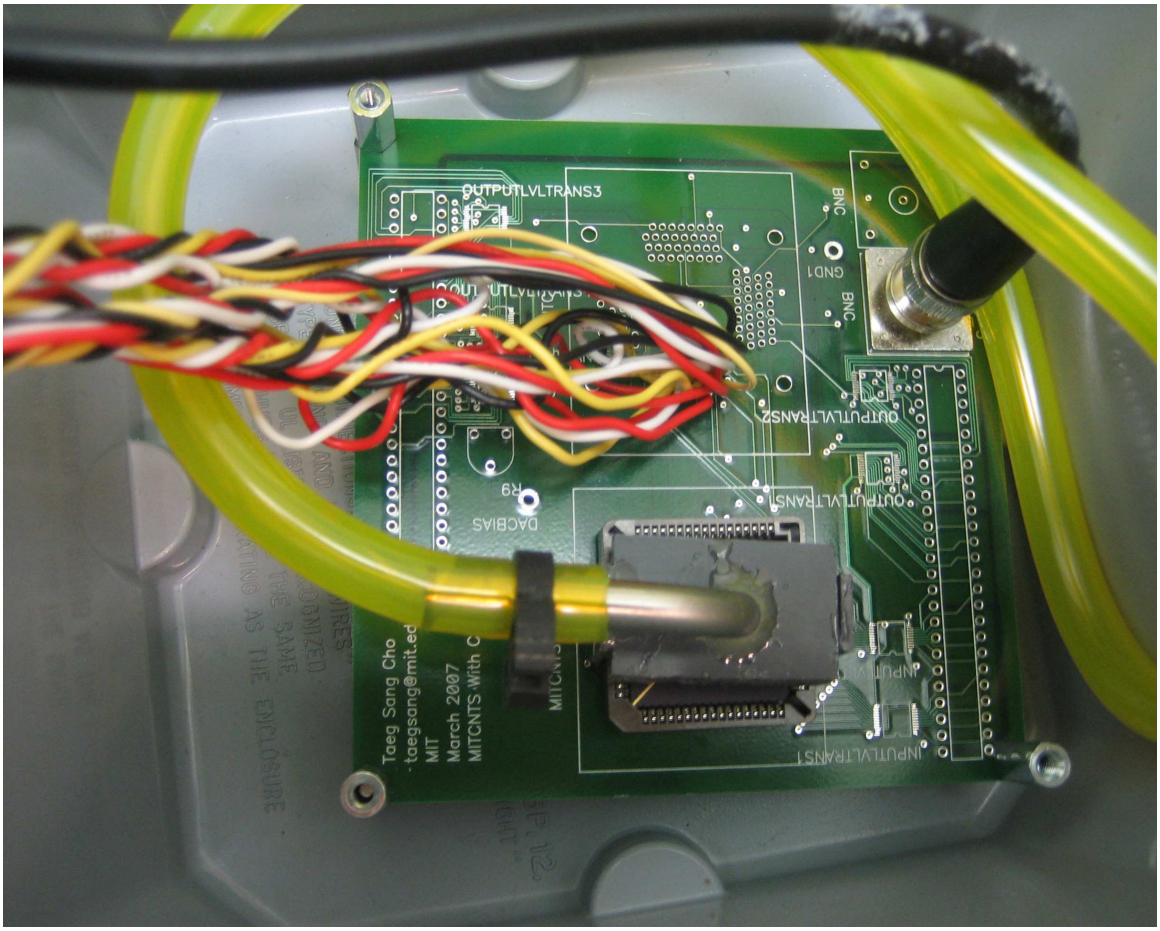


Figure 4-11: CNT sensors are exposed to the chemical through a gas pipe

chemicals is feasible with the system setup. Note that the full system testing was carried out at room temperature.

The variability of the CNT response is evident from the plot. Some sensors exhibit better sensitivity than others. This justfies our use of 24 CNT sensors in this system. If it's possible to package a dense array of CNTs and CMOS chip, the system can gain more reliability. Although the chemical concentration cannot be read off directly from the transient response shown in Figure 4-12, an extensive literature exists to infer the chemical concentration given the response of various sensors [30]. Another way to improve the performance of the system is to investigate the CNT sensors to enhance the reliability. At the time of this writing, many researchers are investigating on how to coat CNTs to improve the selectivity and stability of the CNT sensors [31].

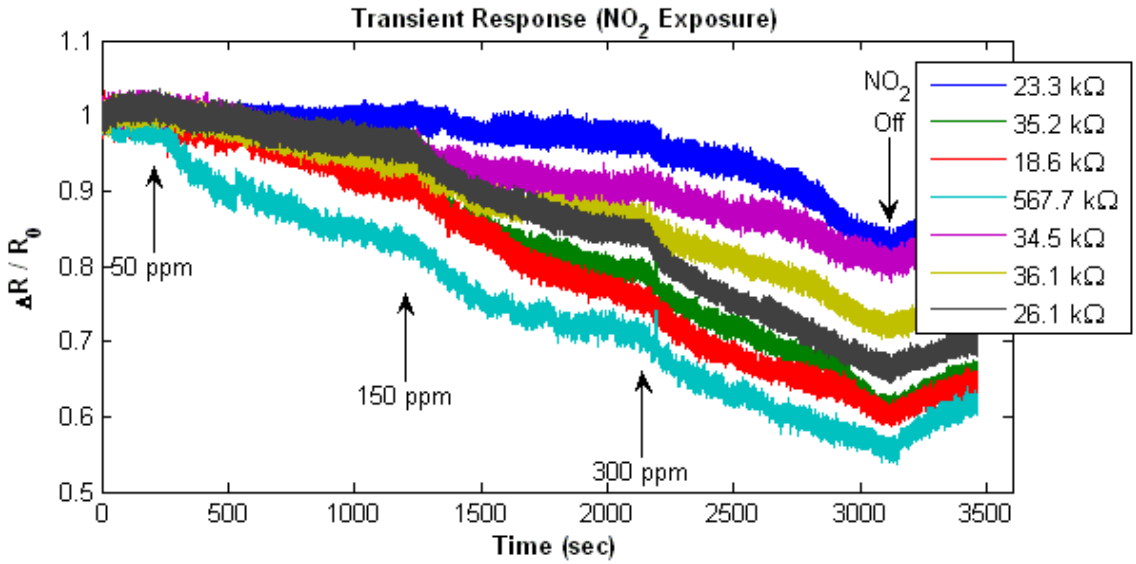


Figure 4-12: The resistance of CNTs changes when exposed to different concentrations of NO_2

Chapter 5

Conclusion

This thesis brings together one of the first demonstrations to bring the carbon nanotubes and CMOS technology together. The main contribution of this thesis is the design of energy efficient CMOS interface to CNT sensor arrays. Although CNTs have shown the potentials to become a mainstream technology, assists from the system structure is needed to fully exploit the benefits of using CNTs due to poor process reliabilities. In the chemical sensor application, a large spread of base resistance in CNTs pose the greatest challenge to the system. This challenge is made harder by the stringent power budget on sensor network applications. Thus, several innovations have been made to design a stable hybrid CNT-CMOS system, and the proposed techniques were verified with a prototype CMOS chip. Several contributions, and possible improvements, are delineated below.

This thesis proposed an OPAMP-less structure to enable an ultra-low power operation by adaptively controlling the actuation of the sensors. The architecture is also sampling-rate scalable, and by duty-cycling the system, a linear power scaling is achieved. This resulted in the worst-case power consumption of $32\mu W$ at 1.7kS/s, a two orders of magnitude power reduction at higher sampling rate and lower accuracy compared with the state-of-the-art sensor interface circuits ([4] and [5].) The majority of the power is consumed from the DAC, and it can be reduced by integrating CNT sensors on-chip to reduce the parasitic capacitance at the signal node.

To adaptively control the DAC current, DAC control can be elaborate, which is

not suitable for low power applications. This thesis proposed a simple DAC control scheme by posing two contraints: DAC can only provide binary multiples of I_{LSB}; DAC current should be maximized while meeting the DAC headroom constraint. This scheme considerably decreased the complexity of the DAC control, enabling a low area overhead and low power consumption.

This chip implements a 10-bit ADC to measure the voltage that's generated by the current source and CNT sensors. The performance of SAR analog-to-digital converter is quite poor compared with state-of-the-art 10-bit analog-to-digital converters, both in terms of energy consumption and accuracy. In most SAR ADC's, as long as the matching of capacitor DAC is under control, a good static linearity performance can be attained. Better matching can be attained from larger unit capacitors and careful layout. As can be seen from the INL plot, the linearity of the ADC could be improved by more than 1LSB, and this will lead to a better performance of the DAC calibration block.

This thesis proposed a number of calibration techniques to overcome process variations and possible performance degradations. The employed techniques increased the accuracy of the measurement by more than 7 times (over 8% measurement error is calibrated down to 1.34% error.) at the expense of off-chip reference resistors. The residual error after the calibration schemes resulted mostly from the mismatches in the reference resistors, as is evident from Chapter 4. Although highly accurate resistors are available off-the-shelf, these resistors tend to be pricy and also adds to the bulkiness of the built system. Furthermore, the accuracy of off-the-shelf resistors in the resistance range of interest may not be good enough to achieve the desired measurement accuracy, as was discussed in the measurement section. Since the purpose of the interface is to measure the *absolute* resistance value, the need for an accurate analog reference is evident. However, if other means to generate the analog reference is available on-chip, the interface circuitry will be more effective.

Appendix A

Proposed Architecture Optimization

In this chapter, the architecture optimization mentioned in Section 2.3.2 is performed. The objective of this optimization is to determine the number of bits to allocate to the ADC and DAC that would result in the optimal energy performance. The energy consumed by the system is given by the following equation.

$$E_{SYSTEM} = P_{ADC} \times T_{ADC} + P_{DAC} \times T_{DAC} + E_{DIGITAL} \tag{A.1}$$

Detailed modeling of each component is studied in this chapter.

A.1 T_{DAC} Model

In order to determine T_{DAC}, an accurate model for the capacitance at the input of the ADC should be developed. In a conventional SAR ADC using a capacitive DAC, the number of capacitors in the DAC increases exponentially as the resolution of the ADC increases. This stems from the binary search nature of the SAR ADC. However, the input capacitance can be reduced drastically if the notion of sub-DAC is applied to the capacitive DAC [6], as shown in Figure A-1. When the resolution of a SAR ADC is N-bit, then the input capacitance with a sub-DAC implementation is roughly

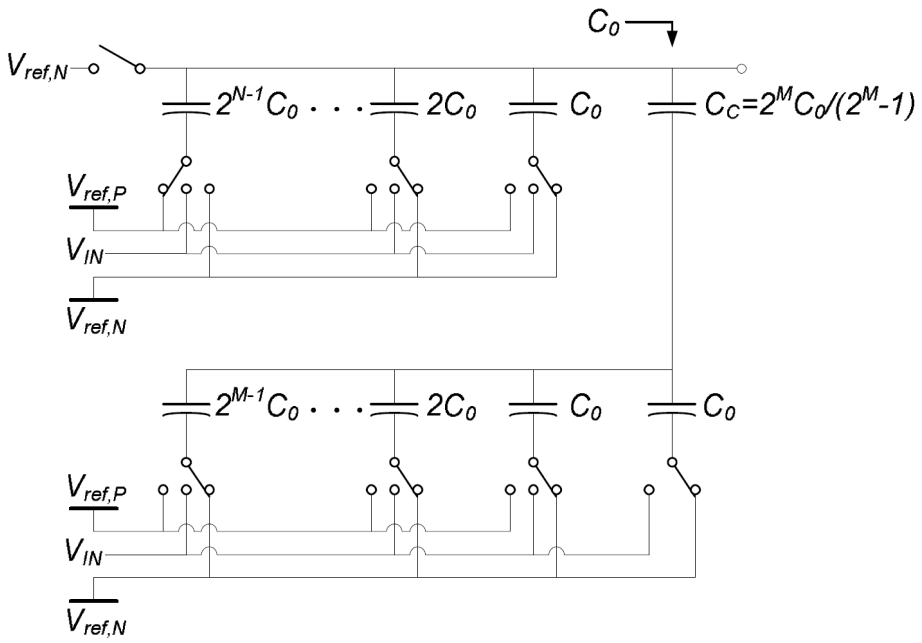


Figure A-1: The concept of sub-DAC implementation [6]

$2\times 2^{\frac{N}{2}}\times C_{unit}$, whereas in a conventional SAR ADC, the input capacitance is $2^N\times C_{unit}$. To get a rough estimate of the input capacitance in each scenario, when C_{unit} is 50fF, a sub-DAC equipped 12-bit SAR ADC will have $2\times 2^6\times 50fF = 6.4pF$ of input capacitance, whereas a conventional 12-bit ADC will have $2^{12}\times 50fF = 204.8pF$ of input capacitance. In the model to be developed, a sub-DAC equipped SAR ADC is assumed.

As the ADC resolution increases, not only the number of capacitors in the capacitive DAC increases, but also the value of C_{unit} itself due to the capacitor matching requirement from the higher resolution. The capacitor matching error is proportional to the square-root of the capacitance value [32]; from the previous art [6], 100 fF has been proven adequate to achieve 12-bit resolution DAC in the $0.18\mu m$ CMOS process. However, scaling this value down for 10-bits or lower resolution ADC's makes the C_{unit} too small to be practical. Therefore, C_{unit} value will be extrapolated for all other resolution SAR ADC's based on the C_{unit} value in two ADC's. In [33], 12fF C_{unit} is used in an 8-bit resolution SAR ADC. Thus, we can safely assume that a 40 fF of C_{unit} can effectively meet the matching error requirement for 9-bit SAR

ADC. From these values, C_{unit} for each ADC resolution can be extrapolated with the following relations.

$$C_{unit-9bit} = 40 \times 10^{-15} = (a \times 2^{2\times 9} + b) \times 10^{-15} \tag{A.2}$$

$$C_{unit-12bit} = 100 \times 10^{-15} = (a \times 2^{2\times 12} + b) \times 10^{-15} \tag{A.3}$$

Solving the two equations, the C_{unit} for an N-bit ADC becomes

$$C_{unit-Nbit} = (3.633 \times 10^{-6} \times 2^{2N} + 39.0476)fF \tag{A.4}$$

This model will be used to calculate the input capacitance of the N-bit SAR ADC.

Apart from the capacitance looking into the ADC, the parasitic capacitance resulting from the DAC, MUX devices and the off-chip wiring has to be included in the model. From the multiplexor layout and the off-chip board parameters, $C_{parasitics}$ is estimated to be about 3pF. Thus, 3pF will be added to the ADC input capacitance to calculate the RC time constant at the ADC input node.

$$C_{INPUT} = C_{ADC} + 3pF \tag{A.5}$$

To a first order approximation, the voltage at the input of the ADC will follow an exponentially tapering waveform, with the time constant $\tau = R_{CNT}C_{input}$. Thus,

$$V_{IN}(t) = V_{FINAL}(1 - exp(\frac{-t}{\tau})) \tag{A.6}$$

In order for the interface to operate properly, the voltage at the input node should settle within V_{LSB} from the V_{FINAL} value before ADC samples it. If the resolution of the ADC is N bits, Equation A.6 can be used to derive the following relationship.

$$V_{FINAL} - V_{IN}(t) = V_{FINAL}exp(\frac{-t}{\tau}) \leq V_{DD}exp(\frac{-t}{\tau}) < V_{LSB} = \frac{V_{DD}}{2^N} \tag{A.7}$$

From Equation A.7, it can easily be seen that

$$T_{SETTLE} > -R_{CNT}C_{INPUT}\ln(2^{-N}) \tag{A.8}$$

The maximum value of R_{CNT} in this application is 9 MΩ, thus the time required to operate the DAC is

$$T_{DAC} = -9M\Omega \times C_{INPUT}\ln(2^{-N}) \tag{A.9}$$

A.2 P_{DAC} Model

As mentioned, the interface aims at attaining 18 bits of dynamic range. Thus, if N bit dynamic range is allocated in the ADC, 18 - N bit will be allocated in the DAC. Since the I_{LSB} is 100nA, P_{DAC} is given by

$$P_{DAC} = 100nA \times 2^{(18-N)} \times 1.2V \tag{A.10}$$

where 1.2V is the supply voltage.

A.3 T_{ADC} Model

A relatively simple model is used for T_{ADC}. Since the SAR ADC performs a binary search algorithm, it takes N cycles to resolve the digital words in an N-bit ADC. Thus, T_{ADC} is simply

$$T_{ADC} = N \times T_{CLK} \tag{A.11}$$

where T_{CLK} is 2μs in our system.

A.4 P_{ADC} Model

From the definition of Figure of Merit (FOM) for ADCs, modeling P_{ADC} is straight forward.

$$P_{ADC} = 2 \times f_{IN} \times 2^N \times FOM \tag{A.12}$$

Assuming that the ADC targets 20kS/s operation of the ADC, and FOM is about 250fJ per conversion step,

$$P_{ADC} = 5 \times 10^{-9} \times 2^{N} \tag{A.13}$$

Appendix B

The Effect of ADC Error on the Proposed DAC Calibration Scheme

Any nonlinearity in the ADC will result in the nonlinearity of the resistance measurement system. To characterize how the offset and gain error effect the system performance, let's consider the effectiveness of the DAC calibration scheme in the presence of ADC offset and gain error. As mentioned above, $V_{OUTADC} = G \times V_{INADC} + V_{OFFSET}$ when ADC has a gain and offset error, where G is the gain factor. Therefore,

$$Cal_N = \frac{V_{REFERENCE-CAL}}{G \times V_{MEASURED-CAL} + V_{OFFSET}} \neq \frac{V_{REFERENCE-CAL}}{V_{MEASURED-CAL}} \tag{B.1}$$

where $V_{REFERENCE-CAL}$ is the precalculated voltage that ideal DAC current will induce on the reference resistor, and $V_{MEASURED-CAL}$ is the actual induced voltage from the reference resistor before being sampled by the ADC in the DAC calibration phase. If we calculate the output resistance with the given Cal_N in the presence of gain and offset error,

$$\begin{aligned} &\frac{G \times V_{INCNT} + V_{OFFSET}}{I_{IDEAL}} \times \frac{V_{REFERENCE-CAL}}{G \times V_{MEASURED-CAL} + V_{OFFSET}} \\ &\neq R_{CNT} = \frac{V_{INCNT}}{I_{IDEAL}} \times \frac{V_{REFERENCE-CAL}}{V_{MEASURED-CAL}} \end{aligned} \tag{B.2}$$

where V_{INCNT} is the voltage induced by the CNT at the input of the ADC. The problem with the DAC calibration scheme is obvious from Equation B.2 since the offset voltage appears in the denominator of Equation B.2. It's also evident that once V_{OFFSET} is subtracted from both the denominator and numerator in Equation B.2,

$$\frac{G \times V_{INCNT}}{I_{IDEAL}} \times \frac{V_{REFERENCE-CAL}}{G \times V_{MEASURED-CAL}} = R_{CNT} = \frac{V_{INCNT}}{I_{IDEAL}} \times \frac{V_{REFERENCE-CAL}}{V_{MEASURED-CAL}} \tag{B.3}$$

Therefore, once V_{OFFSET} is accurately estimated, DAC calibration scheme will not be effected by the ADC offset and gain error.

Offset Voltage Estimation Scheme

In the presence of offset and gain error in the ADC, the transfer characteristic of the ADC can be modeled as $V_{OUTADC} = G \times V_{INADC} + V_{OFFSET}$. It is thus clear from elementary linear algebra that once V_{OUTPUT} and $G \times V_{INADC}$ is known, V_{OFFSET} can be estimated. In order to do so, we reuse the valuable resource from the DAC calibration scheme: highly accurate resistors. Note that the voltage from R_{TEST1} is given by Equation B.4.

$$V_{O,MEASURED1} = G \times (I_{DAC} R_{TEST1}) + V_{OFFSET} \tag{B.4}$$

There are four unknowns in this equation: $V_{O,MEASURED1}, G, I_{DAC}, V_{OFFSET}$. Interestingly, by measuring the output voltage from two different reference resistors with the same DAC current, we can calculate the V_{OFFSET}. Let $V_{O,MEASURED2}$ be the voltage from R_{TEST2}.

$$V_{O,MEASURED2} = G \times (I_{DAC} R_{TEST2}) + V_{OFFSET} \tag{B.5}$$

Therefore,

$$\frac{R_{TEST2}}{R_{TEST1}} = \frac{V_{O,MEASURED2} - V_{OFFSET}}{V_{O,MEASURED1} - V_{OFFSET}} \tag{B.6}$$

By rearranging Equation B.6,

$$V_{OFFSET} = \frac{\frac{R_{TEST2}}{R_{TEST1}} \times V_{O,MEASURED1} - V_{O,MEASURED2}}{\frac{R_{TEST2}}{R_{TEST1}} - 1} \tag{B.7}$$

For the DAC calibration purposes, $\frac{R_{TEST2}}{R_{TEST1}}$ is 2 for several combination of resistors, so Equation B.7 is simplified a lot. Furthermore, by carrying out Equation B.7 operation with a number of resistors at different DAC current settings and taking the average of all operations, we can minimize the random error that might result from a single measurement. After the V_{OFFSET} extraction, we can subtract the V_{OFFSET} value from the CAL_N equation as in Equation B.3 to accurately calculate the nanotube resistance. Interestingly, the gain error in the ADC does not result in any error in the resistance measurement. As seen in Equation B.3, the gain error factor is automatically cancelled by the gain error factor in CAL_N. Therefore, a separate scheme to calibrate the gain error is not needed.

No special system-level calibration scheme is used to combat the measurement error that stems from the nonlinearity of the ADC. Some circuit techniques will be looked into in order to minimize the ADC linearity error.

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