A Low Power Carbon Nanotube Chemical Sensor System

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***Abstract*— This paper presents an energy efficient chemical sensor system that uses carbon nanotubes (CNT) as the sensor. The room-temperature operation of CNT sensors eliminates the need for micro hot-plate arrays, which enables the low energy operation of the system. The sensor interface chip is designed in a 0.18 μm CMOS process and consumes, at maximum, 32 μW at 1.83 kS/s conversion rate. The designed interface achieves 1.34% measurement accuracy over 10 kΩ - 9 MΩ dynamic range. The functionality of the full system, including CNT sensors, has been successfully demonstrated.**

I. Introduction

Chemical gas detection is used in monitoring environmental and industrial processes. With the emergence of nanotechnology, new reliable sensing materials have been developed. Thus, a low-cost and energy-efficient sensor interface circuit could enable an expendable chemical sensor system. This paper investigates the design of an ultra-low power chemical sensor system using carbon nanotubes (CNTs) as the sensing medium targeting at sensor network applications.

II. Carbon Nanotube Chemical Sensors

Since the initial work of CNT sensors [1], research groups have investigated the use of CNTs as chemical and biological sensors. CNTs can be highly sensitive even at room temperature unlike other sensing technologies. This feature renders a micro-hotplate unnecessary, making CNTs particularly attractive for low-power applications. CNTs also have nanometer range diameters and all the atoms exposed on the surface. This allows miniaturization and means for chemical coating to achieve high selectivity to specific chemical agents. However, current fabrication methods generally yield CNTs with large resistance variations. Furthermore, CNT sensors exhibit fast response but slow recovery time to gases. While active heat or UV treatment can accelerate the long recovery time, such schemes are not implemented to maintain low power.

In this study, an array of 24 single-walled CNT FETs is fabricated. The resistance change is monitored as the sensors are exposed to NO_2. NO_2 detection is important for monitoring automotive emissions. CNTs are grown via chemical vapor deposition, using an Fe/Mo-based catalyst and a CH_4 source at 900^{o}C. The catalyst is deposited at pre-patterned sites. The inset of Fig. 1 shows the distribution of resistance for CNTs (4 μm channel, Cr/Au contacts), exhibiting the spread from 10 kΩ to 9 MΩ. This distribution results from one of the most critical and challenging aspects of CNT fabrication: the number of CNTs between the electrodes of each device can vary and can be either metallic or semi-conducting, where semi-conducting CNT FETs have a diameter-dependent band gap.

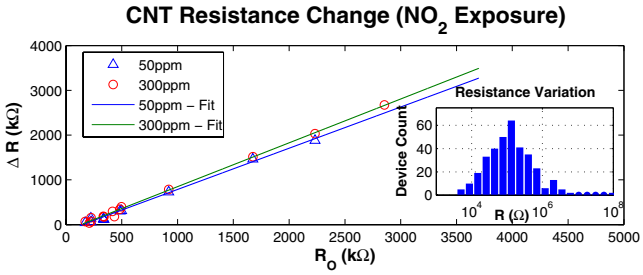


Fig. 1. Experimental data on the linear dependence on ΔR-R_0. inset: Measured data on the distribution of CNT resistance. (Measurement from ~350 devices.)

The CNT array is used as grown without any additional treatment. While the large dynamic range poses circuit challenges, using an array of sensors as opposed to single devices can effectively increase the reliability of gas detection and identification. Fig. 1 shows the linear relation between the resistance change and the initial baseline resistance. This linearity can be parameterized for gas concentration inference. Further details of the CNT sensor array can be found in [2].

To interface to the CNT sensor array, the front-end circuit needs to address a wide resistance range of 10 kΩ - 9 MΩ. In addition, the CNT resistance should be measured with a precision near 2% to detect NO_2 in the sub-ppm range, which results in a 16-bit dynamic range (R_{LSB}=182 Ω).

III. CMOS Interface Architecture

A number of resistive sensor interface architectures have been introduced in literature using an OP-AMP to widen the dynamic range [3] or enhance the accuracy of the measurement [4]. Since high gain is necessary in the OP-AMP, the power consumption of these interfaces is not suited for ultra-low power applications. This paper introduces an architecture that is low-power, power scalable, and high-speed compared with the state-of-the-art sensor interfaces.

A. Architecture

Fig. 2 shows the architecture proposed. The basic idea is to source predetermined current to the CNT sensors, and read the voltage developed across the sensors. This architecture is

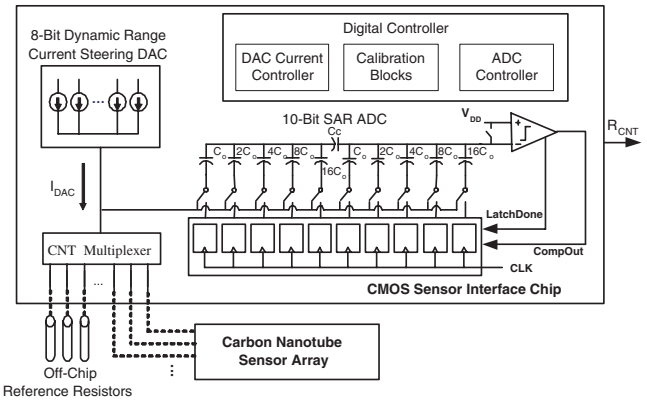


Fig. 2. Proposed interface architecture with an on-chip calibration functionality. CNT sensors and the interface chip are integrated on a PCB level.

attractive because the interface can change the measurement resolution by changing the input current ($R_{LSB} = \frac{V_{LSB}}{I_{INPUT}}$).

This concept can be extended over an appropriate current range to attain the required dynamic range since the system only needs 2% measurement accuracy across the desired range of resistance measurement. Recently, a similar concept has been published [5]; the focus of [5] is on the micro hotplate temperature regulation. The goal of the proposed work is to optimize the architecture in energy constrained applications.

The proposed architecture is composed of an ADC, a current-steering DAC and a digital controller. A successive approximation register (SAR) ADC is chosen for this work because the only components that draw static current are the preamplifiers in the comparator. A thermometer-code current steering DAC is implemented to better match the DAC cells in the presence of process variation. The digital controller block serves three purposes: adaptively controlling the DAC current as the resistance changes, controlling the ADC operation, and calibrating non-linearities of DAC. Note from Fig. 2 that two extra bits are added to the required 16-bit dynamic range to enable an all-digital DAC calibration, as explained in Sec. IV-B. Also, the designed chip can interface to 24 CNT sensors, which are sequentially accessed through a CNT multiplexer.

There are two modes of operation: a DAC calibration mode and a resistance measurement mode (Fig. 3.) In the resistance measurement mode, the analog blocks are duty-cycled to reduce the power consumption. By modeling the operation of each circuit block, the proposed architecture can be optimized.

B. Architecture Optimization

Energy per conversion is a metric used in designing converters for energy-constrained applications, so the same idea is applied to optimize the proposed architecture. The supply voltages in both analog and digital domains are scaled to 1.2V and 0.5V, respectively. Also, different ways of allocating 18-bit dynamic range to 2 analog blocks are studied to optimize the energy consumption. Energy per resistance conversion can be represented as

$$E_{OP} = P_{ADC} \times T_{ADC} + P_{DAC} \times T_{DAC} + E_{DIGITAL} \quad (1)$$

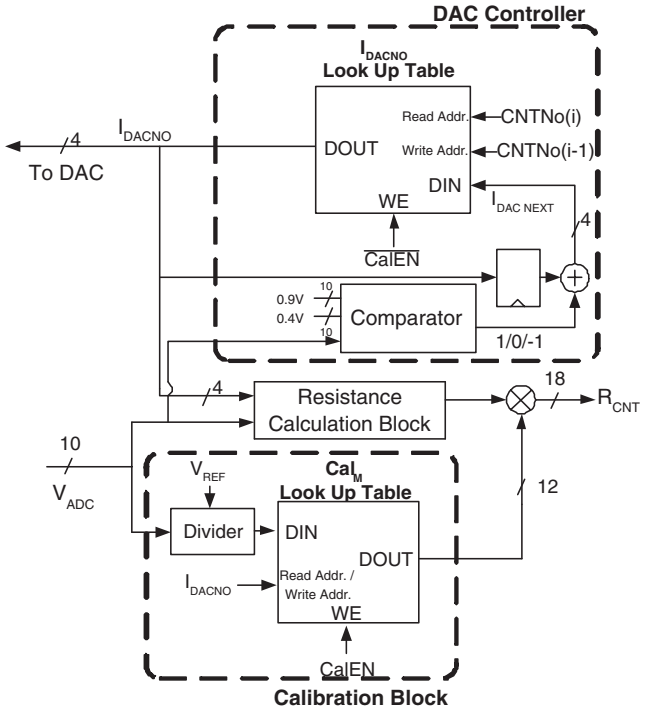


Fig. 3. Block diagram showing the critical dataflow in the digital controller.

The objective of the optimization is to minimize E_{OP} as N varies, where N is the number of bits allocated to the ADC.

In the case of SAR ADC, T_{ADC} can simply be modeled as $N \times T_{CLK}$. Modeling T_{DAC} is not as straight forward because it is in general a function of N and parasitic capacitances at the ADC input node. When the ADC is N bit, the signal present at the ADC input node should also have at least N-bit precision. Thus,

$$T_{DAC} \geq R_{INPUT} \times C_{INPUT} \times \ln(2^N) \quad (2)$$

where R_{INPUT} and C_{INPUT} are the effective resistance and capacitance looking into the ADC input node from the current steering DAC. R_{INPUT} and C_{INPUT} can be approximated as the CNT resistance and the sum of capacitances from the capacitor DAC in the ADC and the parasitic capacitance at the input signal node, respectively. P_{ADC} is extrapolated from the figure-of-merit (FOM) of typical low speed ADCs assuming 20kS/s operation with an FOM of 250fJ/conversion step.

To model the DAC power, I_{LSB} should be determined. The I_{LSB} is determined by the largest resistance of interest and the required voltage headroom for the DAC (in this implementation, 0.3V headroom is guaranteed) : to measure 9MΩ with 0.9V voltage range, 100nA is chosen as the minimum current.

The optimal N is determined based on these models: the energy per conversion achieves a narrow optimum around N = 11. However, designing a single-ended 11-bit ADC is not a trivial task, and the penalty paid by using 10-bit ADC instead is only 17%. Thus, a 10-bit ADC is used in this system.

IV. Circuit Design and Optimization

A. Control Schemes

The DAC control for the proposed architecture is an under-constrained problem in that several combinations of current and voltage can result in the same resistance value. Observing that the proposed architecture can increase the measurement resolution by increasing the input current, the digital controller drives the DAC current to be the maximum while keeping enough headroom for the DAC current sources (Fig. 3.) The control scheme is further simplified by allowing only binary-weighted current from the DAC. In other words, the DAC output current can be one of 9 levels (100 nA, 200 nA, ... , 25.6 μA). Each current level is denoted with 4-bit I_{DACNO}, which takes on the values 0 - 8 in increasing current order.

The resistance of each CNT sensor will change as chemical is introduced: the current controller automatically adjusts I_{DACNO} for the next measurement based on the current measurement (Fig. 3.) If the voltage from the i^{th} sensor is greater than 0.9V or less than 0.4V, the comparator outputs -1 and 1, respectively. The output of the comparator is added to the I_{DACNO} to update the look-up table for that particular CNT's next measurement.

B. DAC Current Calibration

In order to measure the exact resistance, the proposed architecture relies heavily on the ideal characteristics of the DAC and ADC. However, process variations can deteriorate the linearity of the current-steering DAC and ADC. This results in a nonlinear resistance conversion characteristic. Thus, an all-digital calibration technique is proposed to calibrate the DAC current such that the DAC linearity error is less than 1% across the 100 nA - 25.6 μA current range.

Unlike other applications, the DAC does not need to provide an accurate predetermined current. As long as the system *knows* how much current is being supplied at a given current word, the system can adapt to the DAC characteristics to attain the desired accuracy. Since the architecture has 2 extra bits of dynamic range, a digital calibration technique is a viable option (Fig. 3.) Fortunately, there are only 9 different current levels for the DAC, which implies that the DAC can be fully characterized with 9 calibration words (CAL_M, where M is the input current word). The basic idea of the calibration is to source the current to a known reference resistance and read the voltage across the reference resistance. The calibration words can be derived through the following relationship.

$$CAL_M = \frac{I_{IDEAL}}{I_{REAL}} = \frac{V_{REFERENCE}}{V_{MEASURED}} \quad (3)$$

where I_{IDEAL} is the predefined current level (ideal current), I_{REAL} is the actual current sourced by the DAC, $V_{REFERENCE}$ is the voltage across $R_{REFERENCE}$ that would be measured by the system if the DAC current is the same as the predefined current, and $V_{MEASURED}$ is the actual voltage measured by the ADC. To have highly accurate reference resistors, the implemented system has reference resistors off-chip. The calibration is performed when the system is turned on, and whenever the operating environment changes. The proposed digital calibration scheme can cause nonlinearity when V_{OFFSET} is present in the ADC. Thus, two preamplifier stages are introduced in the comparator to reduce V_{OFFSET}.

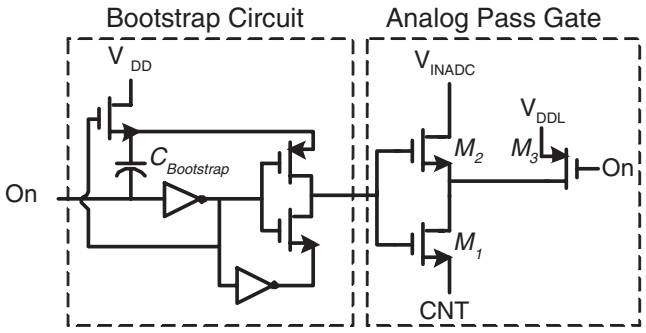
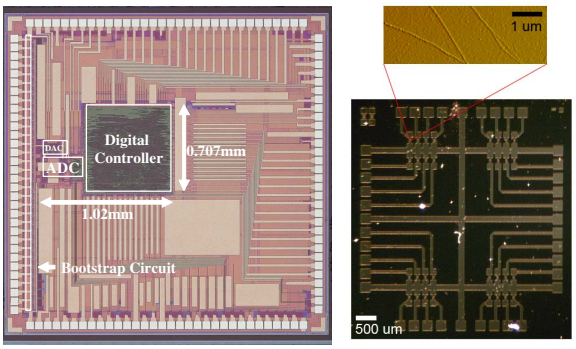


Fig. 4. Analog pass gate structure, with bootstrap circuitry, used in the CNT multiplexer.



(a) (b)

Fig. 5. Die Photo of (a) the developed CMOS interface circuit. (b) the CNT chemical sensor chip.

C. CNT Multiplexer Design

In the low-end resistance measurement, the non-linear resistance of pass transistors can cause linearity errors. The designed system interfaces the CNT through the pass gate shown in Fig. 4. To minimize the on-resistance, the width of pass transistors are made large, and the gate of the pass transistors are voltage bootstrapped with low leakage bootstrap circuitry. When the pass gate is turned off, the access transistor M_2 is reverse-V_{GS} biased via V_{DDL} to minimize the voltage-dependent leakage current through the large pass transistors.

V. Chip Measurement Result

The CMOS interface chip was fabricated in a 0.18 μm CMOS process (Fig. 5(a)) to verify the proposed scheme. T_{DAC} of 512 μs was sufficient to provide 10-bit signal resolution at the input of ADC, and was kept at 512 μs throughout the chip testing. Fig. 6 shows the functionality of

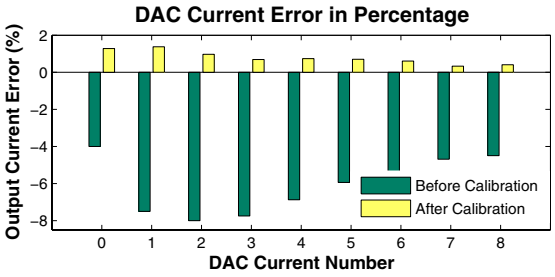
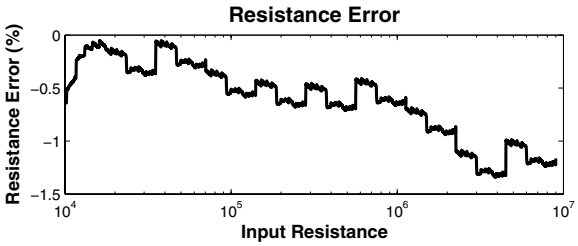
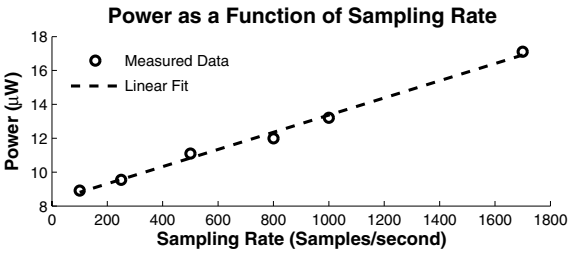


Fig. 6. Current error before and after the proposed calibration



(a)



(b)

Fig. 7. (a) Measurement error across the entire dynamic range. (b) Power scales linearly as the sampling rate decreases.

proposed DAC calibration. DAC current error up to 8% is calibrated to have less than 1.2% error for every DAC word.

Fig. 7(a) shows the accuracy of the interface: the absolute error of measurement is less than 1.34% across the whole dynamic range. The primary source of error in the measurement was the DAC nonlinearity. Fig. 7(b) shows that the power dissipation scales linearly as the sampling rate reduces. Thus, the conversion operation can be gated when the measurement does not require a fine time resolution. Note that the measurement in Fig. 7(b) was taken with random resistor samples, and is subjected to an increase based on the value of sensed resistances. In the worst case, 32 μW is consumed at 1.83 kS/s sampling rate.

VI. System Integration Result

CNT chemical sensors and the interface chip is integrated on a PCB level, and the functionality of the system is tested by exposing the CNT sensors to 50 ppm, 150 ppm and 300 ppm

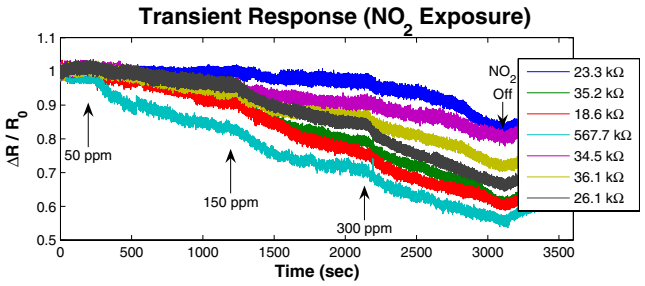


Fig. 8. The CNT resistance change detected with the interface circuitry. Experimental conditions (gas exposure time, chamber size, and device geometry) differ from that in Fig. 1.

of NO_2. The gas was introduced to the CNT sensors that sit in a gas chamber, and the measurement taken by the fabricated chip is acquired by a logic analyzer. The real-time sensing operation of the CNTs as well as the proper functionality of the CMOS interface can be seen from Fig 8.

VII. Conclusion

A low power chemical sensor system using carbon nanotubes as the sensing medium is presented. Extending the dynamic range using an automatic gain control, along with on-chip digital calibration of analog components, can be achieved with low energy overhead. This work can be extended to develop a single-chip solution of chemical sensor system by bringing reference resistors on-chip and packaging carbon nanotubes on-die.

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