Research Portfolio

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Contents

Microbial Robotics 2
Symbolic Multiprocessor Architectures 3
Replacing Precision with Computation 4
Reversible Computers 6
VLSI Microdisplays 9
Energy Recovering Logic Gates 11
Abacus SIMD Vision Processing array 14
Reprogrammable Logic Devices 17
Lattice Gas Fluid Flow Computing 21
Quasi-Static Compilers 23
Low Latency and High Speed
  Chip to Chip Signalling Technologies 24
Switched Capacitor Linear Equation Solvers 28
Metro Routing Architecture 30
New Research Directions 34
Earlier Work 35
Microbial Robotics
Symbolic Multiprocessor Architectures
Replacing Precision with Computation

Synopsis

Escalating costs and increased demand for precision fabrication characterize essentially all technologies, except for the, exponential decreases in the cost of computation and storage capacity over the past 50 years. This availability of essentially free computation and storage strongly motivates replacing precision with computation wherever possible. Our recent work capitalizes on this idea in two areas:

- **Synthetic Aperture Microscopy** replaces the precision optical fabrication required for microscope objectives with computational lenses, achieving unprecedented combinations of depth of field, numerical aperture (hence resolution) and dramatically lower cost of manufacture.

- **Multiple Projector Displays** utilize this idea by software aligning and color correcting a set of overlapped projection displays such that the seams become invisible. Previous approaches attempted to correct color, geometric defects, and intensity gradients by manual adjustment or precision optical and mechanical assembly, resulting in costly and unstable designs.

Artifacts

- Three increasingly sophisticated versions of the SAM have been constructed by Dr. Michael Mermelstein for his Ph.D. research. Additional more sophisticated versions are under development, including some which will also address the issues of lithographic patterning using similar technology.

- A software only prototype of the multiple projector display has been demonstrated by Dr. Rajeev Surati as part of his Ph.D. research, and a fully automatic frame buffer refresh version is under development by Ivan Gonsalves using field programmable gate array technology.

Student involvement and thesis work


Patents

- Surati, R, and Knight, TF, “Seamless Video Displays” (applied)

Impact

I anticipate that this set of techniques will become one of the dominant engineering metaphors in the next decade, as the economic benefits of reduced manufacturing costs become obvious. Dr. Mermelstein has started a Watertown based company developing these ideas supported by commercial sales of the microscope, and developing more sophisticated versions for mask exposure.
Reversible Computers

Synopsis

Reversible computation is important for three reasons:

- Technologically, it yields low energy dissipation in computing structures. This may be important for energy recovery in silicon after the VDD power supply voltage reductions now underway reach their limits of approximately 1 volt.

- Scientifically, reversibility is a key concept relating physics (thermodynamics) and computation (information theory). Understanding this relationship more deeply will be important as we try to build computationally intensive structures at smaller levels, such as molecular and quantum computers. Indeed, all quantum computation is by necessity completely reversible.

- Organizationally, reversibility plays an essential and likely under appreciated role in some architectural and programming domains, such as speculative execution, error recovery and the transactional updates of databases.

Funding history

Currently this work is funded under an Arpa contract “Reversible Computers for Energy Efficient and Trustable Computation.” Options in this effort fund very general studies in the physics of computation, as well. Funding began in October, 1995 and continues until October, 1998.

Papers


Artifacts

Figure 4.1: Tick, the first fully reversible computer implementation is a simple 8 bit processor built with a standard CMOS logic family and technology. Future versions will be more sophisticated architectures and use SCRL gate technology.

Student involvement and thesis work

- Matt DeBergailis is currently an undergraduate UROP student working with us, but also worked with on this project as a high school student in the RSI summer program. His presentation and writeup won the top award for students in that program.
Impact

I anticipate no significant short term products out of this effort, which is directed more towards long range scientific results, rather than short term industrial spinoffs. Scientifically, has been important to demonstrate the first reversible machines which recover energy by virtue of their reversibility, and to develop programming techniques for this class of processor. There may be shorter term spinoffs associated with the organizational ideas, and their relationship to program integrity and auditing.

Dr. Norman Margolus is assisting in this effort, and has published on the physical limits of computation.
VLSI Microdisplays

Synopsis

The use of off the shelf CMOS fabrication technology for the construction of high resolution displays provides significant cost reductions over macroscopic construction techniques, allowing the integration of driver logic, memory, and computation onto the same die as the display. This allows construction of true single chip processors, where the display as well as the computation is integrated onto a single die. The key economic factor is the ability to leverage the $100 billion/year investment in silicon processing technology for a wider range of applications.

Funding History

My initial work in this area was unfunded and concentrated on polyaniline materials. Liquid crystal work was funded from October 1993 through October 1995 with a grant from the Arpa/ESTO display technology office.

Papers


Artifacts

- First display incorporating optical distortion correction in pixel placement.
- First display incorporating pixel jitter for antialiasing elimination.
- First microdisplay using covered grating structures as color filters.

Impact

Phillip Alvelda has formed a startup, The MicroDisplay Corporation, funded at $10M, and has secured a two year $6M Arpa contract to fabricate high resolution liquid crystal displays on silicon. He has been joined by two of my other students, Michael Bolotski and Carlin Vieri, and they are currently ramping up to production on a 120,000 unit order. The company is in the final stages of being acquired by a major semiconductor manufacturer.
Figure 5.1: The first liquid crystal microdisplay using tri-band color filters constructed with diffraction gratings, and manufactured with a standard silicon VLSI process. Here, the different grating spacings of the three adjacent red, green, and blue filters are shown within each 30 x 30 micron tri-color pixel.

**Patents**


**Student involvement and thesis work**

- Alvelda, Phillip, “Liquid Crystal on Silicon VLSI Microdisplays,” SM May, 1994
- De Souza, John, “Developing a Prototype Micro Liquid Crystal Display,” SB May, 1993
Energy Recovering Logic Gates

Synopsis

The dissipation of integrated circuit components was the driving force behind the technological shift from NMOS logic families to CMOS technology in about 1980. Ironically, modern CMOS processors are now limited primarily by the $CV^2f$ power dissipation of their logic. Since the work of Landauer, Bennett and Fredkin in the early seventies, we have known that it was possible in principle to perform dissipationless computing. Our major contribution in this work is to demonstrate the first practical implementation of a dissipationless technology, using off the shelf CMOS fabrication processes. The 8 x 8 integer multiplier Saed Younis describes in his thesis is the most complex fully reversible computing element yet constructed, and demonstrated the power savings possible with this technology.

Funding history

This work has been largely funded under the Arpa low power contract which also funded the Abacus project, and has received little explicit funding. More recent work has been funded under the reversible computing umbrella.

Papers


Artifacts

- Designed and tested 8 x 8 reversible multiplier chip demonstrating the technology and the power savings achievable.
- Designed and tested transmission line power supply techniques and demonstrated effective power savings.
Figure 6.1: This closeup of the first circuit constructed and tested with SCRL logic shows a forward and backward gate and the power recovering clock rails in an 8 x 8 reversible multiplier array.

**Patents**

- Knight, TF, and Younis, S, “Charge Recovery Logic including Split Level Logic” (No. 5,378,940)

**Popular Press**

- “Silicon in Reverse,” Peter Wayner, Byte Magazine, August, 1994

**Student involvement and thesis work**

- Saed Younis completed a Ph.D., “Asymptotically Zero Energy Computing Using Split-Level Charge Recovery Logic,” in July, 1994, and is now running an advanced VLSI design group at Qualcomm, Inc. in the area of low power digital design.


- Mathew Becker completed a Ph.D. thesis “Resonant Transmission Line Drivers,” in January, 2000, which demonstrates both practical and theoretical results in the design of
high efficiency resonant power supplies for SCRL and for the provision of low energy, low skew clock distribution in high speed conventional processors.

Impact

SCRL will become an important technology when current techniques for lowering on chip power (largely voltage reduction) bottom out in about five years. Until then, the overheads associated with SCRL logic circuitry make the approach unattractive. Special applications, such as driving highly capacitive loads, could become important application areas sooner. Applications for such capacitive drivers include clocks in CCD imagers, VLSI microdisplays, and clocking signals in high performance conventional processors.

Academically, our work, along with the work of Bill Athas at ISI, has sparked renewed interest in the field, with active research now going on at AT&T, IBM Yorktown, Georgia Tech, and Yale. Theoretical computer scientists such as Vitanyi and Li have taken note and are producing theoretical results based on dissipationless reversible computing.
Abacus SIMD Vision Processing array

Synopsis

This project is an outgrowth of my earlier work on the connection machine. I was disappointed in the performance achieved by commercial implementations of this architecture, both at Thinking Machines, and at other locations such as MasPar. Our effort has resulted in the fastest implementation to date of the massively parallel SIMD architecture, operating with a processor density more than 64 times higher than the CM-2, and a clock rate 16 times higher. This was achieved with both careful architectural design and meticulous attention to implementation details.

Papers


Funding History

This project was funded by an Arpa Low Power program from the ESTO office, running from October 1992 through October 1995. Much of our other low power work was funded under this same contract.

Student involvement and thesis work


Figure 7.1: The Abacus die photograph showing the 1024 processors arranged in a pair of 16 x 32 arrays separated by instruction and address drivers. The die is mounted in a custom, controlled impedance and controlled power distribution integrated circuit package.

Patents

• Hillis, W, et al., “Connection Machine Processor Design” (No. 4,709,327)

• DeHon, A, Bolotski, M, and Knight, TF; “DPGA-Coupled Microprocessors,”(patent applied)

Impact

With the scaling down of industrial work in highly parallel computers, the commercial competitors to this work (MasPar, NCR GAPP, CM-2, DAP) have largely abandoned the massively parallel computing arena. I anticipate that significant commercial impact will arise from the
Figure 7.2: The Abacus processor consists of two 32 bit two-read one-write register files and a pair of three input lookup tables, together with local neighbor interconnection networks.

reconfigurable versions of these architectures, which will incorporate the high clock speeds and sophisticated signalling strategies used in Abacus. Likely this work will be centered around processor-in-memory ideas, which are enjoying renewed interest for large scale database applications.
Reprogrammable Logic Devices

Synopsis

The enormous success of the PC computing platform comes at the cost of rigid standardization of the architectures of the machines. Our next major technical advance in computer architecture will be to wean ourselves from this rigid dependence by the creation and application of reprogrammable logic devices substantially more potent than the simple structures available today. This work innovates in two important directions – active re-use of wiring within the die, and increased functionality of the reconfigurable components. Future work will concentrate on software issues for dynamically reprogramming this logic, and in integrating this technology with other important components, such as DRAM and high performance processors.

Funding history

This project is funded under an Arpa contract, “Reinventing Computing,” which runs from October 1994 through October 1997. Other projects in this effort include the quasistatic compiler.

Papers


Artifacts

- DPGA Prototype chip fabricated and tested.
- TSFPGA component fabricated.
Matrix component fabricated.

Figure 8.1: The first reconfigurable logic component which can change its logic elements and interconnection patterns in a single clock cycle. The chip caches four on-chip contexts which can be quickly interchanged.

**Student involvement and thesis work**


- Helen Ruan is a VI-A student assigned to Intel, and who is assisting us in high level Verilog modelling of the reconfigurable components, and in writing partitioning and routing tools.

Figure 8.2: Four cells from the first coarse grained reconfigurable logic component, containing a 3 port SRAM array, an 8 bit ALU, and an 8x8 multiplier array. Data, addresses, and instructions are all 8 bit wide quantities, and are routed in a uniform array of gang-routed 8 bit wiring channels.


Patents

- DeHon, A, Bolotski, M, and Knight, TF, “DPGA-Coupled Microprocessors,” (No. 6,052,773, April, 2000)
- DeHon, A, Knight, TF, Bolotski, M, Tau, E, Eslick, I, Chen, D, and Brown, J, “Dynamically Programmable Gate Array with Multiple Contexts,” (No. 5,742,180 April, 1998)
- DeHon, A, Mirsky, E, and Knight, TF, “Intermediate Grain Rconfigurable Processing Device,” (No. 6,266,760, July, 2001)

Popular Press

Scientific American, in its June 1997 features a discussion of reconfigurable computers, including a discussion of our work.
Impact

Ethan Mirsky, Ian Eslick, and Robert French have formed a startup company, Silicon Spice, with $2 million in venture capital and a $800,000 DARPA contract to commercialize the results of this research. Other commercial firms such as Xilinx and GigaOps are following our work closely, and we believe that Xilinx is about to announce a product similar to our DPGA part. Toronto, the University of Washington, and Berkeley have active research programs working in similar areas. Discussions with Intel, Sun, and Digital on the possible application of this technology in next generation processors are ongoing. Hewlett Packard Laboratory in Bristol, England is collaborating on similar work. Andre DeHon completed a post-doc at Berkeley with Prof. Warznyeck following up on some of this work and is continuing to work in this area as a junior faculty member at Caltech. Researchers at Lockheed/Sanders are using some of our approaches in a high performance DSP processor for synthetic aperture radars.

Silicon Spice was purchased by Broadcom in August, 2000 at a valuation of approximately one billion dollars.

More recently, many of the Matrix concepts are directly incorporated into the RAW architecture of Prof. Agarwal.
Lattice Gas Fluid Flow Computing

Synopsis

Physicists have known for several years that simple forms of cellular automata can approximately model fluid behavior of gases and liquids. A variety of problems with these approaches, including non-isotropic behavior, poor boundary behavior, and an inability to handle the problem with multi-gridding approaches made the approach unusable for more than toy problems. In collaboration with Prof. Kim Molvig and Prof. Greg Papadopoulos several of these difficult problems were solved, along with the development of a novel computer architecture for efficiently implementing the inner algorithm loop. Exa Corporation was formed to commercialize these efforts. In addition to architectural design, I played a major role in the development of over-relaxation techniques for dramatically reducing the effective viscosity of the fluids, allowing computations with much higher Reynolds’s number than could be achieved previously. More recently, the company has transitioned to a software only approach, using the VIS instruction set of the UltraSparc processor to quickly perform parallel, limited range arithmetic operations on a standard platform.

Funding History

This work was performed at Exa, Inc., a startup venture to commercialize discrete fluid flow simulations, and was funded by personal investments, venture capital, and an Arpa/ISTO contract.

Patents

Figure 9.1: The FX processor component implements a parallel version of the lattice gas fluid flow calculation algorithm. The eight parallel integer units at the lower right process particle collisions at each voxel.
Quasi-Static Compilers

Synopsis

The tension between powerful language features and efficient compilation has a history as long as the history of programming languages themselves. In this work, we attempt to resolve this tension by recognizing that the compilation of a program need not be viewed as a one-time operation, but can be viewed a part of a process of optimizing execution. Often compilers are unaware of important aspects of the programs, the execution environment, or the data being processed. By instrumenting compiled code, we can measure the dynamic behavior of programs operating on the real data, in the real environment, and then use those measurements to improve subsequent compilation results.

Funding History

This effort is funded under the Arpa “Reinventing Computing” contract, October 1994 through October, 1997.

Students

- Blair, Michael, “Descartes: A Dynamic Execution and Optimization Environment for Scheme Programs,” Expected September, 1997

Impact

Jeremy Brown is preparing a journal article for publication on results of dynamic inlining and branch prediction feedback. We have an ongoing relationship with Josh Fischer’s compiler group at Hewlett Packard Laboratory.
Low Latency and High Speed Chip to Chip Signalling Technologies

 Synopsis

High latency and limited wiring bandwidth are principal concerns of modern digital engineering. This work develops several new ideas to improve performance by capitalizing on the complex structures which can be inexpensively be constructed on modern integrated circuits. By making the tradeoff of higher performance at the cost of increasing circuit complexity, we have improved the wiring capacity by factors of ten or more.

 Funding history

This effort has been funded as part of a number of different projects. Work on the controlled impedance drivers was funded under the LCS/AI/RLE VLSI contract. Work on the capacitive coupling was performed at Polychip, Inc. Parallel termination work was performed at Thinking Machines, Inc. Results of this research were applied as part of the Abacus and Metro efforts (q.v.).

Papers

- DeHon, A, and Knight, TF, “High Performance Point to Point Transmission Line Signalling,” accepted, VLSI Design.


**Artifacts**

- Test circuits for low voltage high speed terminated signalling fabricated and tested.
- Test circuits for boundary scan sensing of the wiring environment fabricated and tested.
- First test circuits for noise and power coding fabricated and tested.
- First implementations of capacitive chip to board signalling technology designed and tested.
- First implementations of on-chip servoed parallel terminations fabricated and tested.
- First implementations of postcharge logic buffering fabricated and tested.

Figure 11.1: The first fully automatic impedance adjusting pad design was tested on this die for the Metro interconnection network, and reported in an ISSCC paper. A subsequent paper describes how to perform board level testing of interconnect with a slightly modified version of this same design.

Figure 11.2: The first silicon die coupled capacitively to a substrate, designed to mate with large printed circuit board traces in this high speed test die.
Student involvement and thesis work

- Ed Ouellette is currently working as a Ph.D. student with me and Prof. Kimmerling (Materials Science) on Erbium doped silicon photoemitters for high speed on chip signalling.
- Amirtharajah, Rajaveen, “High Bandwidth Interchip Communication for Regular Networks,” SM May, 1994
- Simon, Thomas, “Fast CMOS Buffering With Post-Charge Logic,” SM June, 1994
- Biber, Alice, “The Design of an Application Specific Interface Driver for a High Capacitive Load,” SM December, 1989

Patents

- Knight, TF, and Wu, Henry, “Method and Apparatus for Skew-Free Distribution of Digital Signal Using Matched Variable Delay Lines” (patent applied)
- Knight, TF, and Salzman, D, “Method and Apparatus for Capacitive Chip to Chip Signalling” (No. 5,629,838, May 13, 1997)

Impact

Our techniques are now being widely used in important commercial applications, such as the signalling in the high speed Rambus memory components. Similar low voltage signalling is used in an NEC signal processor. Capacitive signalling is being actively explored by Intel for next generation processor to memory interconnect. In our own work, we are applying the controlled impedance drive in the Abacus processor design and in the Metro routing network components. Sun will be using the parallel termination ideas in their next generation of parallel
server systems. The noise and power coding ideas explored in theses by Lee and Tabor are being pursued in the academic environment by Prof. Burleson at UMass Amherst, and in an industrial setting within the high performance processor group at NEC in Japan.
Switched Capacitor Linear Equation Solvers

Synopsis

This work investigates a radically different way of solving computational problems. In it, we apply analog switched capacitor circuit techniques to the solution of linear systems of equations, including least-squared solutions and linear constraint problems. The solution technique is unusual because information flow is bidirectional – error is distributed uniformly among all the terms of a constraint equation. Again, the technique is unusual because the form of the solving circuit directly reflects the problem constraints, accepting input values on whatever nodes have information. These solution techniques have been successfully applied to discretized partial differential equations for computer vision, but I believe have a dramatically larger range of applicability. In particular, I believe that such constraint satisfaction by bidirectional information flow is central to the functioning of the brain.

Funding History

There has been no specific funding for this research.

Papers


Artifacts

• Discrete component implementation of a switched capacitor linear equation solver fabricated and tested.
• Integrated circuit implementing switched capacitor constraints fabricated and tested for vision applications.

Student involvement and thesis work


Metro Routing Architecture

Synopsis

The major technical difficulty in construction of high performance parallel machines is the construction of low latency, high bandwidth interconnection networks. This work presents a complete solution to the design of such networks, based on novel networks, novel packaging, novel interconnection technology, and novel circuit design.

Funding history

This project was funded under the last joint LCS/AI/RLE VLSI contract, running from October 1991 through October 1994.

Papers


Artifacts

• RN-1 Router component designed and tested.

• Custom packages for 3-D network designed and fabricated.

• Novel button contact connector designed and fabricated.

• Simulators for fault tolerance behavior implemented.

• Simulators for network performance implemented.

• Metro architecture implemented in Actel gate array technology.

• Test environment for Transit router on Sun SBUS boards.

Student involvement and thesis work

• Becker, Matt, “Fast Arbitration in Dilated Routers,” SM May, 1995

• Hara, Kazuhiro, “High Speed Economical Design Implementation of the Transit Network Router,” SM May, 1995

• Chen, Weip, “Communications Effects on Parallel Algorithm Performance,” SB May, 1993

• DeHon, Andre, “Robust High-Speed Network Design for Large Scale Multiprocessing,” SM February 1993


• Teran, Gregory, “Analytical Estimation of Multipath Fault Tolerance in Multistage Interconnection Networks,” SB May, 1992

• Lackritz, Neal, “TMNC – A Distributed Crossbar Switch Architecture,” SM May, 1992

• Sobalvarro, Patrick, “Probabilistic Analysis of Multistate Switching Network Performance,” SM February, 1992
Figure 13.1: The RN-1 routing component formed the core of the Transit multiprocessor interconnection network. Here the die is shown in its custom controlled impedance 3-D stackable package with cooling channels.
• DeHon, Andre, “Fat Tree Interconnection Networks in Transit,” SB January, 1990

**Patents**

• Leighton, T, Maggs, B, and Knight, TF, “Expansive and Dispersive Multibutterfly Networks” (No. 5,521,591, May, 1996)

**Impact**

This work set the direction for much of the SCI P1596 IEEE interconnection standard, during initial meetings with John Moussouris. It also has had significant impact on the designs of the Convex, Maspar, and Thinking Machines interconnection networks, although the TMC machine affected was never built.
New Research Directions

In addition to completing the research described above, I have several startup efforts under way, including:

- **Computing with Biological Cells:** I am investigating ways in which we can use engineered microorganisms to perform useful computation. The central advantages of such an approach include low cost manufacturing, engineering at the atomic level, and the ability to construct artifacts with from four to six orders of magnitude more components. Significant problems in speed and reliability remain.

- **Amorphous Computing:** In a collaboration with Prof. Sussman and Prof. Abelson, we have recently proposed an ambitious effort to develop a new branch of computer science based on the profligate use of potentially unreliable and unorganized computation to solve important engineering problems. One implementation technology for such systems might be the microbial cells discussed above, but we intend to engineer examples from more traditional silicon technology as a prelude. The effort combines aspects from diverse disciplines such as manifold theory, parallel algorithm design, physics, and language design to lead to a new computational style in which we assume that the difficult problem is communication rather than computation – relying solely on local communication to solve a problem. We believe there are important pedagogic as well as scientific and engineering spinoffs from this project, centered around the notion that the complexity of most engineering problems arises not from the physics – which is locally simple – but from the often misguided attempt to understand that physics with global techniques.

- **Aries Language and Architecture:** A novel dynamically typed, data ownership, capability based language and architecture are under development with a strong emphasis on safety, introspective design, and performance. Inherently parallel, with typing of not only data objects, but also operations and typing on compound data objects such as tensors and matrices, the Aries language and processor attempt to change the way in which we program parallel machines, bringing them much more in line with the mathematical operations users typically wish to perform.

Some smaller projects which I am involved with currently include:

- **High speed CMOS logic gates:** I have developed a novel inverter circuit which has an loaded delay 36% smaller than the delay of a normal inverter, at the cost of higher dissipation and lowered noise margins.

- **Constraint Based Logic Gates:** I am developing a logic family which implements logical constraints, i.e. can compute an input from a set of outputs. I believe such gates may be important in implementing some of the newer constraint based computational models proposed by Yip and Sussman.

- **Full Color Stereograms:** I have developed a novel approach to viewing stereo pairs, similar to the comic book red/blue stereoscopy, in full color, using non-overlapping red/green/blue spectral bands for each eye.
**Earlier Work**

A synopsis of some of my earlier contributions include

1. **ITS operating system (1967)**
   - Wrote the initial kernel of the ITS operating system for the PDP-6 (later PDP-10) computer in the period 1966-1973. Authored the modified debugger/command processor used as the top level user interface. ITS was the dominant operating system along with CTSS and Multics for Project Mac, and subsequently the Artificial Intelligence Laboratory and Laboratory for Computer Science. It was transferred to four other PDP-10 installations at MIT, updated to run on all versions of the PDP-10 hardware, and is now still running on emulated hardware (PDP-10 emulation on a Digital Alpha processor).

2. **PDP-6 teletype control (1966)**
   - Designed and implemented the first PDP-6 teletype controller capable of handling multiple serial terminals. This hardware enabled the development of a time shared operating system on the PDP-6. Similar hardware was replicated for several of the other MIT KA-10 configurations.

3. **Arpanet interface (1968)**
   - Designed and supervised the construction of the first PDP-10 Arpanet interfaces with Bob Metcalfe on the MIT Dynamic Modelling machine. Replicated for all MIT PDP-10s.

   - Designed and constructed with Jeff Rubin the first direct memory access interface between user level code on the PDP-10 operating system and PDP-11 memory. This interface played a crucial role in the development of the XGP, bitmapped displays, and the Lisp Machine.

5. **XGP interface (1970)**
   - Modified and implemented with J. Pitts Jarvis a University of Utah interface for the Xerox Graphics Printer. Wrote all PDP-11 and PDP-10 support code and font conversion software. This printer became an MIT wide resource for bitmap printing until it was replaced in 1976 by the Xerox Dover printer.

6. **Logo displays (1970)**
   - Designed and implemented stroke based displays specialized for turtle graphics in support of the Laboratory’s Logo development effort. These displays were used for a month-long elementary educational experiment in Exeter, England in 1971.

7. **Bitmap displays (1972)**
• Designed and implemented one of the first semiconductor memory based bitmap displays. Replicated at the Plasma Fusion Center at MIT and commercialized with sales to Bolt Beranek and Neuman and INRIA. Led directly to the development of the Bedford Computer Systems newspaper layout system, and indirectly to many of the bitmapped display devices available today.

8. Network Shared File System (1972)
• Designed and implemented with Jeff Rubin the first transparent remote file access over the Arpanet, allowing any ITS program to access remote files as if they were local, without modification to the requesting program.

• Designed and implemented a prototype (1974) and production (1976) version of the MIT Lisp Machine processor, a general purpose 32 bit microprogrammed machine with performance tuned to emulation of other instruction sets. Thirty-four of these 2000+ chip machines were constructed at MIT in our laboratory and at the Plasma Fusion Center. The design was later (1981) implemented directly by Symbolics and LMI. LMI re-engineered the design again as the basis of all of their later machines. Texas Instruments later (1982-83) implemented a slightly modified version with surface mount technology, and subsequently designed a custom single chip version, with largely the same architecture, in 1987.

• Designed and implemented with Jack Holloway the first local area network on campus, as a re-engineered version of the Xerox 3 Mbaud Ethernet. The Chaosnet ran at 8 Mbaud, and was eventually installed on all of the PDP-10 machines on campus, including the Speech and EE Department facilities, and was used to tie the Plasma Fusion Center and Math Department display facilities into other on-campus hardware. The important idea of using a preamble bit string, as part of the Ethernet packet standard, first used on the Chaosnet, was eventually incorporated in the 10 Mbaud Ethernet standard through discussions with Ethernet designers at Digital.

• Cooperated in the development of the connection machine architecture and prototype implementations at MIT. Responsible for choice of signalling technology between processors and much of the processor architecture.

12. First Silicon Retina (1981)
• Designed and implemented the first silicon image sensor with integral data processing. This sensor used switched capacitor smoothing techniques. Mark Seidel has recently shown how to analytically model such switched capacitor constraint networks and improved the implementation substantially in his Ph.D. thesis.

- The Symbolics 3600 was a complete redesign of the MIT Lisp Machine, with an extended 36 bit word size. I played largely an advisory role in the detailed design of the processor, but was involved in details of the packaging, electrical and timing specifications of the busses, and in I/O interface design and specification.


- Designed and implemented a single chip integrated optical mouse, relying on statistical summation of motion estimates from a large number of sensor elements to achieve high performance without a predefined pattern of surface features. The quality increase and cost reductions of the mechanical mice during this time led to the abandonment of the project as a commercially feasible product, although working prototypes were produced, interfaced to Lisp Machines, and used within Symbolics.


- A detailed design of enhanced version of the connection machine architecture was carried out from 1983-1986 in collaboration with General Electric Corporate Research and Development. This planned architecture implemented dramatically improved processor density and performance goals (10x), and was dominated by a completely new high performance interconnection network called the Cross-Omega network. The network relied on novel high dilation switch components, with dramatically improved probability of interconnection success, and consequent reduced communications latency (30x). The project was halted due to lengthy delays in funding.

16. Ivory (1985)

- Architectural design and detailed circuit design for the Symbolics Ivory processor, a single chip 40 bit Lisp oriented symbolic processor.