Muralidaran Vijayaraghavan

CONTACT INFORMATION

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INTERESTS

Computer Architecture, Formal Verification, Proof Assistants, Distributed System Design, Programming Language Design

PROGRAMMING LANGUAGES

- *Functional languages:* Haskell
- *Imperative languages:* C, C++
- *Hardware description languages:* Verilog, Bluespec
- *Theorem provers:* Coq

EDUCATION

Massachusetts Institute of Technology, Cambridge, MA
Post Doctoral Associate, Computer Science and Artificial Intelligence Lab, ***Current***

- Supervisor: Assoc. Prof. Adam Chlipala

Massachusetts Institute of Technology, Cambridge, MA
Ph.D., Electrical Engineering and Computer Science, **GPA: 5.0/5.0** ***February 2016***

- Thesis topic: *Modular Verification of Hardware Systems*
- Advisor: Prof. Arvind, Assoc. Prof. Adam Chlipala

S.M., Electrical Engineering and Computer Science, **GPA: 5.0/5.0** ***February 2009***

- Thesis topic: *Theory of composable latency-insensitive refinements*
- Advisor: Prof. Arvind

Indian Institute of Technology, Madras, Chennai, India
B.Tech., Computer Science and Engineering, **GPA: 9.53/10.0** ***June 2006***

WORK EXPERIENCE

Research Intern, IBM T.J. Watson Research Center, Yorktown Heights, NY
Supervisor: Dr. Kattamuri Ekanadham
Summer 2010

Research Intern, VSSAD group, Intel Corporation, Hudson, MA
Supervisor: Prof. Joel Emer
Summer 2007, Summer 2008

SELECTED PUBLICATIONS

1. **Vijayaraghavan, M.**, Chlipala, A., Arvind, Dave, N. "Modular Deductive Verification of Multiprocessor Hardware Designs" *CAV 2015*
2. Yu, X., **Vijayaraghavan, M.**, Devadas, S. "A Proof of Correctness for the Tardis Cache Coherence Protocol" *CoRR arXiv:1505.06459 2015*

3. Karczmarek, M., Arvind, **Vijayaraghavan, M.** "A new synthesis procedure for atomic rules containing multi-cycle function blocks" *MEMOCODE 2014*
4. **Vijayaraghavan, M.**, Dave, N., Arvind. "Distributed Modular Hardware Compilation of Guarded Atomic Actions" *MEMOCODE 2013*
5. Khan, A., **Vijayaraghavan, M.**, Boyd-Wickizer, S., Arvind."Fast and cycle-accurate modeling of a multicore processor" *ISPASS 2012*
6. Khan, A., **Vijayaraghavan, M.**, Arvind. "A general technique for deterministic model-cycle-level debugging" *MEMOCODE 2012*
7. Pellauer, M., Agarwal, A., Khan, A., Ng, M. C., **Vijayaraghavan, M.**, Brewer, F., Emer, J. S. "Design contest overview: Combined architecture for network stream categorization and intrusion detection (CANSCID)" *MEMOCODE 2010*
8. Pellauer, M., **Vijayaraghavan, M.**, Adler, M., Arvind, Emer, J. S. "A-Port Networks: Preserving the Timed Behavior of Synchronous Systems for Modeling on FPGAs" *TRETS (2009)*
9. Agarwal, A., Dave, N., Fleming, K., Khan, A., King, M., Ng, M. C., **Vijayaraghavan M.** " Implementing a fast cartesian-polar matrix interpolator" *MEMOCODE 2009*
10. **Vijayaraghavan, M.**, Arvind. "Bounded Dataflow Networks and Latency-Insensitive circuits" *MEMOCODE 2009*
11. Pellauer, M., **Vijayaraghavan, M.**, Adler, M., Arvind, Emer, J. S. "A-Ports: an efficient abstraction for cycle-accurate performance models on FPGAs" *FPGA 2008*
12. Pellauer, M., **Vijayaraghavan, M.**, Adler, M., Arvind, Emer, J. S. "Quick Performance Models Quickly: Closely-Coupled Partitioned Simulation on FPGAs" *ISPASS 2008*
13. Fleming, K., King, M., Ng, M. C., Khan, A., **Vijayaraghavan, M.** "High-throughput Pipelined Mergesort" *MEMOCODE 2008*
14. Ng, M. C., **Vijayaraghavan, M.**, Dave, N., Arvind, Raghavan, G., Hicks, J. "From WiFi to WiMAX: Techniques for High-Level IP Reuse across Different OFDM Protocols" *MEMOCODE 2007*
15. Dave, N., Fleming, K., King, M., Pellauer, M., **Vijayaraghavan, M.** "Hardware Acceleration of Matrix Multiplication on a Xilinx FPGA" *MEMOCODE 2007*

Honours and Awards

- Winner of MEMOCODE design contests in 2007, 2008, 2009 and 2010
- All India Rank 15 in the Joint Entrance Examination for admission into IITs, June 2002
- Highest GPA in the Department of Computer Science and Engineering at IIT Madras, June 2003