Muralidaran Vijayaraghavan

CONTACT INFORMATION

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EDUCATION

Massachusetts Institute of Technology, Cambridge, MA
Ph.D., Electrical Engineering and Computer Science, **GPA 5.0/5.0** ***February 2016***

- Thesis topic: *Modular Verification of Hardware Systems*
- Advisors: Prof. Arvind, Prof. Adam Chlipala

S.M., Electrical Engineering and Computer Science, **GPA 5.0/5.0** ***February 2009***

- Thesis topic: *Theory of composable latency-insensitive refinements*
- Advisor: Prof. Arvind

Indian Institute of Technology, Madras, Chennai, India
B.Tech., Computer Science and Engineering, **GPA 9.53/10.0** ***June 2006***

WORK EXPERIENCE

Research Intern, IBM T.J. Watson Research Center, Yorktown Heights, NY ***Summer 2010***
Supervisor: Dr. Kattamuri Ekanadham

- Developed StructuralSpec, a high-level language for writing synchronous hardware modules with a very powerful static elaborator
- Developed a tool that converts a synchronous module into a latency-tolerant module, thus enabling modular refinements that even affect timing behaviors, without redesigning the circuit

Research Intern, VSSAD group, Intel Corporation, Hudson, MA ***Summers 2007, 2008***
Supervisor: Prof. Joel Emer

- Helped develop the *HASim* framework for designing FPGA-based simulators which have several orders of magnitude higher performance than conventional software simulators
- Helped establish a functional/timing partition for HASim, which enabled reuse of the same functional partition for different micro-architectures
- Implemented an out-of-order superscalar processor based on MIPS R10000 in HASim

INTERESTS

Programming Languages, Proof Assistants, Formal Verification, Language Specification, DSL, Computer Architecture, Hardware Synthesis

PROGRAMMING LANGUAGES

- *Functional languages:* Haskell
- *Imperative languages:* C, C++
- *Hardware description languages:* Verilog, Bluespec
- *Scripting:* Perl, Bash
- *Theorem provers:* Coq

PUBLICATIONS

1. Sizhuo Zhang, Arvind, **Muralidaran Vijayaraghavan**: *Taming Weak Memory Models.* CoRR abs/1606.05416 (2016)
2. **Muralidaran Vijayaraghavan**, Adam Chlipala, Arvind, Nirav Dave: *Modular Deductive Verification of Multiprocessor Hardware Designs.* CAV (2) 2015: 109-127
3. Xiangyao Yu, **Muralidaran Vijayaraghavan**, Srinivas Devadas: *A Proof of Correctness for the Tardis Cache Coherence Protocol.* CoRR abs/1505.06459 (2015)
4. Michal Karczmarek, Arvind, **Muralidaran Vijayaraghavan**: *A new synthesis procedure for atomic rules containing multi-cycle function blocks.* MEMOCODE 2014: 22-31

5. **Muralidaran Vijayaraghavan**, Nirav Dave, Arvind: *Modular compilation of guarded atomic actions*. MEMOCODE 2013: 177-188
6. Asif Khan, **Muralidaran Vijayaraghavan**, Silas Boyd-Wickizer, Arvind: *Fast and cycle-accurate modeling of a multicore processor*. ISPASS 2012: 178-187
7. Asif Khan, **Muralidaran Vijayaraghavan**, Arvind: *A general technique for deterministic model-cycle-level debugging*. MEMOCODE 2012: 109-118
8. Michael Pellauer, Abhinav Agarwal, Asif Khan, Man Cheuk Ng, **Muralidaran Vijayaraghavan**, Forrest Brewer, Joel S. Emer: *Design contest overview: Combined architecture for network stream categorization and intrusion detection (CANSCID)*. MEMOCODE 2010: 69-72
9. Michael Pellauer, **Muralidaran Vijayaraghavan**, Michael Adler, Arvind, Joel S. Emer: *A-Port Networks: Preserving the Timed Behavior of Synchronous Systems for Modeling on FPGAs*. TRETS 2(3): 16:1-16:26 (2009)
10. Abhinav Agarwal, Nirav Dave, Kermin Fleming, Asif Khan, Myron King, Man Cheuk Ng, **Muralidaran Vijayaraghavan**: *Implementing a fast cartesian-polar matrix interpolator*. MEMOCODE 2009: 73-76
11. **Muralidaran Vijayaraghavan**, Arvind: *Bounded Dataflow Networks and Latency-Insensitive circuits. MEMOCODE 2009*: 171-180
12. Michael Pellauer, **Muralidaran Vijayaraghavan**, Michael Adler, Arvind, Joel S. Emer: *A-Ports: an efficient abstraction for cycle-accurate performance models on FPGAs*. FPGA 2008: 87-96
13. Michael Pellauer, **Muralidaran Vijayaraghavan**, Michael Adler, Arvind, Joel S. Emer: *Quick Performance Models Quickly: Closely-Coupled Partitioned Simulation on FPGAs*. ISPASS 2008: 1-10
14. Kermin Fleming, Myron King, Man Cheuk Ng, Asif Khan, **Muralidaran Vijayaraghavan**: *High-throughput Pipelined Mergesort*. MEMOCODE 2008: 155-158
15. Man Cheuk Ng, **Muralidaran Vijayaraghavan**, Nirav Dave, Arvind, Gopal Raghavan, Jamey Hicks: *From WiFi to WiMAX: Techniques for High-Level IP Reuse across Different OFDM Protocols*. MEMOCODE 2007: 71-80
16. Nirav Dave, Kermin Fleming, Myron King, Michael Pellauer, **Muralidaran Vijayaraghavan**: *Hardware Acceleration of Matrix Multiplication on a Xilinx FPGA*. MEMOCODE 2007: 97-100

Patents

Michal Karczmarek, Arvind Mithal, **Muralidaran Vijayaraghavan**: *Hardware synthesis from multicycle rules*, Patent number: 8350594, Filed: November 9, 2009, Date of Patent: January 8, 2013, Assignee: MIT

Honours and Awards

- MEMOCODE design contest winner 2007, 2008, 2009, 2010
- All India Rank 15 in the Joint Entrance Examination for admission into IITs, June 2002
- Highest GPA in the Department of Computer Science at IIT Madras, June 2003