Xiangyao Yu

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32-G826, 32 Vassar Street
Cambridge, MA 02139, U.S.A.

RESEARCH INTERESTS

Computer Architecture, Databases, Distributed Systems

EDUCATION

Massachusetts Institute of Technology 2015 - 2017 (expected)
Ph.D., Electrical Engineering & Computer Science
Advisor: Srinivas Devadas

Massachusetts Institute of Technology 2012 - 2015
M.S., Electrical Engineering & Computer Science
Advisor: Srinivas Devadas

Tsinghua University, China 2008 - 2012
B.S., Microelectronics

PUBLICATIONS

1. **Xiangyao Yu**, Hongzhe Liu, Ethan Zou, Srinivas Devadas, "Tardis 2.0: Optimized Time Traveling Coherence for Relaxed Consistency Models", Proceedings of the 25th International Conference on Parallel Architectures and Compilation Techniques (***PACT***), September 2016.

2. **Xiangyao Yu**, Andrew Pavlo, Daniel Sanchez, Srinivas Devadas, "TicToc: Time Traveling Optimistic Concurrency Control", Proceedings of ***SIGMOD***, June 2016.

3. Rachata Ausavarungnirun, Chris Fallin, **Xiangyao Yu**, Kevin Chang, Greg Nazario, Reetuparna Das, Gabriel Loh, and Onur Mutlu, "A Case for Hierarchical Rings with Deflection Routing: An Energy-Efficient On-Chip Communication Substrate", Parallel Computing (***PARCO***), Volume 54, May 2016.

4. **Xiangyao Yu**, Christopher Hughes, Nadathur Satish, Srinivas Devadas, "IMP: Indirect Memory Prefetcher", Proceedings of the 48th International Symposium on Microarchitecture (***MICRO***), December 2015.

5. **Xiangyao Yu**, Srinivas Devadas, "Tardis: Time Traveling Coherence Algorithm for Distributed Shared Memory", Proceedings of the 24th International Conference on Parallel Architectures and Compilation Techniques (***PACT***), October 2015. **Best Paper Session.**

6. **Xiangyao Yu**, Syed Kamran Haider, Ling Ren, Christopher Fletcher, Albert Kwon, Marten van Dijk, Srinivas Devadas, "PrORAM: Dynamic Prefetcher for Oblivious RAM", International Symposium on Computer Architecture (***ISCA***), June 2015.

7. **Xiangyao Yu**, George Bezerra, Andrew Pavlo, Srinivas Devadas, and Michael Stonebraker, "Staring into the Abyss: An Evaluation of Concurrency Control with One Thousand Cores", Proceedings of the ***VLDB*** Endowment, vol. 8, iss. 3, November 2014.

8. Rachata Ausavarungnirun, Chris Fallin, **Xiangyao Yu**, Kevin Chang, Greg Nazario, Reetuparna Das, Gabriel Loh, and Onur Mutlu, "Design and Evaluation of Hierarchical Rings with Deflection Routing", Proceedings of the 26th International Symposium on Computer Architecture and High Performance Computing (***SBAC-PAD***), October 2014.

9. Christopher Fletcher, Ling Ren, **Xiangyao Yu**, Marten van Dijk, Omer Khan, and Srinivas Devadas, "Suppressing the Oblivious RAM Timing Channel While Making Information Leakage and Program Efficiency Trade-offs", Proceedings of the Int'l Symposium on High Peformance Computer Architecture (***HPCA***), February 2014.

10. **Xiangyao Yu**, Christopher Fletcher, Ling Ren, Marten Van Dijk, and Srinivas Devadas, "Generalized External Interaction with Tamper-Resistant Hardware with Bounded Information Leakage", Proceedings of the Cloud Computing Security Workshop (***CCSW***), November 2013

11. Emil Stefanov, Marten van Dijk, Elaine Shi, Christopher Fletcher, Ling Ren, **Xiangyao Yu**, and Srinivas Devadas, "Path ORAM: An Extremely Simple Oblivious RAM Protocol", Proceedings of the 20th Computer and Communication Security Conference (***CCS***), 2013. **Best Student Paper Award.**

12. Ling Ren, Christopher W. Fletcher, **Xiangyao Yu**, Marten van Dijk, and Srinivas Devadas, "Integrity Verification for Path Oblivious-RAM", Proceedings of the 17th IEEE High Performance Extreme Computing Conference (***HPEC***), 2013 (to appear)

13. Ling Ren, **Xiangyao Yu**, Christopher W. Fletcher, Marten van Dijk, Srinivas Devadas, "Design Space Exploration and Optimization of Path Oblivious RAM in Secure Processors", 40th International Symposium on Computer Architecture (***ISCA***), 2013

14. Yuan Lin Yeoh, Bo Wang, **Xiangyao Yu**, Tony Tae Hyoung Kim, "A 0.4V 7T SRAM with Write Through Virtual Ground and Ultra-fine Grain Power Gating Switches." IEEE International Symposium on Circuits and Systems (***ISCAS***), 2013

15. Chris Fallin, Greg Nazario, **Xiangyao Yu**, Kevin Chang, Rachata Ausavarungnirun, Onur Mutlu. "MinBD: Minimally- Buffered Deflection Routing for Energy-Efficient Interconnect." In 6th ACM/IEEE International Symposium on Networks-on-Chip (***NOCS***), 2012.

UNDER SUBMISSION/PREPARATION

1. **Xiangyao Yu**, Yu Xia, Daniel Sanchez, Andrew Pavlo, Larry Rudolph, Srinivas Devadas, "Sundial: Distributed Time Traveling Concurrency Control with Dynamic Data Caching", ***SIGMOD'17.***

2. **Xiangyao Yu**, Christopher Hughes, Nadathur Satish, Onur Mutlu, Srinivas Devadas, "Banshee: Bandwidth-Efficient DRAM Caching Via Software/Hardware Cooperation", ***ISCA'17.***

3. **Xiangyao Yu**, Siye Zhu, Justin Kaashoek, Andrew Pavlo, Srinivas Devadas, "Parallel Logging with Fine-Grained Dependency Tracking", ***VLDB'17***, in preparation.

TALKS

Tardis 2.0: Optimized Time Traveling Coherence for Relaxed Consistency Models

1. Conference talk at PACT, Haifa, Israel, September 2016

TicToc: Time Traveling Optimistic Concurrency Control

1. Intel Science and Technology Center for Big Data (ISTC-BD), Hillsboro, OR, August 2016
2. Conference talk at SIGMOD, San Francisco, CA, June 2016
3. Huawei, Santa Clara, CA, June 2016
4. North East Database Day (NEDB), MIT, January 2016

Time Traveling Cache Coherence and Concurrency Control

1. Intel, Santa Clara, CA, June 2016
2. Huawei, Santa Clara, CA, June 2016
3. Brown University, February 2016
4. Harvard University, February 2016
5. University of Massachusetts, Amherst, February 2016

IMP: Indirect Memory Prefetcher

1. Conference talk at MICRO, Honolulu, HI, December 2015
2. Intel, Santa Clara, CA, August 2014
3. Intel Science and Technology Center for Big Data (ISTC-BD), Hillsboro, OR, August 2014

Tardis: Time Traveling Coherence Algorithm for Distributed Shared Memory

1. Conference talk at PACT, San Francisco, CA, October 2015

Staring into the Abyss: An Evaluation of Concurrency Control with One Thousand Cores

1. Conference talk at VLDB, Kohala Coast, HI, September 2015
2. MIT cloud workshop, MIT, September 2014
3. CSAIL Alliance Program (CAP) annual meeting, MIT, May 2014
4. Poster at New England Database Day (NEDB), MIT, January 2014
5. Poster at Intel Science and Technology Center for Big Data (ISTC-BD), Santa Clara, CA, December 2013

Generalized External Interaction with Tamper-Resistant Hardware with Bounded Information Leakage

1. Conference talk at CCSW, Berlin, Germany, November 2013

Design Space Exploration and Optimization of Path Oblivious RAM in Secure Processors

1. IBM China Research Lab, Beijing, China, August 2013
2. Conference talk at ISCA, Tel-Aviv, Israel, June 2013

TEACHING AND MENTORSHIP

MIT, 6.004 Computation Structures
Teaching Assistant — Fall 2016
Instructors: Chris Terman, Silvina Hanono Wachman

MIT, 6.046/18.410 Design and Analysis of Algorithms
Teaching Assistant — Spring 2015
Instructors: Erik Demaine, Srini Devadas, Nancy Lynch

Students mentored

1. Quan Nguyen, PhD student. Project: Synchronization in Timestamp-Based Cache Coherence Protocols.
2. Yu Xia, PhD student. Project: Distributed Transaction Processing with Efficient Fault Tolerance.
3. Isaac Grosof, Undergraduate Research Opportunities Program (UROP). Project: A proof of Correctness for the Tardis Cache Coherence Protocol.
4. Siye Zhu and Justin Kaashoek, High school students (MIT PRIMES). Project: Parallel Logging with Fine-Grained Dependency Tracking
5. Ethan Zou and Henry Liu, High school students (MIT PRIMES). Project: Tardis 2.0: Optimized Time Traveling Coherence for Relaxed Consistency Models.
6. Nathan Wolfe and Ethan Zou, High school students (MIT PRIMES). Project: Optimizing Path ORAM for Cloud Storage Applications.

WORK EXPERIENCE

Parallel Computing Lab, Intel Jun 2014 - Aug 2014
full-time intern, Manager: Dr. Pradeep Dubey
Project: Graph algorithm scalability

Mobile And Sensing System Group, Microsoft Research Asia Oct 2011 - Jun 2012
full-time intern, Mentor: Dr. Thomas Moscibroda
Project: Task scheduling on mobile phone, service allocation in datacenter

ECE, Carnegie Mellon University Jun 2011 - Sep 2011
research summer intern, Advisor: Dr. Onur Mutlu
Project: Energy-efficient hierarchical ring on-chip interconnect

Hulu, Beijing Aug 2009 - Feb 2010
part-time intern, Manager: Dr. Zhibing Wang
Project: Search tracking service

PATENTS

Hardware prefetcher for indirect access patterns
Xiangyao Yu, Christopher J. Hughes, Nadathur Rajagopalan Satish
US 20160188476

Service Allocation in a Distributed Computing Platform
Thomas Moscibroda, Zhengping Qian, Mark Eugene Russinovich, **Xiangyao Yu**, Jiaxing Zhang, Feng Zhao
US 20160188476

HONORS

1. Presented in the best paper session in PACT 2015 October 2015
2. CCS13 Best Student Paper Award November 2013
3. Energy initiative fellowship 2012 - 2013
4. Graduation with honors from Tsinghua University June 2012
5. 1st class prize for scientific research at Tsinghua University September 2010

6. 1st prize in 28th Challenge Cup at Tsinghua University — April 2010
7. Comprehensive scholarship — 2009 - 2012
8. 3rd prize in 21st International Young Physicists' Tournament (IYPT) — June 2008

REFERENCE (ALPHABETICAL)

Srinivas Devadas (advisor)
Professor of EECS
Massachusetts Institute of Technology
devadas@mit.edu

Christopher Hughes
Researcher at Parallel Computing Lab
Intel Corporation
christopher.j.hughes@intel.com

Andrew Pavlo
Assistant Professor of Computer Science
Carnegie Mellon University
pavlo@cs.cmu.edu

Daniel Sanchez
Assistant Professor of EECS
Massachusetts Institute of Technology
sanchez@csail.mit.edu

Michael Stonebraker
Adjunct Professor of EECS
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stonebraker@csail.mit.edu