Kermin Fleming

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Research Interests

I am interested in all aspects of high-performance hardware design, especially implementations involving reconfigurable logic. I believe that reconfigurable logic offers an attractive power-performance that can be brought to bear on many future workloads, particularly as we move towards mobile and human-oriented tasks. However, current reconfigurable logic has a long way to go before this goal can be realized. To this end I am interested in developing tools that leverage high-level properties of hardware programs and that simplify integrating reconfigurable logic with traditional architectures.

Education

- **Massachusetts Institute of Technology**, Cambridge, MA — October. 2012
  Ph.D. in Electrical Engineering and Computer Science — GPA: 5.0/5.0
  Title: Scalable Reconfigurable Computation
  Advisor: Arvind, Joel Emer
- **Carnegie Mellon University**, Pittsburgh, PA — May 2006
  M.S. Electrical and Computer Engineering — GPA: 4.0/4.0
  B.S. Electrical and Computer Engineering — GPA: 4.0/4.0
  B.S. Computer Science — GPA: 4.0/4.0

Research Experience

- **Multiple FPGA Compiler** — 2011 – present
  Thesis Topic
  Computer Science and Artificial Intelligence Laboratory, MIT

  High-level synthesis tools and modular, parametric design have enabled designers to express concisely express scalable designs. However, the physical realization of these programs is generally constrained to a single FPGA, even if the program itself scales descriptionally. In this work, I add a new latency-insensitive FIFO primitive to a commercial HDL. I use this primitive to automatically partition designs among platforms consisting of multiple FPGAs. Designs so partitioned may even outperform single FPGA implementations due to increased resource availability in the partitioned system. Currently this tool is being used internally at Intel and at MIT in three research groups. Advised by Joel Emer and Arvind.

- **AirBlue** — 2008 – 2012
  Computer Science and Artificial Intelligence Laboratory, MIT

  Wireless networks are increasingly interference limited, due to the high density of wireless devices; in order to improve performance in future wireless networks, many cross-layer protocols, which break the traditional OSI model, have been proposed. The AirBlue project seeks to provide a highly configurable, FPGA-based radio experimentation platform, expressly for testing cross-layer protocols, by providing protocol designers with full access to the PHY and MAC layers. I was involved in implementing the initial WiFi base band MAC and PHY. I subsequently implemented SoftPhy, which uses data from the forward error correction algorithm to differentiate between noise and interference. Recently, I have been involved in implementing a novel rateless transceiver using Spinal Codes. Advised by Arvind, Devavrat Shah, and Hari Balakrishnan

- **BlueSSD** — 2009 – 2013
  Computer Architecture , Seoul National University

  This project seeks to develop a high-performance Linux compatible, FPGA-based solid state disk. One objective of the SSD platform is to evaluate various hardware accelerators including compression and advanced error correction. A second objective is to provide a malleable substrate for developing driver software. Currently, I am in the process of developing an extensible controller for the SSD. Advised by Arvind, Jihong Kim (Seoul National University)

- **MD6** 2009
  Computer Science and Artificial Intelligence Laboratory, MIT

  MD6, a highly vector and thread parallel algorithm, was a submission to the SHA3 competition. My role consisted of evaluating the hardware and parallel software implications of various design decisions made by the algorithm design team. I suggested several modifications to the algorithm to simplify hardware implementation without compromising performance. Advised by Ron Rivest

- **H264 Decoder** 2006 – 2010
  Computer Science and Artificial Intelligence Laboratory, MIT

  H264 is a common kernel in most consumer audio/visual devices. For high-resolution video streams, the computational and memory loading of H.264 is very high, as a result H.264 has traditionally been implement in hardware. With another student, I implemented a base profile H.264 implementation. I developed an optimized cache hierarchy for the decoder, focusing on improving performance while reducing power consumption. The FPGA implementation of the H.264 decoder is capable of decoding HD streams in real-time. Advised by Arvind

Open Source Experience

- **LEAP FPGA Operating System** 2009 – present

  LEAP (Latency-insentive Environment for Application Programming) is set of open source tools intended to facilitate FPGA design and collaboration among diverse sets of hardware researchers. LEAP provides a virtual layer of devices interfaces, for example unboundedly large memory, on top of physical a FPGA. The intention of this project is to decouple the user program from the physical reality of the FPGA, much like the operating system in a normal computer.

- **GTKWave** 2007

  GTKWave is the pre-eminent open source waveform viewer. Unfortunately, it was originally written in C, and had become rather difficult to augment. I implemented the "waveform reload" feature of GTKWave. During the implementation, I converted GTKWave into an object-oriented program with context. This conversion was facilitated by writing a new back-end for the Tiny C Compiler, and has enable many subsequent augmentations to GTKWave . Project leader: Anthony Bybell

Teaching Experience

- **SNU 4541.763 – Complex Digital Systems for Software People** Fall 2009
  Teaching Assistant

  Continued development of FPGA based labs and added support for complex peripherals, such as DRAM.

- **MIT 6.375 – Complex Digital Systems** Spring 2009
  Teaching Assistant

  Developed FPGA based course labs including a functional (Simplified)MIPS processor. Mentored student hardware projects, including real-time packet inspection hardware
  (`http://csg.csail.mit.edu/6.375`)

- **MIT 6.823 – Computer Architecture** Fall 2007
  Teaching Assistant

  Developed new course laboratories using Pin tool to model various architectural features, created course exams, and assisted students with homework

- **SNU 4541.763 – Complex Digital Systems for Software People** Fall 2009
  Teaching Assistant

  Continued development of FPGA based labs and added support for complex peripherals, such as DRAM.

- **CMU 18.551 – Digital Communications and Signal Processing Systems** Spring 2006
  Laboratory Teaching Assistant

  Ported course laboratories to new DSP board, advised student DSP projects involving hardware and software co-design

Industrial Experience

- **Intel** Hudson, Massachusetts 2009 – present
  Software Engineer

  Continuing development of the LEAP FPGA operating system. Also contributed to development of high-performance, low-area memory systems for accelerators.
  (`http://asim.csail.mit.edu/`)

- **Nokia Research**, Cambridge, Massachusetts Summer 2007,2008
  Hardware Intern

  Developed a hardware implementation of turbo error correction codes. Re-architected the system data-flow, improving throughput by 5% while reducing design area by 15%.

- **Google**, Mountain View, California Summer 2006, 2007
  Software Intern, Summer of Code

  Implemented a two new data storage features for a massively parallel, distributed database project. With mentor, developed a full system test for the data warehouse portion of the database.

  For Summer of Code, I developed a compiler back-end to convert legacy C programs into a simple object-oriented format. Used the tool to convert the open-source waveform viewer GTKWave into an object-oriented format and added a wave form reload feature.

- **Lexmark** Lexington, Kentucky Summer 2004 – Summer 2006
  Firmware Intern

  Developed an multi-threaded, embedded debugging suite allowing developers to communicate with and control development hardware. Implemented a serial device driver for serial communications and a host for remote TCP/IP communication. Developed auto-alignment program, which was deployed on manufacturing line.

Awards and Honors

- Best Paper, ANCS 2010
- Intel PhD. Fellowship 2010, 2011
- MEMOCODE Hardware-Software Co-design Project Winner 2007, 2008, 2009
- Andrew Carnegie Scholar 2006
- E. M. Williams Student Award of Scholarship 2006
- Tau Beta Pi, Eta Kappa Nu, and Phi Beta Kappa National Honor Societies 2005,2006
- David T. Tuma Award for best undergraduate project 2005
- College Jeopardy! Champion 2004

Publications

Peer-Reviewed Conferences and Journals

- Sang Woo Jun, **Kermin Fleming**, Michael Adler, and Joel Emer. "ZIPIO: An Architecture for Application Specific Compression of Big Data." *International Symposium on Field Programmable Technology (FPT)*, December 2012.

- Peter Iannucci, **Kermin Fleming**, Jonathan Perry, Hari Balakrishnan, and Devavrat Shah. "A Hardware Spinal Decoder." *Architectures for Networking and Communication Systems(ANCS)*, October 2012.

- Jonathan Perry, Peter Iannucci, **Kermin Fleming**, Hari Balakrishnan, and Devavrat Shah. "Spinal Codes" *ACM SIGCOMM*, August 2012.
- **Kermin Fleming**, Michael Adler, Michael Pellauer, Angshuman Parashar, Arvind and Joel Emer. "Leveraging Latency-Insensitivity to Ease Multiple FPGA Design" *International Symposium on Field Programmable Gate Arrays (ISFPGA)*, February 2012.
- Sungjin Lee, Jihoon Park, **Kermin Fleming**, Arvind, Jihong Kim. "Improving Performance and Lifetime of Solid-state Drives Using Hardware-accelerated Compression " *IEEE Transactions on Consumer Electronics*, November 2011.
- Micheal Adler, **Kermin Fleming**, Angshuman Parashar, Micheal Pellauer, and Joel Emer. "LEAP Scratchpads: Automatic Memory and Cache Management for Reconfigurable Logic " *International Symposium on Field Programmable Gate Arrays (ISFPGA)*, February 2011.
- **Kermin Fleming**, Man Cheuk Ng, Samuel Gross, Hari Balakrishnan, and Arvind. "WiLIS: Architectural Modelling of Wireless Systems" *International Symposium on Performance Analysis of Systems and Software(ISPASS)*, April 2011.
- Man Cheuk Ng, **Kermin Fleming**, Mythili Vutukuru, Samuel Gross, Hari Balakrishnan, and Arvind. "Airblue: A System for Cross-Layer Protocol Development." *Architectures for Networking and Communications Systems (ANCS)*, October 2010. **Best Paper Award**
- **Kermin Fleming**, Chun-Chieh Lin, Nirav Dave, Gopal Raghavan, Jamey Hicks, and Arvind. "H.264 Decoder: A Case Study in Multiple Design Points." *Formal Methods and Models of Co-design (MEMOCODE)*, Jun. 2008.

Invited Papers and Workshops

- Angshuman Parashar, Micheal Adler, **Kermin Fleming**, Micheal Pellauer, and Joel Emer. "LEAP: A Virtual Platform Architecture for FPGAs " *Workshop on the Intersections of Architecture and Reconfigurable Logic (CARL)*, December 2010.
- Sungjin Lee, **Kermin Fleming**, Jihoon Park, Keonsoo Ha, Adrian Caulfield, Steven Swanson, Arvind, and Jihong Kim. "BlueSSD: An Open Platform for Cross-layer Experiments for NAND Flash-based SSDs" *Workshop on Architectural Research Prototyping (WARP)*, June 2010.
- Abhinav Agarwal, Nirav Dave, **Kermin Fleming**, Asif Khan, Myron King, Man Cheuk Ng, and Muralidaran Vijayaraghavan. "Implementing a Fast Cartesian-Polar Matrix Interpolator." *Formal Methods and Models of Co-design (MEMOCODE)*, Jul. 2009.
- Man Cheuk Ng and **Kermin Fleming** "AirBlue: A High Throughput and Low Latency Radio Prototyping Platform." *Design Automation and Test Europe (Poster Session) (DATE 2009)*, Aug. 2009.
- Ronald L. Rivet, Benjamin Agre, Daniel V. Bailey, Christopher Crutchfield, Yevgeniy Dodis, **Kermin E. Fleming**, Asif Khan, Jayant Krishnamurthy, Yucheng Lin, Leo Reyzin, Emily Shen, Jim Sukha, Drew Sutherland, Eran Tromer, Yiqun Lisa Yin "The MD6 Hash Function." `http://groups.csail.mit.edu/cis/md6/submitted-2008-10-27/Supporting_Documentation/md6_report.pdf` *Submission to NIST SHA-3 Competition*, Oct. 2008 .
- **Kermin Fleming**, Myron King, Man Cheuk Ng, Asif Khan and Muralidaran Vijayaraghavan. "High-throughput Pipelined Mergesort." *Formal Methods and Models of Co-design (MEMOCODE)*, Jun. 2008.
- Nirav Dave, **Kermin Fleming**, Myron King, Michael Pellauer, and Muralidaran Vijayaraghavan. "Hardware Acceleration of Matrix Multiplication on a Xilinx FPGA." *Formal Methods and Models of Co-design (MEMOCODE)*, May 2007.
- **Kermin Fleming** and Joel Emer. "Resource-efficient FPGA Content Addressable Memories." *Workshop on Architectural Research Prototyping (WARP)*, May 2007.

Under Review

- Hsin-Jung Yang, **Kermin Fleming**, Michael Adler, and Joel Emer. "Scaling With Moore's Law: Using Prefetching to Improve FPGA Performance." *submitted to Design Automation Conference (DAC)*, June 2013.

Patents

- **Kermin Fleming** and Peter Iannucci. 2012. "Spinal Decoder." U.S. Patent 61/651,336 filed May 24, 2012. Patent Pending.