Quan M. Nguyen

Contact Information

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Education

Ph.D., Massachusetts Institute of Technology — May 2022
Department of Electrical Engineering and Computer Science
Thesis Title: "Accelerating Irregular Applications with Pipeline Parallelism"
Adviser: Daniel Sanchez

S.M., Massachusetts Institute of Technology — June 2016
Department of Electrical Engineering and Computer Science
Thesis Title: "Synchronization in Timestamp-Based Cache Coherence Protocols"
Adviser: Srinivas Devadas

B.S., University of California, Berkeley — May 2014
Department of Electrical Engineering and Computer Sciences

Research Interests

Novel techniques at the **hardware/software interface** (i.e., **computer architecture**) to accelerate applications not well-served by conventional architectures (e.g., **irregular applications** with unpredictable control flow and data-dependent memory accesses)

Publications

"Phloem: Automatic Acceleration of Irregular Applications with Fine-Grain Pipeline Parallelism", **Quan Nguyen**, Daniel Sanchez, to appear, *Proceedings of the 29th International Symposium on High-Performance Computer Architecture* **(HPCA'23)**, February 2023

"Fifer: Practical Acceleration of Irregular Applications on Reconfigurable Architectures", **Quan Nguyen**, Daniel Sanchez, *Proceedings of the 54th International Symposium on Microarchitecture* **(MICRO'21)**, October 2021

"Pipette: Improving Utilization on Irregular Applications through Intra-Core Pipeline Parallelism", **Quan Nguyen**, Daniel Sanchez, *Proceedings of the 53rd International Symposium on Microarchitecture* **(MICRO'20)**, October 2020

"A Case for MVPs: Mixed-Precision Vector Processors", Albert Ou, **Quan Nguyen**, Yunsup Lee, Krste Asanović, *2nd International Workshop on Parallelism in Mobile Platforms (PRISM-2), at ISCA-41*, June 2014

Work Experience

Postdoctoral Associate, MIT — September 2022 – Present
Mentor: Daniel Sanchez
Department of Electrical Engineering and Computer Science

Research Intern, NVIDIA — June 2020 – August 2020
Explored pipeline parallelism on a novel explicit decoupled data-orchestrated architecture

Research Assistant, MIT — September 2014 – May 2022
Department of Electrical Engineering and Computer Science

Engineering Intern, Apple — June – August 2016
Modeled functional performance of next-generation iPhone and iPad processors

Undergraduate Research Assistant, UC Berkeley — June 2012 – June 2014
Department of Electrical Engineering and Computer Sciences

Teaching Experience

Teaching Assistant, MIT 6.004 (Computation Structures) Fall 2019
Introductory course in computer architecture
Led two recitations of approx. 20 students each, twice a week
Conducted three class-wide examination review sessions
Overhauled laboratory assignment for new hardware description language
Evaluation score: 6.9/7 with 33 responses

Teaching Assistant, MIT 6.175 (Constructive Computer Architecture) Fall 2016
Intermediate course in computer architecture
Led one recitation of approx. 20 students, once a week
Evaluation score: 6.7/7 with 13 responses

Laboratory Assistant, UC Berkeley CS 61C (Machine Structures) Fall 2011
Introductory course in computer architecture
Aided students with laboratory assignments

Honors and Awards

Irwin Mark Jacobs and Joan Klein Jacobs Presidential Fellow 2014
Massachusetts Institute of Technology

High Honors in Electrical Engineering and Computer Sciences 2014
University of California, Berkeley
(top ten percent of graduating class)

Hobbies

Lindy Hop: dancing East Coast Swing and teaching the next generation of dancers

SIGTBD: hosted MIT CSAIL's annual joke conference in 2021 and 2022

Minecraft: developing an automatic place-and-route tool for synthesis of Redstone circuits from Verilog

Bicycling: crossed the United States by bicycle (Massachusetts to Oregon via TransAmerica Trail) in the summer of 2022