About This Manual

Objectives of This Manual

The *DPEAC Reference Manual* describes the DPEAC instruction set, a macroinstruction facility used for programming the accelerator chip hardware of the Connection Machine CM-5 supercomputer. DPEAC is an extension of SUN-4 assembler code, providing additional assembly-level operations that are CM-5 specific.

This manual also describes **`dpas`**, an extension of the SUN-4 assembler **`as`**, which takes a file of DPEAC code, translates it into the corresponding assembly source code, and hands this resulting code to **`as`** for final assembly.

Intended Audience

This manual is intended to be read by experienced DPEAC programmers, and is not intended as either a tutorial or a programming guide. However, this document does contain numerous programming tricks and performance hints to help a knowledgeable programmer get the best performance from CM-5 DPEAC code.

Revision Information

This manual is a revision of a reference document, the *DPEAC Language Specification and dpas User's Guide*.

Organization of This Manual

Chapter 1 The DPEAC Instruction Set
Presents an overview of the purpose and structure of DPEAC.

Chapter 2 Accelerator Chip Memory Mapping
Describes how the accelerator chip hardware is mapped into the node memory of the CM-5.

Chapter 3 The DPEAC Instruction Set
Describes the basic types and syntax of DPEAC instructions.

Chapter 4 DPEAC Instruction Formats
Describes the five main DPEAC instruction formats.

Chapter 5 Instructions and Opcodes
Presents an overview of the entire DPEAC instruction set.

Chapter 6 Indirect VU Instruction Execution
Describes in more detail the technique of indirect (from memory) execution of DPEAC instructions.

Chapter 7 VU Arithmetic Instruction Set
Describes in more detail the arithmetic subset of the DPEAC instruction set.

Chapter 8 Lexical Directives
Describes the directives recognized by the internal source code preprocessor of **`dpas`**.

Chapter 9 Accelerator Chip Notes
Describes some of the inner workings of the accelerator chip, and how they relate to the execution of DPEAC code.

Chapter 10 Performance Considerations
Details key operation timings of the accelerator chip, and provides useful performance coding tips and efficient algorithms.

Chapter 11 dpas Assembler User's Guide
Describes the command line interface of **`dpas`**, the DPEAC assembler, and lists the switches it accepts.

Chapter 12 Sample DPEAC Routine
Presents a complete DPEAC routine that exemplifies the basic features of the instruction set.

Related Documents

- *SPARC RISC User's Guide*, (Austin, Texas: Ross Technology, Inc., 1990)
- The UNIX manual page for the **`as`** assembler

Notation Conventions

The table below displays the notation conventions observed in this manual.

Convention	Meaning
`bold typewriter`	DPEAC instructions, modifiers, and header file names, when they appear embedded in text. Also names of associated UNIX commands (such as **`dpas`** and **`as`**).
italics	Argument names and placeholders in function and command formats.
`typewriter`	Code examples and code fragments, where they appear separate from the main body of text.
`%` **`bold typewriter`** `regular typewriter`	In interactive examples, user input is shown in **`bold typewriter`** and system output is shown in `regular typewriter` font.