6.823 Computer Architecture	DUE: 2/27/2002, EXTENSION: 3/4/2002
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Problem Set 1	*Instructors: Krste Asanovic, Srinivas Devadas*

Problem 1

(a) We need to fetch $3 + 10 * 4 = 43$ instructions. In bytes, $6 + 10 * 8 = 86$ bytes. We need to fetch $10 * 4 = 40$ bytes of data memory and do not have to store anything.

(b) Assume R1: N, R2: a, R3: I, R4: sum, R5: condition register, R6: temporary register.

```
xorl    %eax,%eax                 XOR     R3,R3,R3
cmpl    %ebx,%eax                 SUB     R6,R3,R1
jge     .L4                       SLTI    R5,R6,#1
                                  BNEZ    R5, .L4
addl    (%ecx,%eax,4),%edx        SLLI    R6,R3,#2
                                  ADD     R6,R6,R2
                                  LW      R6,0(R6)
                                  ADD     R4,R4,R6
cmpl    %ebx,%eax                 SUB     R6,R3,R1
jl      .L6                       SGTI    R5,R6,#0
                                  BNEZ    R5,.L6
```

(c) If every DLX instruction uses 4 bytes then we will have to fetch $(4 + 10 * 8) * 4 = 256$ bytes. We need to fetch the same amount of data memory, 40 bytes and store 0 bytes. We see that problem **1.A** is more efficient because we only have 1/3 bytes of instructions.

(d) Assume: R1: N, R2: a, R3: I, R4: sum, R5: Conditional register, R6: temp

```
        SLLI    R1,R1,#2        # Get 4*N...
        ADD     R1,R1,R2        # ...to set N = a + 4*N
        SLT     R5,R2,R1
        BEQZ    R5,.L4
.L6:
        LW      R6,0(R2)        # sum += a[I]
        ADD     R4,R4,R6
        ADDI    R2,R2,#4        # a += 4
        SLT     R5,R2,R1
        BNEZ    R5,.L6
.L4:
```

Therefore we would have $(5 + 10 * 4) * 4 = 216$ bytes of instructions to fetch and we need to fetch $10 * 4 = 40$ bytes of data memory and do not have to store anything. Therefore we do a lot better then in problem **1.B** but still worse than in problem **1.A**. On the other hand we do not have so many micro instructions.