6.823 Computer Architecture	DUE: 2/27/2002, EXTENSION: 3/4/2002
Timothy Danford, Killian Pohl, Bryan Russell	
Problem Set 1	*Instructors: Krste Asanovic, Srinivas Devadas*

Problem 4

(a) From problem **1.D**, only 1 temporary register is required (namely $R6$). For $n = 10$, there are $5 * 10 + 4 = 54$ dynamic instructions (instructions executed at run-time).

(b) Using the indirect addressing-mode for arithmetic instructions, we get the following code sequence:

```
        SLLI    R1,R1,#2        # Get 4*N...
        ADD     R1,R1,R2        # ...to set N = a + 4*N
        SLT     R5,R2,R1
        BEQZ    R5,.L4
.L6:
        ADD     R4,(R2)         # sum += *(a)
        ADDI    R2,R2,#4        # a += 4
        SLT     R5,R2,R1
        BNEZ    R5,.L6
.L4:
```

Now, we do not use any temporary registers (we only use $R1 - R4$ and the condition register $R5$). We now have $4 * 10 + 4 = 44$ dynamic instructions for this code sequence.

(c) Using the auto-increment addressing-mode for arithmetic instructions, we get the following code sequence:

```
        SLLI    R1,R1,#2        # Get 4*N...
        ADD     R1,R1,R2        # ...to set N = a + 4*N
        SLT     R5,R2,R1
        BEQZ    R5,.L4
.L6:
        ADD     R4,(R2)+        # sum += *(a); a += d;
        SLT     R5,R2,R1
        BNEZ    R5,.L6
.L4:
```

Again, we do not use any temporary registers. We now have $3 * 10 + 4 = 33$ dynamic instructions for this code sequence.

(d) To add indirect addressing, we need to add a datapath from the "A" register in the Execution (EX) stage to the registers between the Execution and Memory access (MEM) stages and add an ALU in the MEM stage. The input to be added ALU in the MEM stage would be the forwarded "A" register and the output from the Data Memory. The result would then be written back to the Register ("A") in the Write Back (WB) pipe stage.

To add auto-increment addressing, we would need the above plus an additional ALU in the MEM pipe stage (2 ALUs in total in the MEM pipe stage). The second ALU would take the register holding the address and add the constant "d" to it. Then the output from both ALUs would then be written to the Registers in the WB pipe stage.

For both cases, we might encounter timing issues. By adding the ALU operation after the data memory read, we increase the amount of time that needs to be spent in the MEM pipe stage. To fix this, we may have to change the clock speed which will cause the overall pipeline to slow down.