6.823 Computer Architecture DUE: 5/8/2002

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Problem Set 6 *Instructors: Krste Asanovic, Srinivas Devadas*

Problem 2

(a) (b)

initial state	cached	ops	actions	final state	this cache	other caches	mem
cleanExclusive	no	none	none	CE	X		X
		CPU read	none	CE	X		X
		CPU write	none	OE	X		
		replace	none	I			X
		CR	none	CS	X	X	X
		CRI	none	I		I	
		CI	none	Impossible			
		WR	none	Impossible			
		CWI	none	I			X

initial state	cached	ops	actions	final state	this cache	other caches	mem
ownedExclusive	no	none	none	OE	X		
		CPU read	none	OE	X		
		CPU write	none	OE	X		
		replace	WR	I			X
		CR	CCI	OS	X	X	
		CRI	none	I		X	
		CI	none	Impossible			
		WR	none	Impossible			
		CWI	none	I			X

initial state	cached	ops	actions	final state	this cache	other caches	mem
cleanShared	no	none	none	CS	X		X
		CPU read	none	CS	X		X
		CPU write	CI	OE	X		
		replace	none	I			
		CR	none	CS	X	X	X
		CRI	none	I		X	
		CI	none	Impossible			
		WR	none	Impossible			
		CWI	none	I			X

initial state	cached	ops	actions	final state	this cache	other caches	mem
cleanShared	yes	none	same	CS	X	X	X
		CPU read	as	CS	X	X	X
		CPU write	above	OE	X		
		replace		I		X	X
		CR		CS	X	X	X
		CRI		I		X	
		CI		I		X	
		WR		CS	X	X	X
		CWI		I			X

initial state	cached	ops	actions	final state	this cache	other caches	mem
ownedShared	no	none	none	OS	X		
		CPU read	none	OS	X		
		CPU write	CI	OE	X		
		replace	WR	I			X
		CR	CCI	OS	X	X	
		CRI	none	I		X	
		CI	none	Impossible			
		WR	none	Impossible			
		CWI	none	I			X

initial state	cached	ops	actions	final state	this cache	other caches	mem
ownedShared	yes	none	same	OS	X	X	
		CPU read	as	OS	X	X	
		CPU write	above	OE	X		
		replace		I		X	X
		CR		OS	X	X	
		CRI		I		X	
		CI		I		X	
		WR		OS	X	X	
		CWI		I			X

Note: We also talked to Henry Atkins about this problem.