Thomas Bourgeat

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Education and Internships

Fall 2015–2022 **PhD**, *MIT*, Cambridge.
Formal specification and hardware design with Arvind and Adam Chlipala

Summer 2018 **Internship**, *NVidia*, Westford.
Data Orchestration on GPU

Summer 2017 **Internship**, *NVidia*, Santa Clara.
Weak Memory Model testing

April – August 2015 **Internship**, *UPC*, Barcelona.
Process mining of asynchronous circuits, with J. Cortadella

April – August 2014 **Internship**, *MIT*, Boston.
Rule-Based Hardware Design with Arvind

2013–2015 **Master**, *Université Paris Diderot and ENS Ulm*, Paris, MPRI.

June – August 2013 **Internship**, *INRIA*, Rennes.
Algorithms and protocols with the LPN problem, with P-A. Fouque

2012 – 2013 **BS**, *ENS Ulm*, Paris.
Bachelor Degree in Computer Science

Papers

ASPLOS2022 **DAGguise: Mitigating Memory Timing Side Channels**.
Peter W. Deutsch, Yuheng Yang, Thomas Bourgeat, Jules Drean, Joel Emer, Mengjia Yan

ISCA2021 **FlexMiner: A Pattern-Aware Accelerator for Graph Pattern Mining**.
Xuhao Chen, Tianhao Huang, Shuotao Xu, Thomas Bourgeat, Chanwoo Chung, Arvind

ICRA2021 **Accelerating Robot Dynamics Gradients: Hardware-Sofware Co-Design on a CPU, GPU, and FPGA**.
Brian Plancher, Sabrina Neuman, Thomas Bourgeat, Scott Kuindersma, Srini Devadas, Vijay Janapa Reddi

CoqPL2021 **An experience report on writing usabe DSLs in Coq**.
Clément Pit-Claudel, Thomas Bourgeat

ASPLOS2021 **Effective Simulation and Debugging for High-Level Hardware Languages Using Software Compilers**.
Clément Pit-Claudel, Thomas Bourgeat, Stella Lau, Arvind, Adam Chlipala

ASPLOS2021 **Robomorphic Computing: A Design Methodology for Domain-Specific Accelerators Parameterized by Robot Morphology**.
Sabrina M. Neuman, Brian Plancher, Thomas Bourgeat, Thierry Tambe, Srini Devadas, Vijay Janapa Reddi

MICRO2020 **CaSA: End-to-end Quantitative Security Analysis of Randomly Mapped Caches**.
Thomas Bourgeat, Jules Drean, Yuheng Yang, Lillian Tsai, Joel Emer, Mengjia Yan

MICRO2020 **AQUOMAN An Analytic-Query Offloading Machine**.
Shuotao Xu, Thomas Bourgeat, Tianhao Huang, Hojun Kim, Sungjin Lee, Arvind

PLDI2020 **The essence of Bluspec: a core language for rule-based hardware design**.
Thomas Bourgeat, Clément Pit-Claudel, Adam Chlipala, Arvind

MICRO2019 **MI6: Secure Enclaves in a Speculative Out-of-Order Processor**.
Thomas Bourgeat, Ilia A. Lebedev, Andrew Wright, Sizhuo Zhang, Arvind, Srini Devadas

MICRO2018 **Composable Building Blocks to Open up Processor Design**.
Sizhuo Zhang, Andrew Wright, Thomas Bourgeat, Arvind

ASYNC2016 **Specification mining for asynchronous controllers**.
Javier San Pedro, Thomas Bourgeat, Jordi Cortadella

Draft-2014 **A probabilistic Hadwiger-Nelson problem**.
Thomas Bourgeat, Paul Melotti, Marc Heinrich

SEC2014 **New Algorithmic Approaches to Point Constellation Recognition**.
Thomas Bourgeat, Julien Bringer, Herve Chabanne, Robin Champenois, Jeremie Clement, Houda Ferradi, Marc Heinrich, Paul Melotti, David Naccache, Antoine Voizard

Teaching experiences

- Teaching assistant for Computation Structures (6.S084 that became 6.004), at MIT (Spring 2018)
- Teaching assistant for Constructive Computer Architecture (6.175), at MIT (Fall 2017)
- Teaching assistant in Maths and Computer Science, at Lycee Saint-Louis (2013-2015)

Committees

- OOPSLA 2022 External Reviewing Committee

Languages

English Fluent

French Mother tongue