

RAW HANDHELD BOARD

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PROJECT NAME: AMP

SCHEMATIC NAME:

RAW\_HANDHELD

RAW

REV#=1.0

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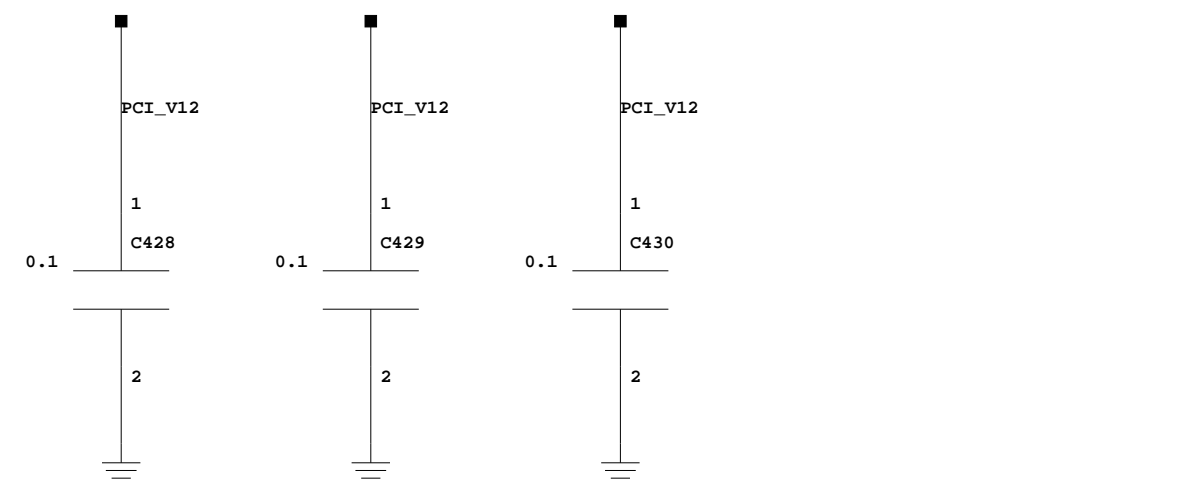
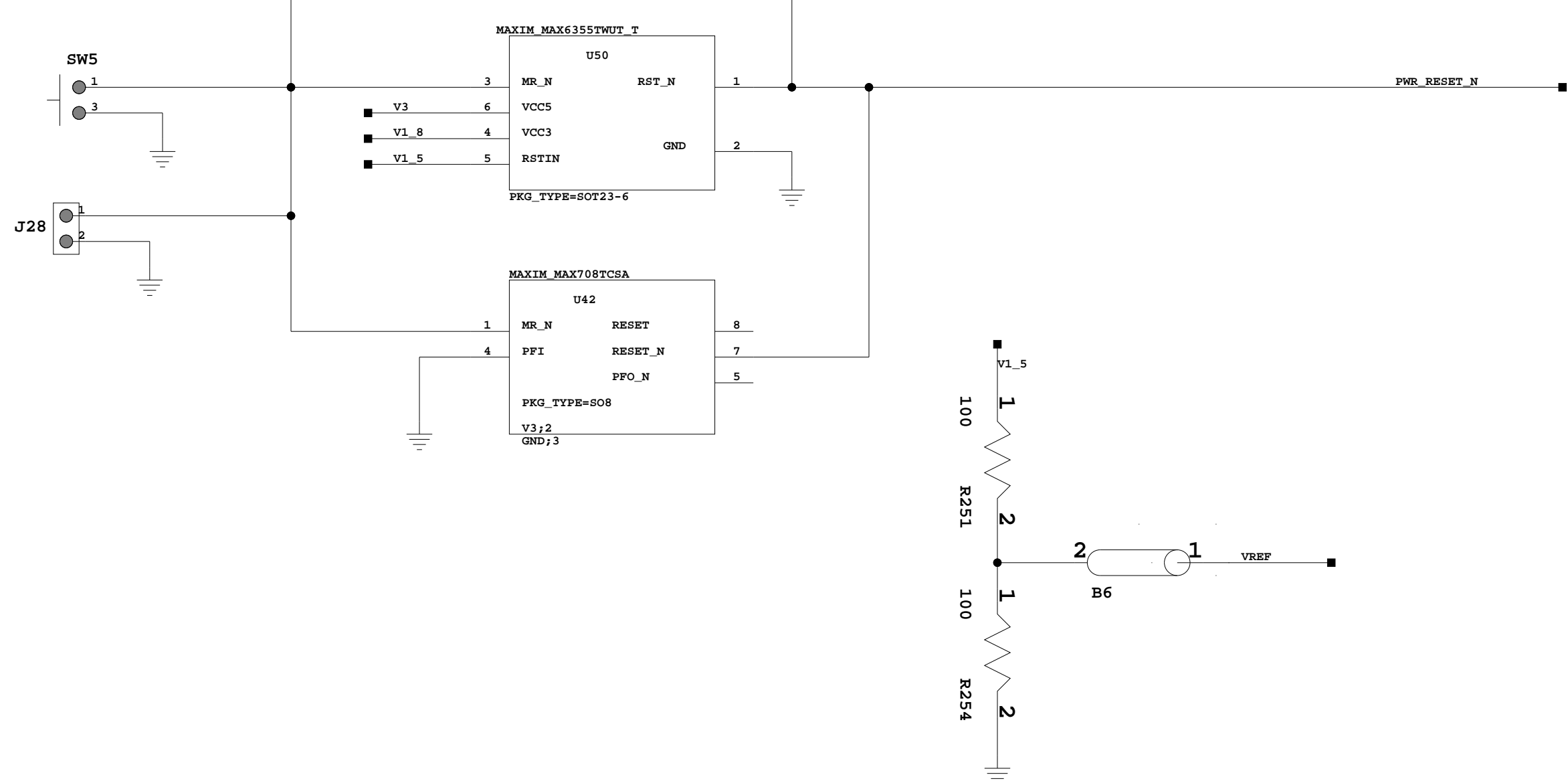
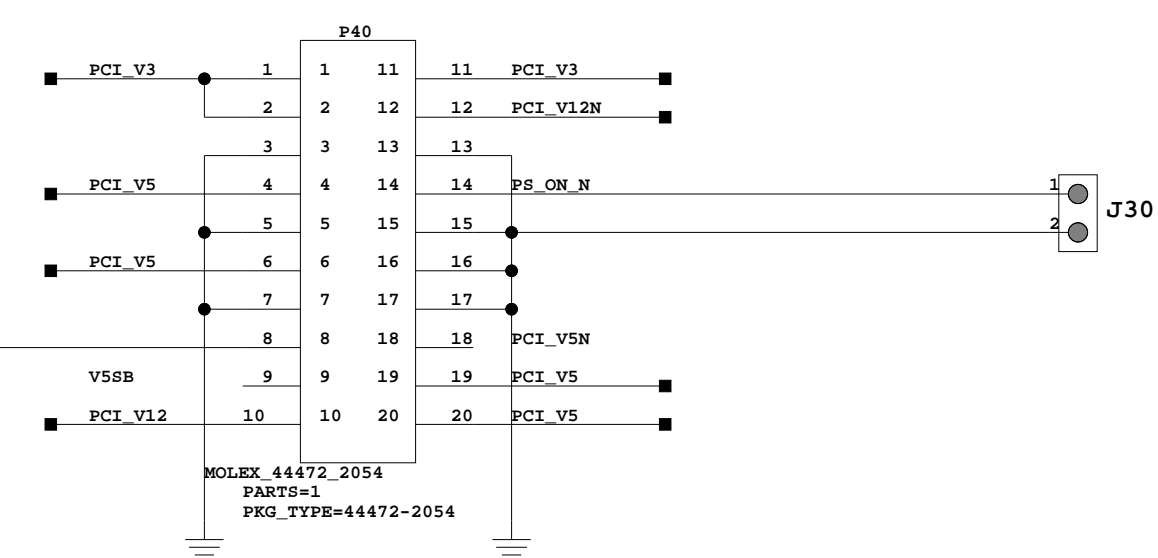
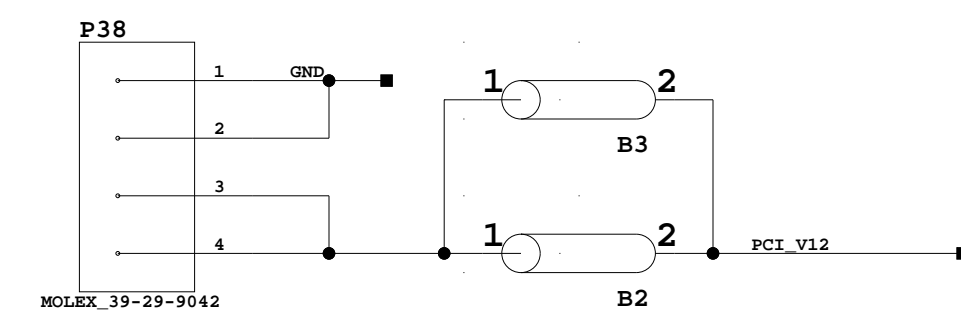
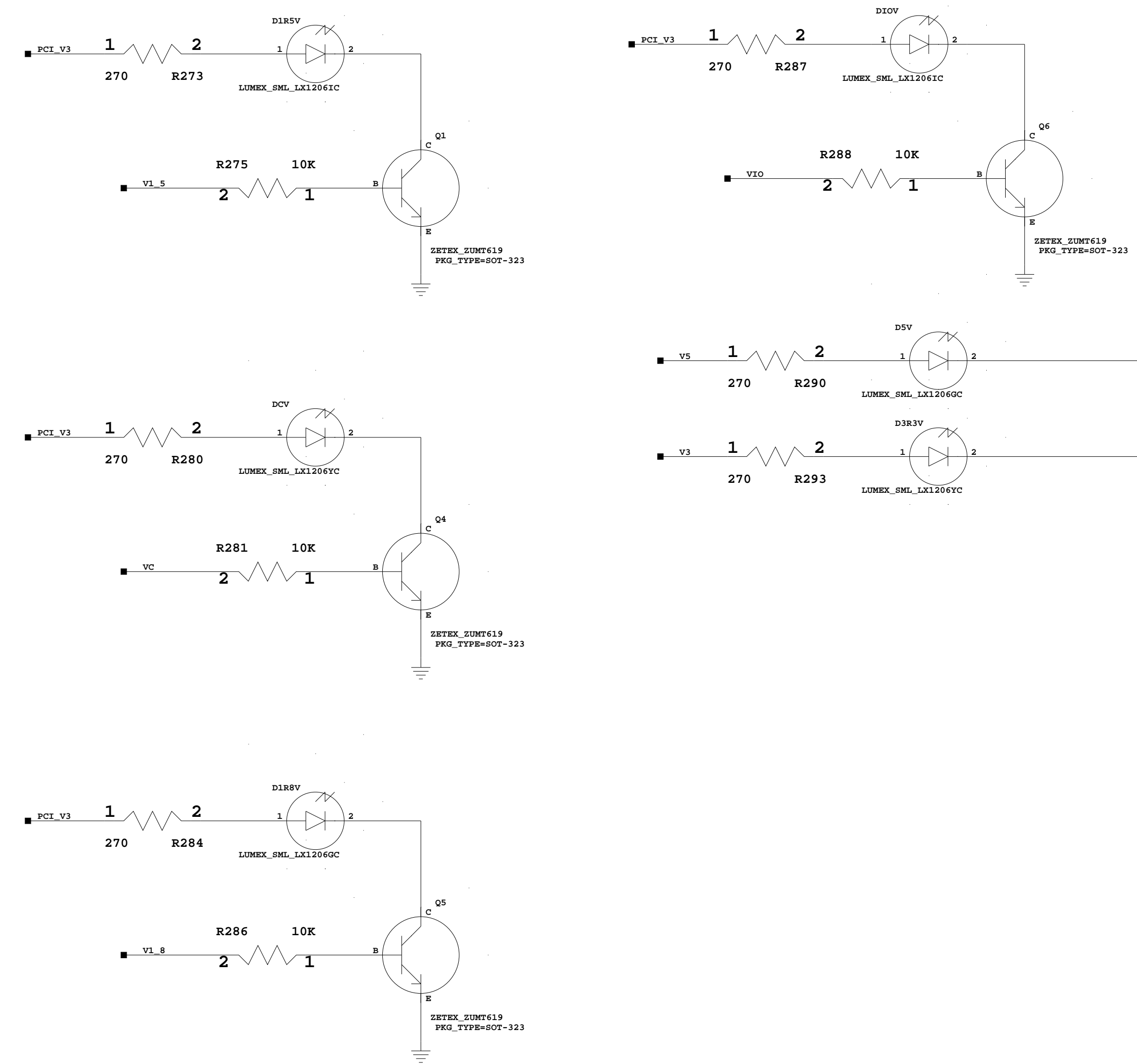
SHEET SIZE E

SHEET OR 30

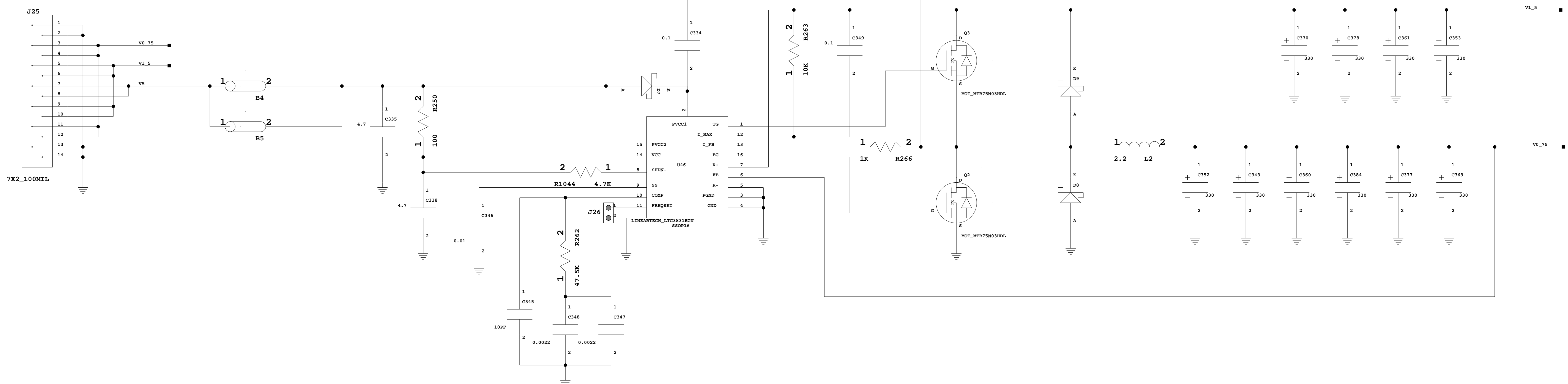




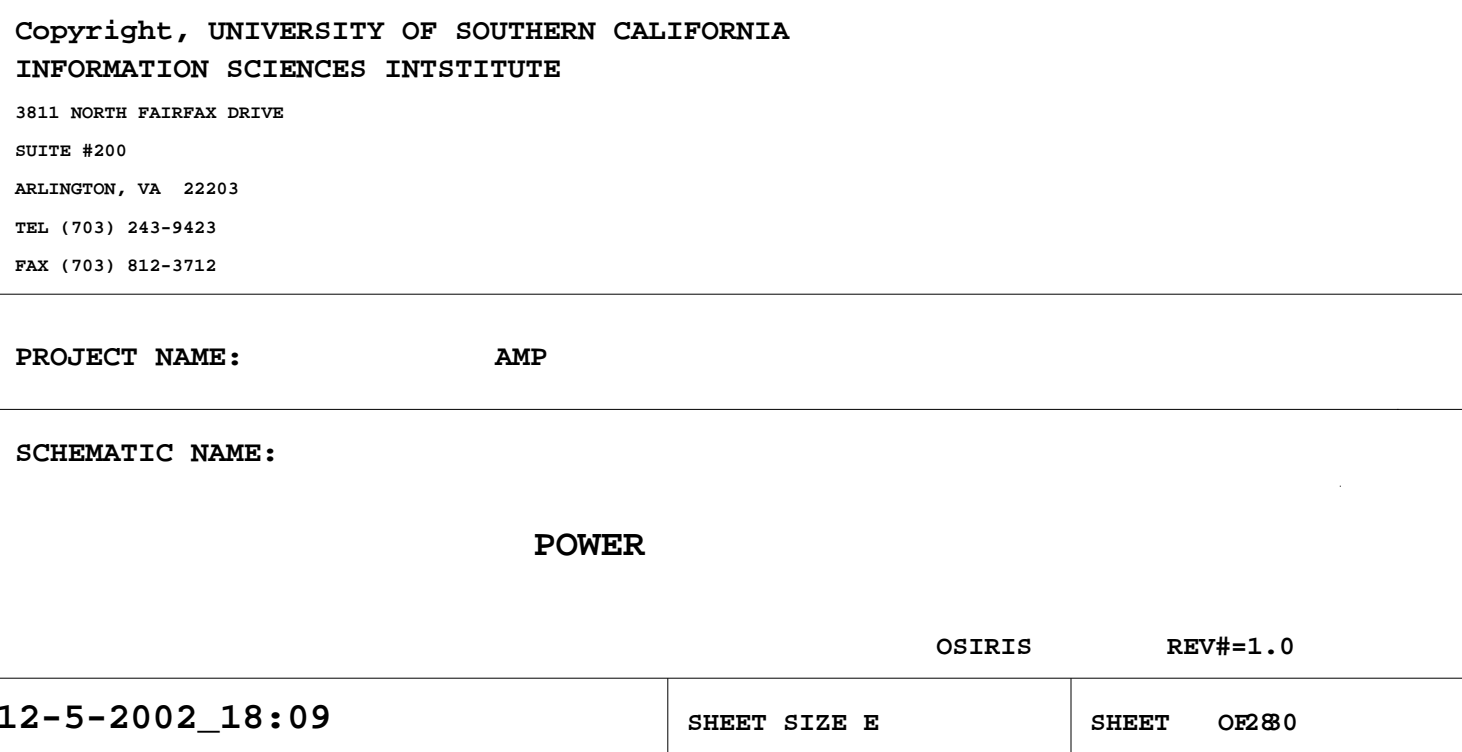




		P37			
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■	AMD	62	2	1	PCI_V12 ■
■	AMD	61	2	2	PCI_V12 ■
■	AMD	60	3	3	PCI_V12 ■
■	AMD	59	4	4	PCI_V12 ■
VMM	Reserved	58	5	5	Reserved
■	VYD0	57	6	6	Key
■	VYD0	56	7	7	VID0
■	VYD0	55	8	8	VID0 ■
VMM	Reserved	54	9	9	Reserved
VMM	OTDR	53	10	10	
■	VCF	52	11	11	AMD
Reserved	Reserved	51	12	12	Reserved
■	VCF	50	13	13	AMD
■	VCF	49	14	14	VCF ■
■	AMD	48	15	15	AMD
■	AMD	47	16	16	VCF
■	AMD	46	17	17	AMD
■	VCF	45	18	18	VCF
■	AMD	44	19	19	AMD
■	VCF	43	20	20	VCF
■	AMD	42	21	21	AMD
■	VCF	41	22	22	VCF
■	AMD	40	23	23	AMD
■	VCF	39	24	24	VCF
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■	VCF	37	26	26	VCF
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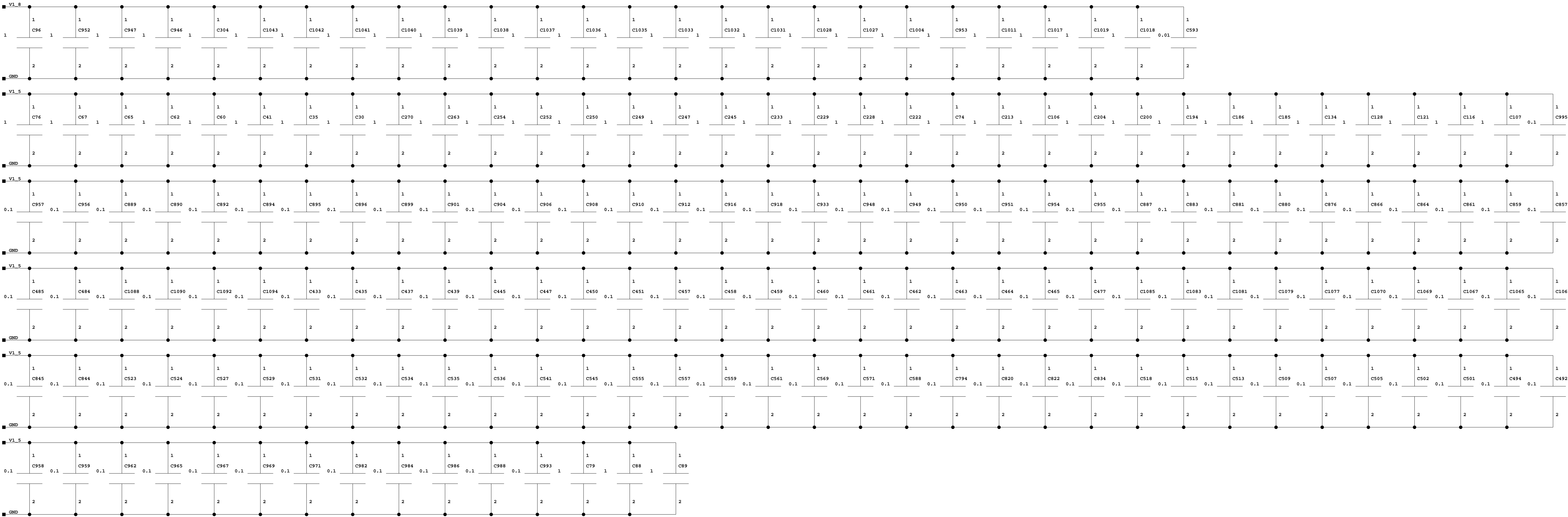
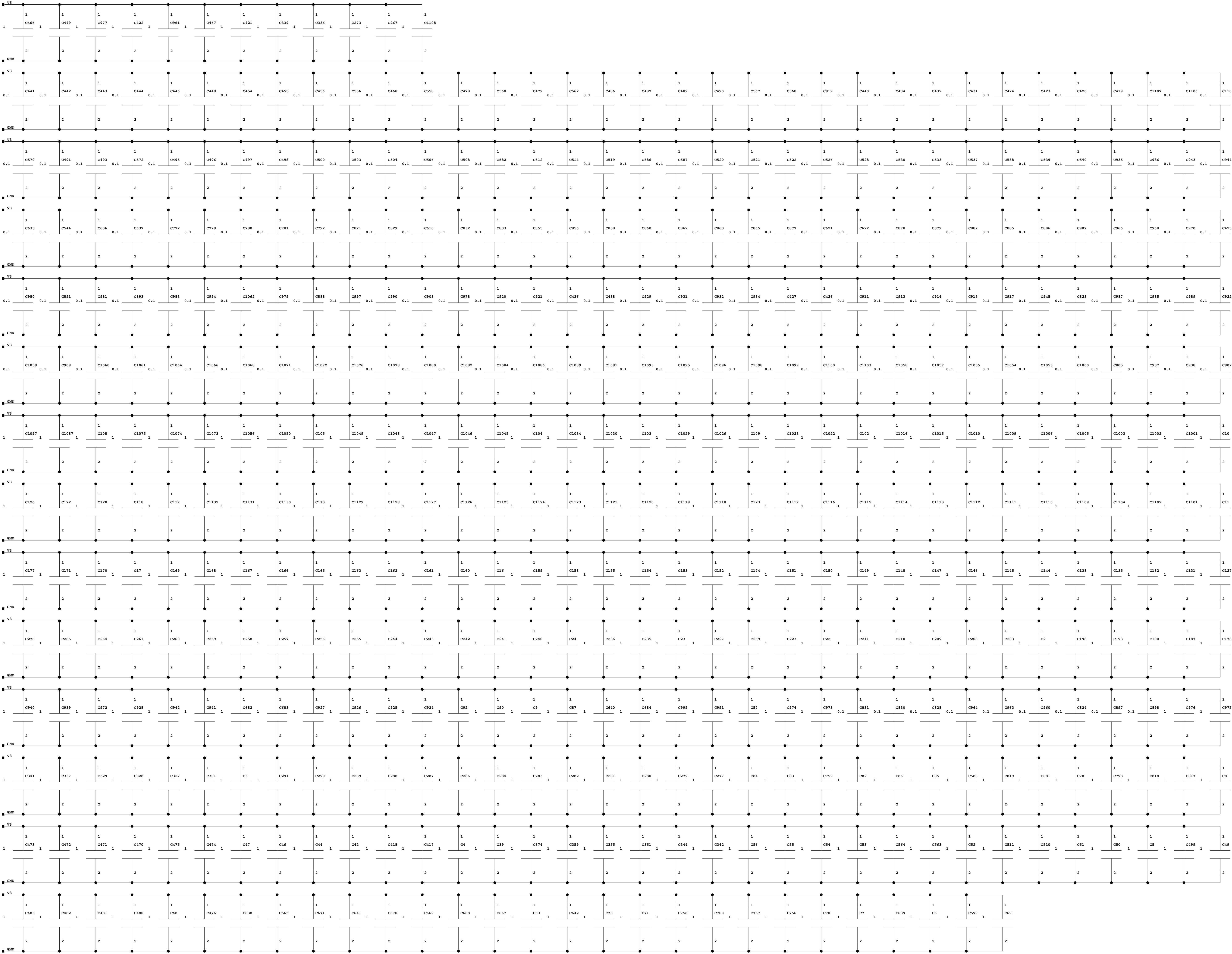




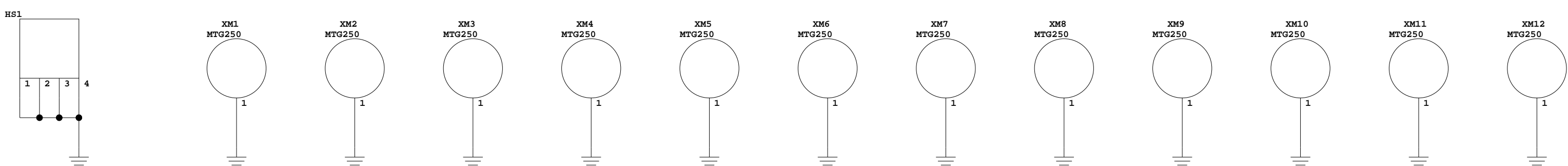




UTILITY 1/2



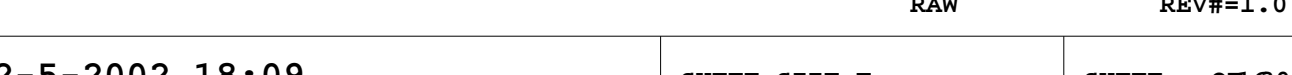




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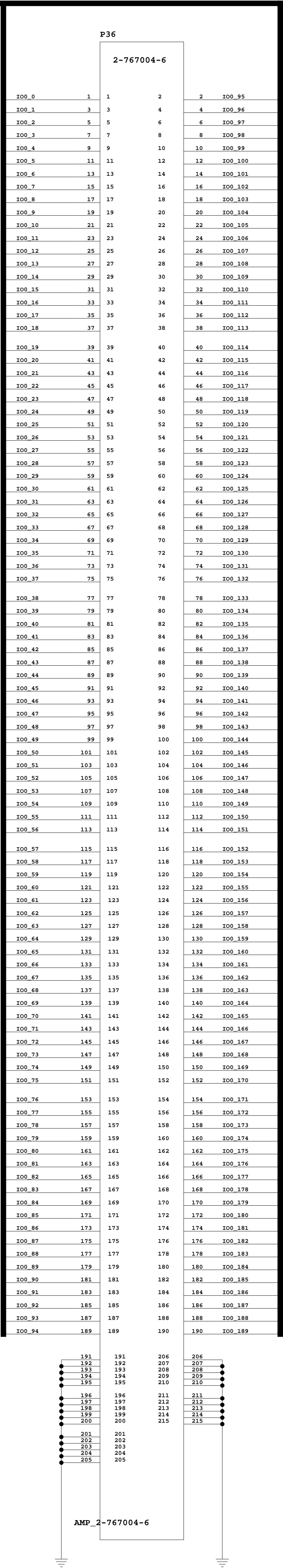
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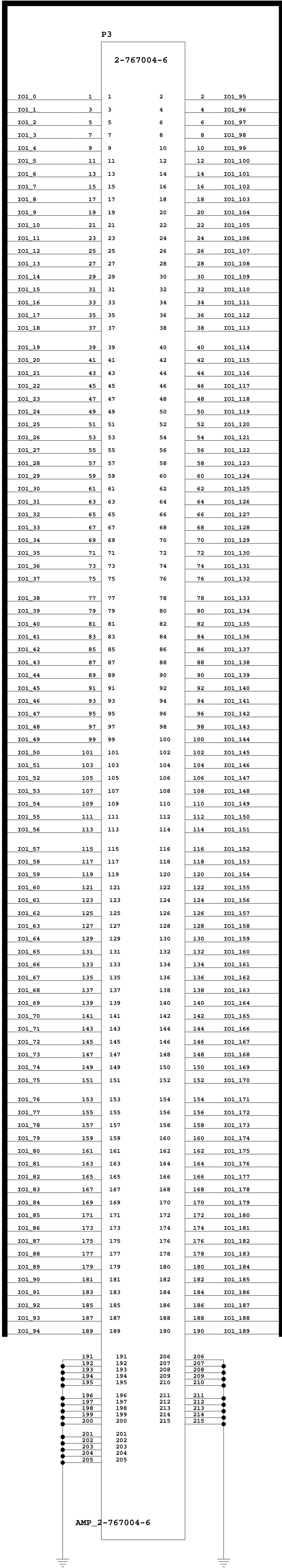


EXPANSION CONNECTORS

100\_1189-01



100\_1189-01



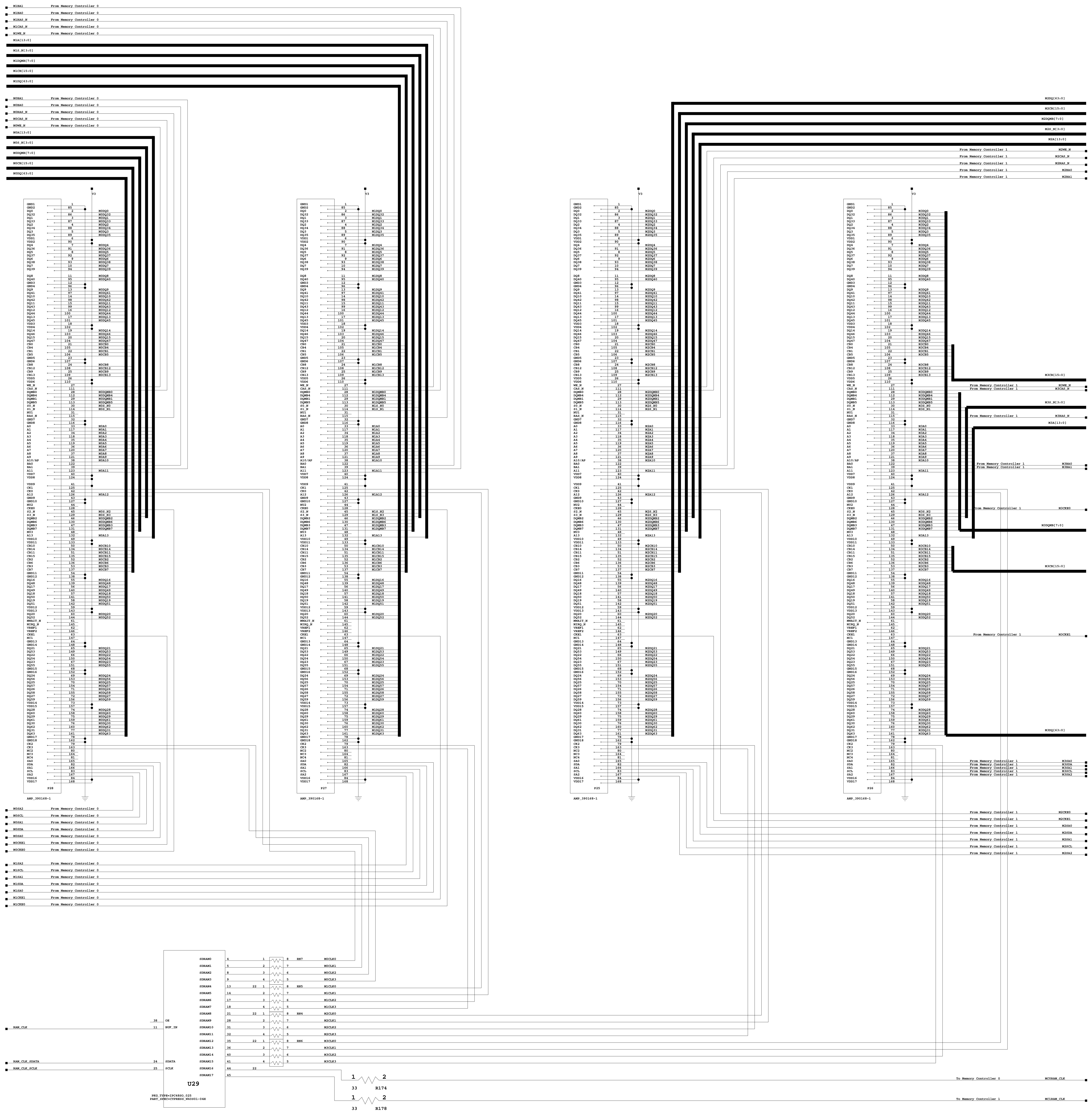
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PROJECT NAME: AMP

SCHEMATIC NAME:  
EXP\_CONN



## SDRAM 's

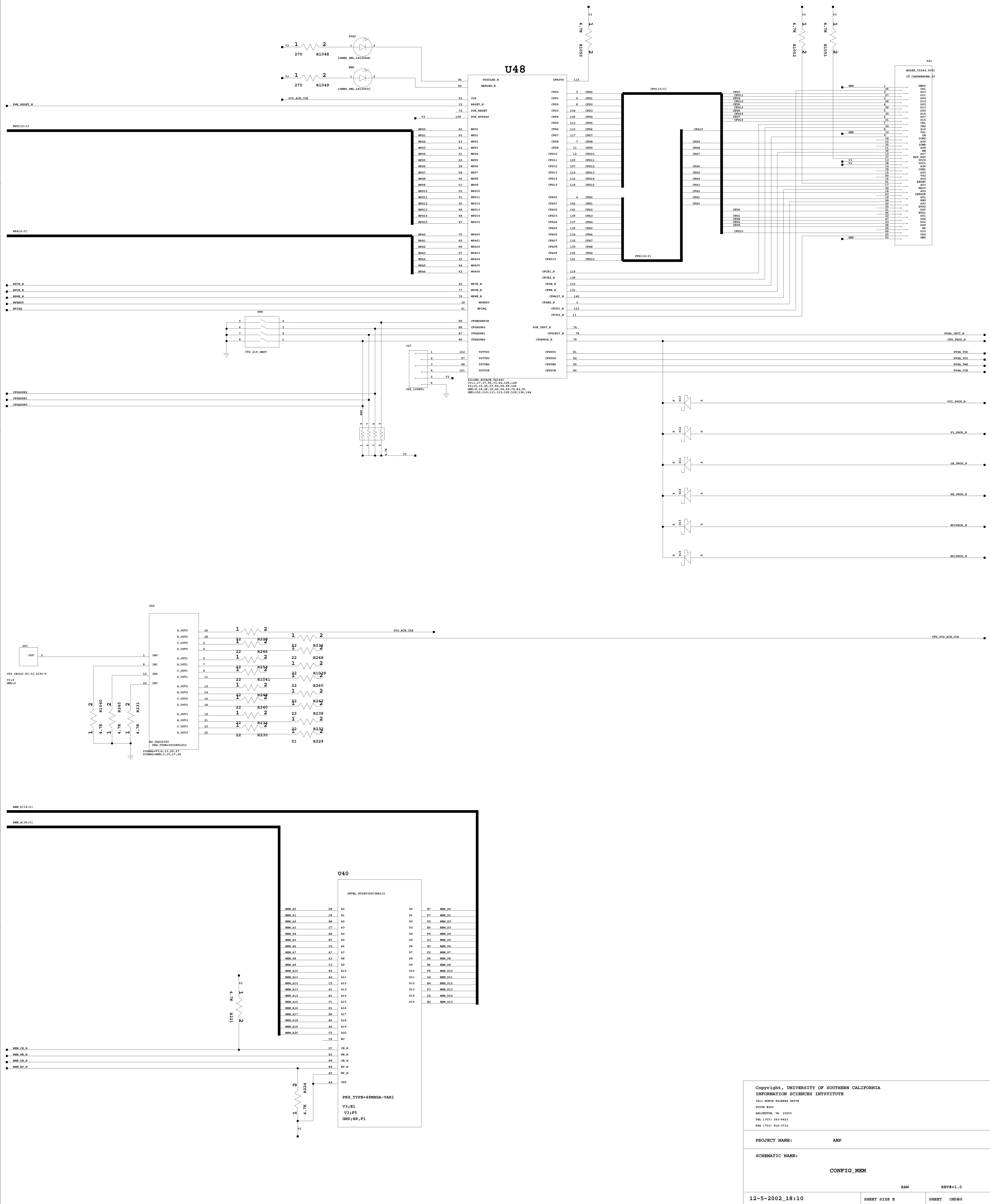






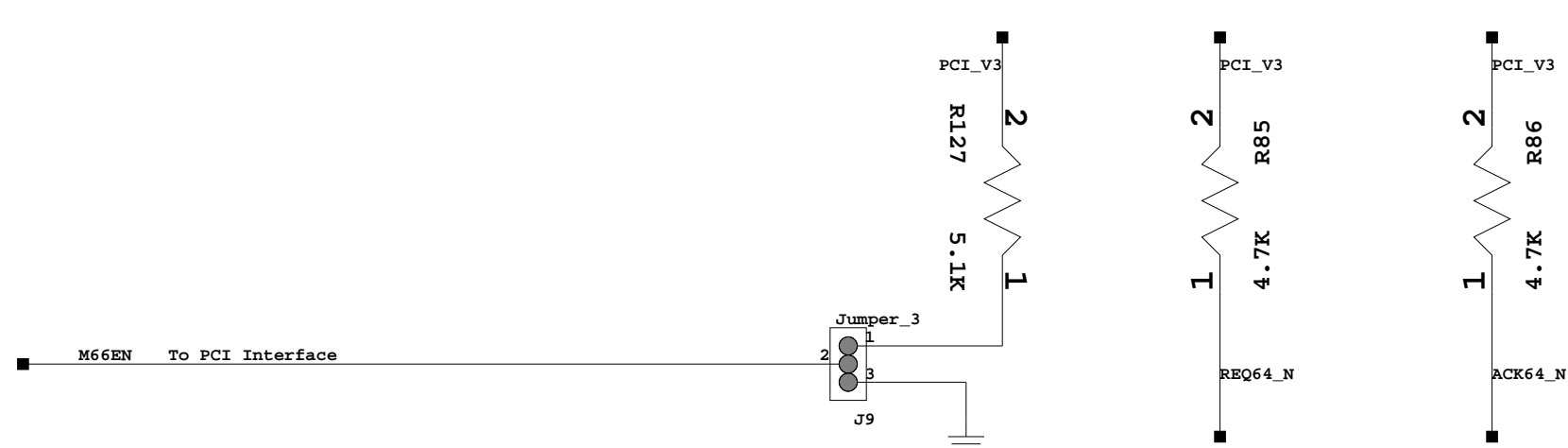
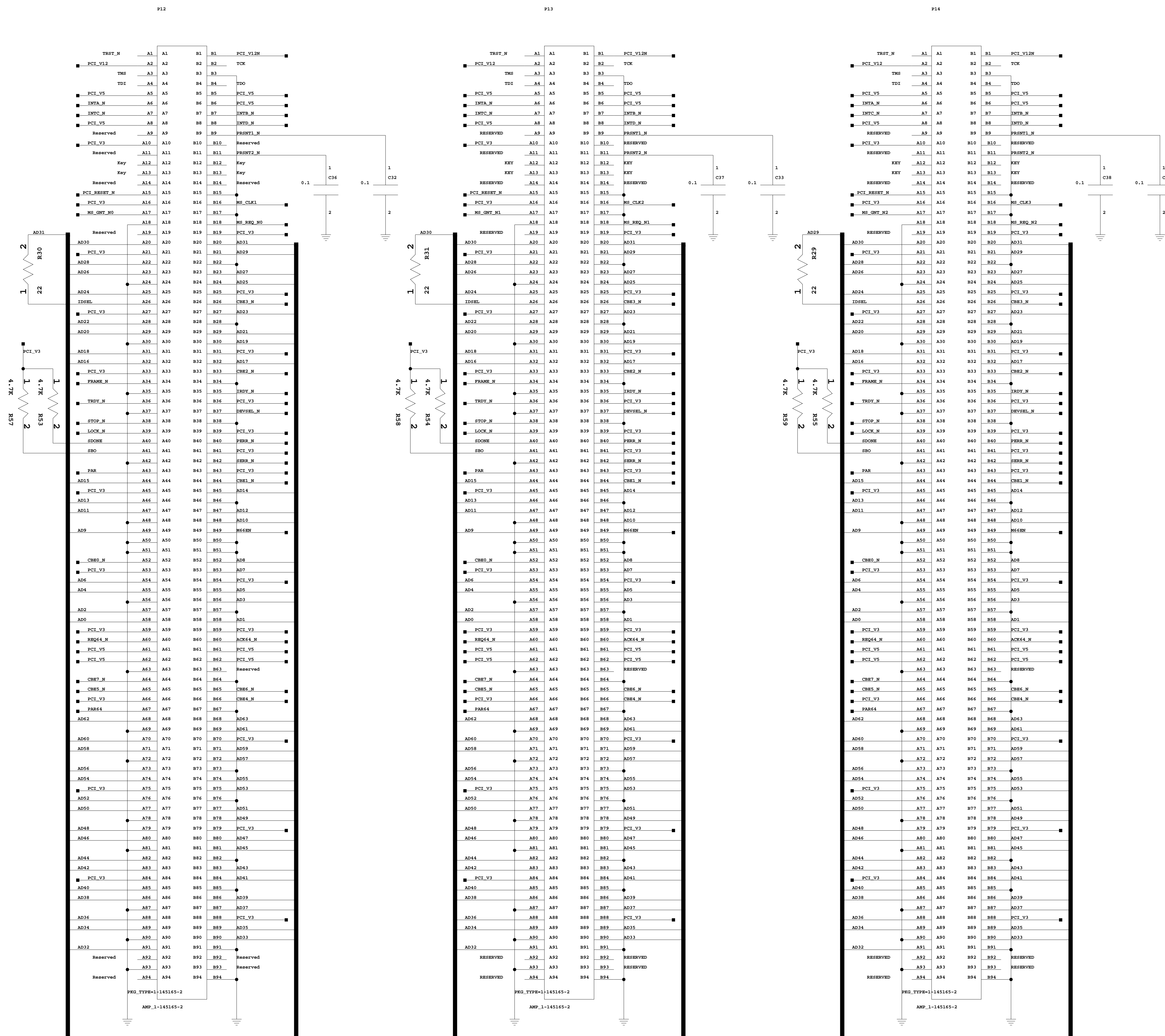


## CONFIGURATION MEMORY





## PCI CONNECTORS



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PROJECT NAME:	AMP
<hr/>	
SCHEMATIC NAME:	PCI_CONN

RAW REV#=1.0

12-5-2002\_18:10

SHEET SIZE E	SHEET OF230
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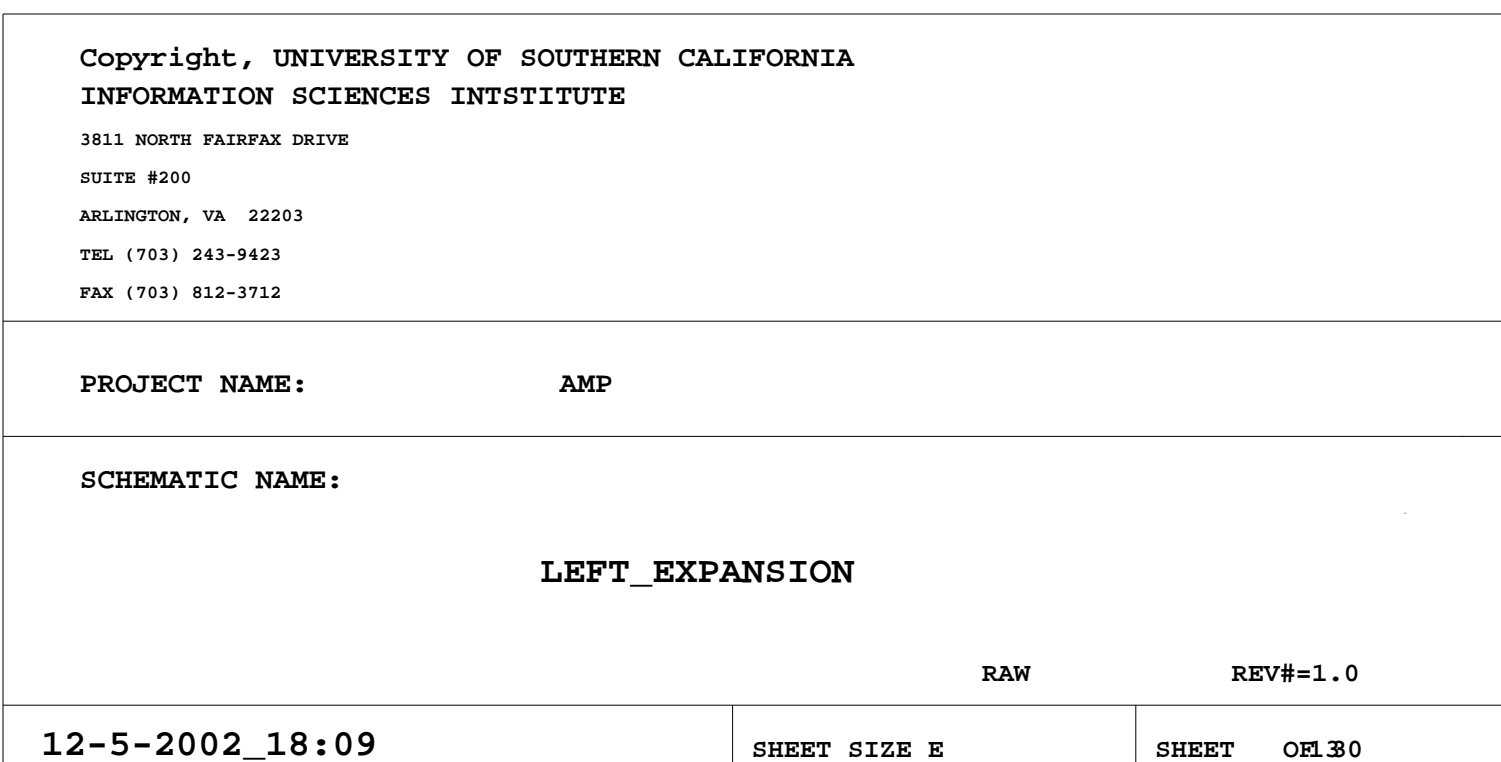
The schematic diagram illustrates a complex electronic circuit, likely a power supply or signal processing unit. The central component is a large integrated circuit (IC) labeled U5, which is connected to various other components. The circuit includes a power input section with a transformer (T1) and a rectifier (D1). The control section includes a microcontroller (U3) and several other ICs (U1, U2, U4, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25, U26, U27, U28, U29, U30, U31, U32, U33, U34, U35, U36, U37, U38, U39, U40, U41, U42, U43, U44, U45, U46, U47, U48, U49, U50, U51, U52, U53, U54, U55, U56, U57, U58, U59, U60, U61, U62, U63, U64, U65, U66, U67, U68, U69, U70, U71, U72, U73, U74, U75, U76, U77, U78, U79, U80, U81, U82, U83, U84, U85, U86, U87, U88, U89, U90, U91, U92, U93, U94, U95, U96, U97, U98, U99, U100). The signal processing section includes a series of comparators (U1, U2, U3, U4, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25, U26, U27, U28, U29, U30, U31, U32, U33, U34, U35, U36, U37, U38, U39, U40, U41, U42, U43, U44, U45, U46, U47, U48, U49, U50, U51, U52, U53, U54, U55, U56, U57, U58, U59, U60, U61, U62, U63, U64, U65, U66, U67, U68, U69, U70, U71, U72, U73, U74, U75, U76, U77, U78, U79, U80, U81, U82, U83, U84, U85, U86, U87, U88, U89, U90, U91, U92, U93, U94, U95, U96, U97, U98, U99, U100) and a series of operational amplifiers (U1, U2, U3, U4, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25, U26, U27, U28, U29, U30, U31, U32, U33, U34, U35, U36, U37, U38, U39, U40, U41, U42, U43, U44, U45, U46, U47, U48, U49, U50, U51, U52, U53, U54, U55, U56, U57, U58, U59, U60, U61, U62, U63, U64, U65, U66, U67, U68, U69, U70, U71, U72, U73, U74, U75, U76, U77, U78, U79, U80, U81, U82, U83, U84, U85, U86, U87, U88, U89, U90, U91, U92, U93, U94, U95, U96, U97, U98, U99, U100). The circuit is organized into several functional blocks, including a power input section, a control section, and a signal processing section. The schematic includes numerous labels for components and their connections, as well as a detailed list of components at the bottom.

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RAW REV#=1.0

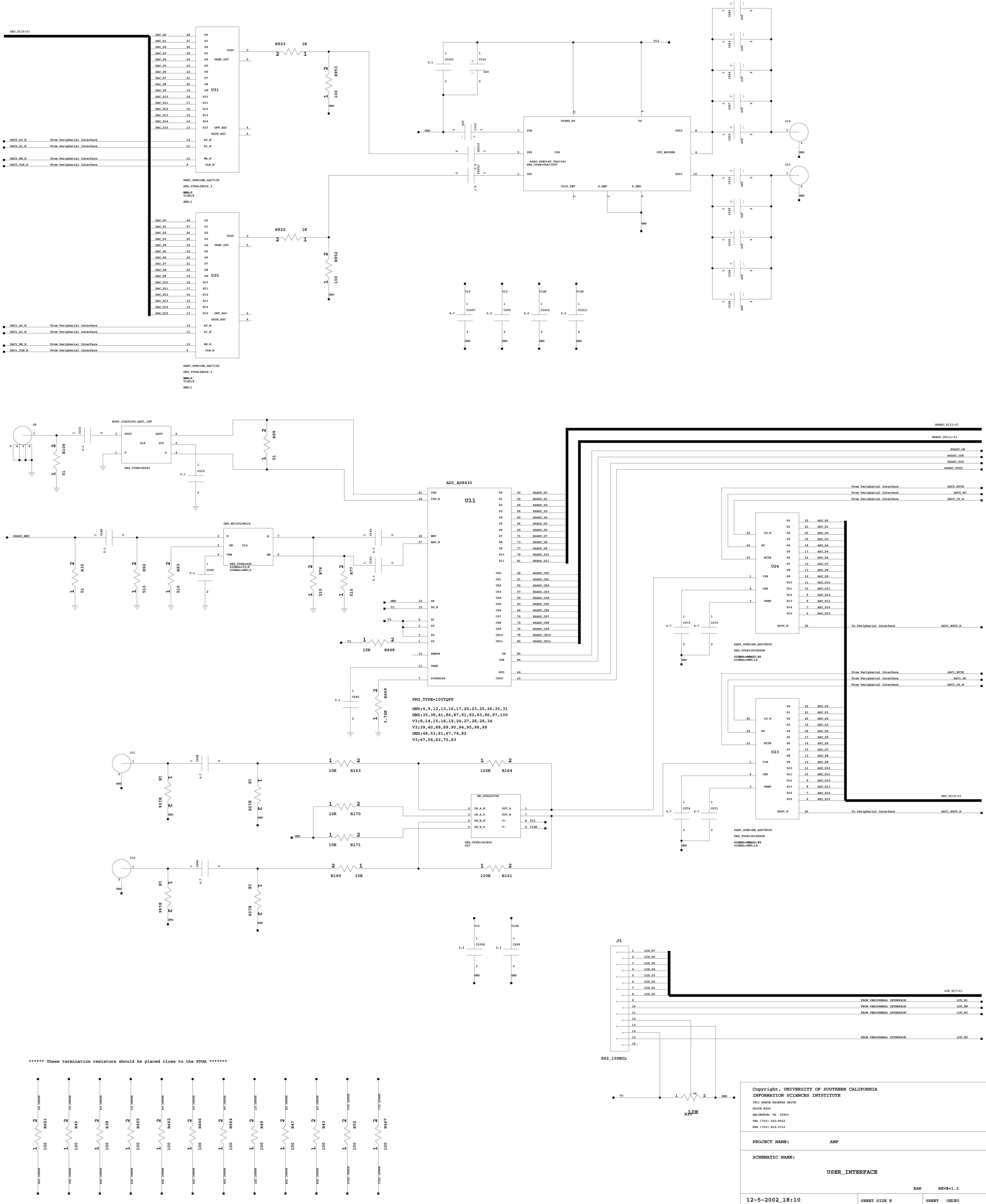
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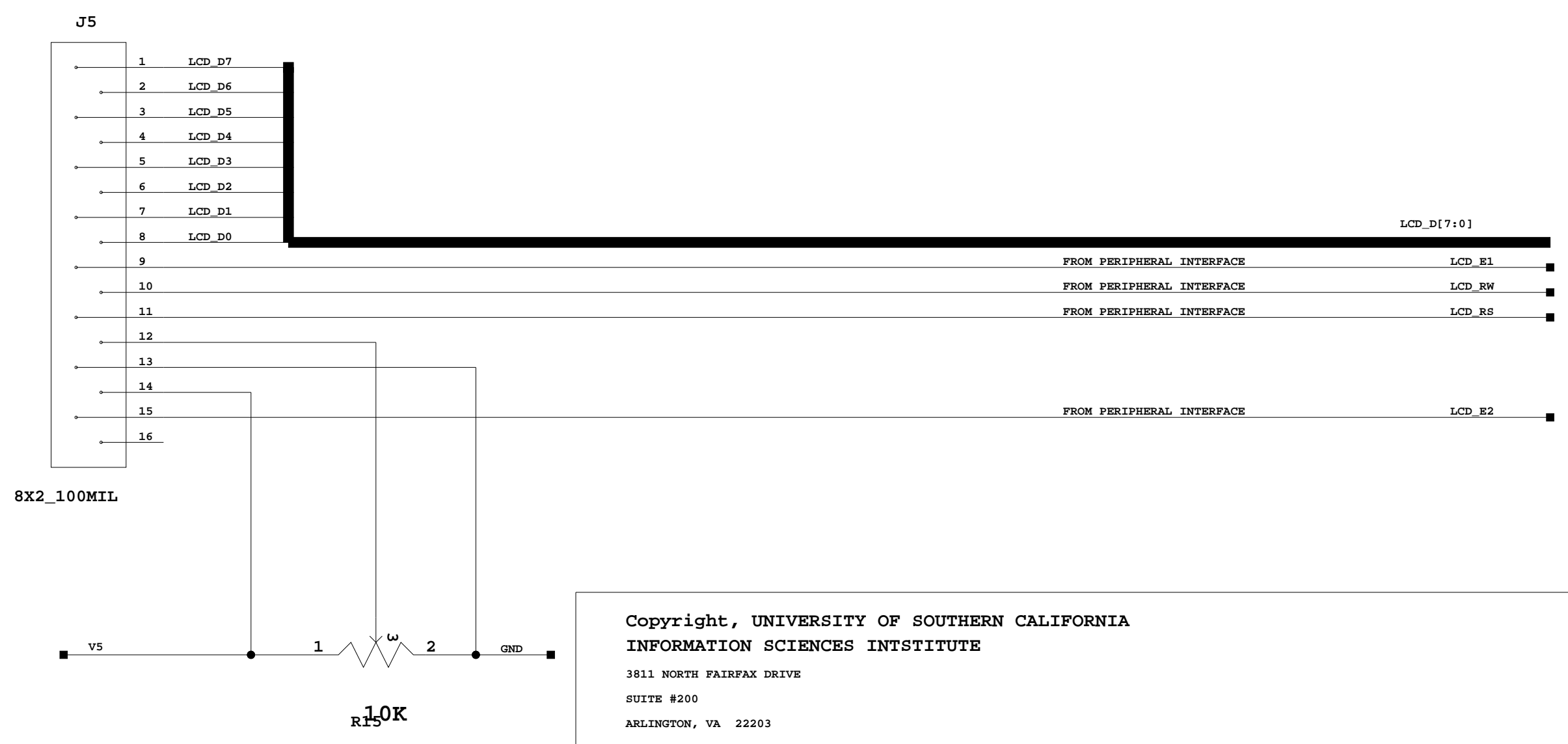
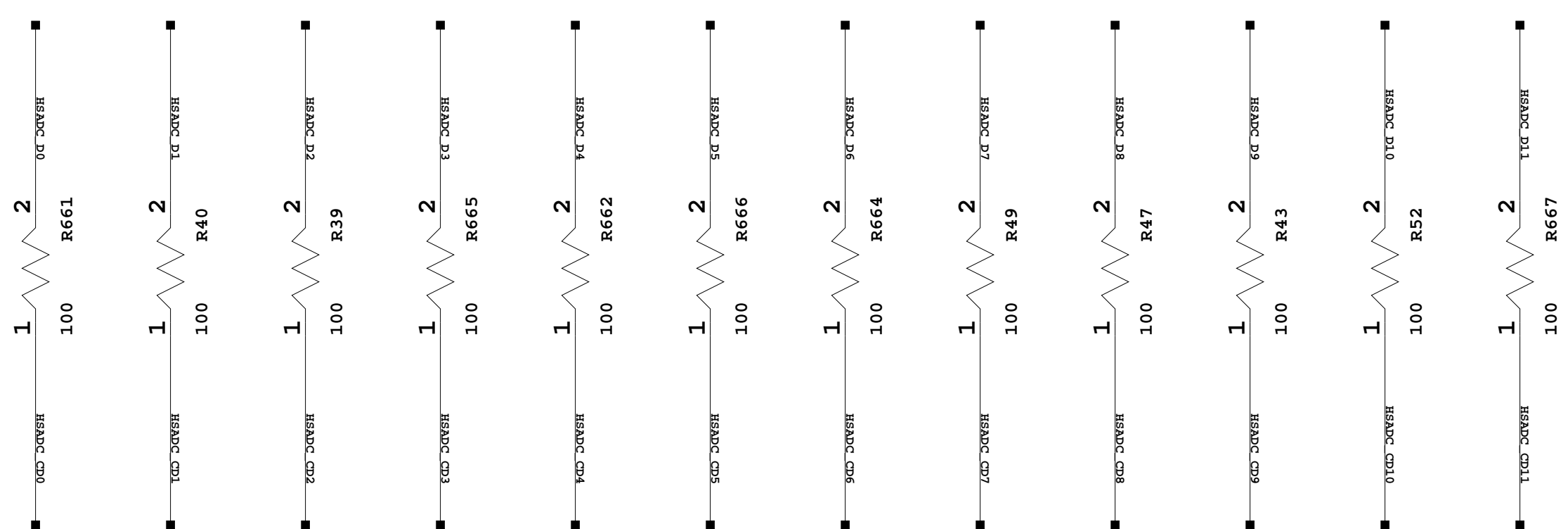




## USER INTERFACES



\*\*\*\*\* These termination resistors should be placed close to the FPGA \*\*\*\*\*



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PROJECT NAME: AMP

---

SCHEMATIC NAME:

USER INTERFACE

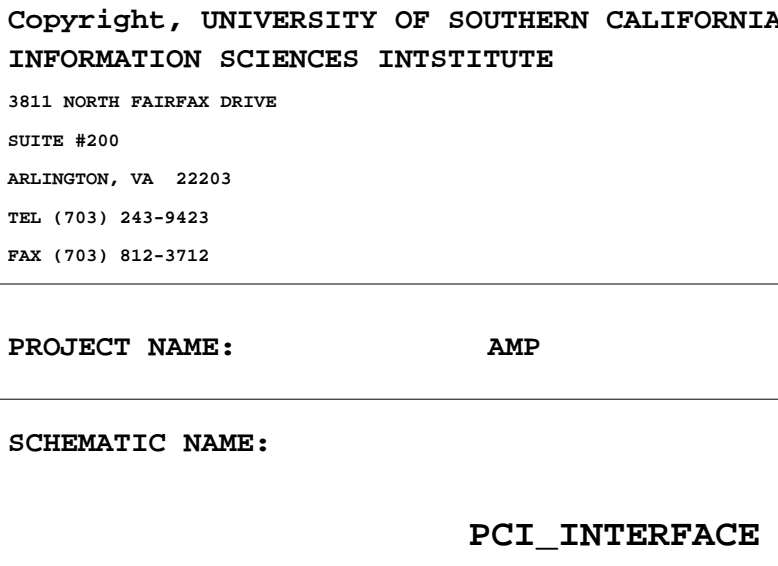
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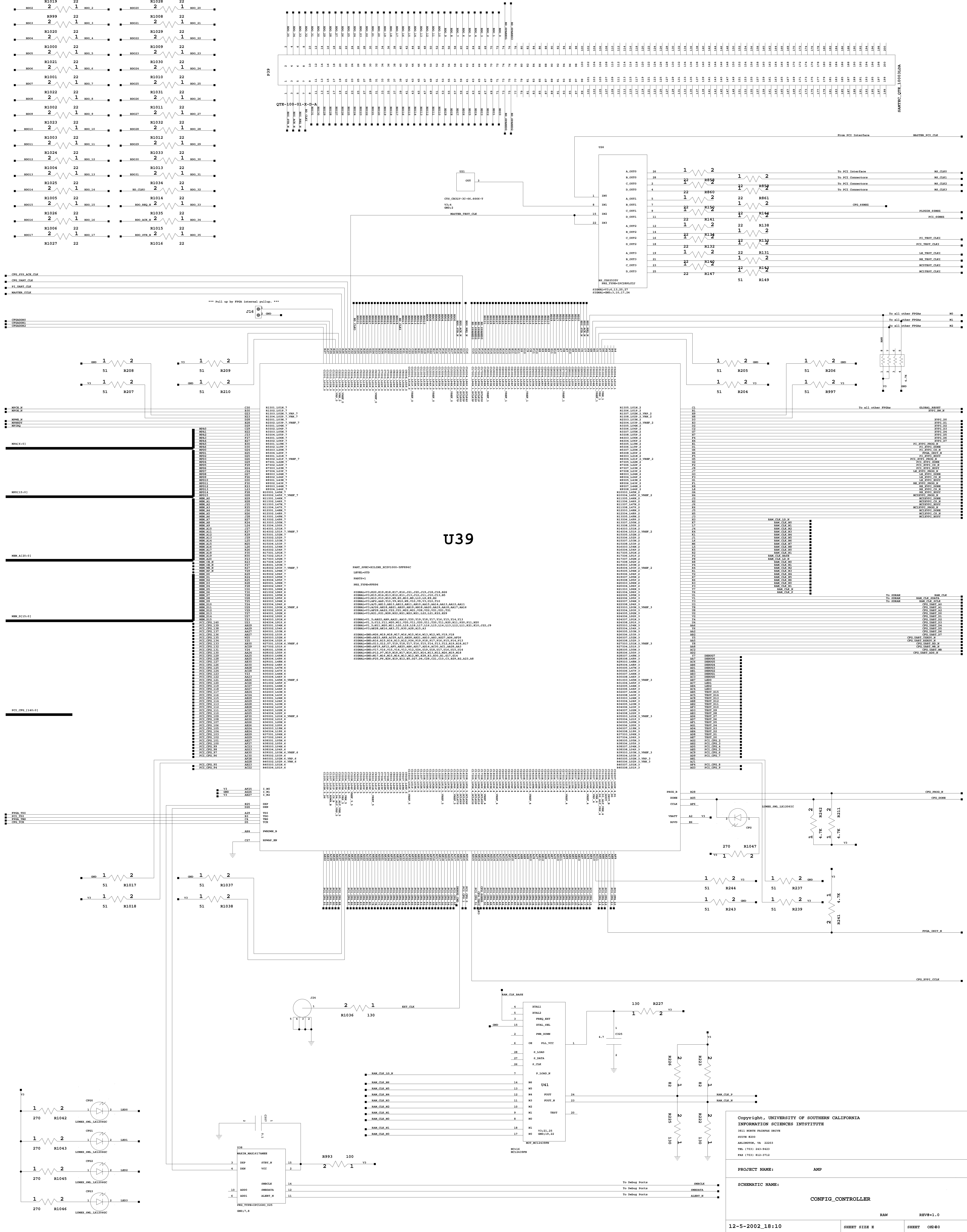


# U15



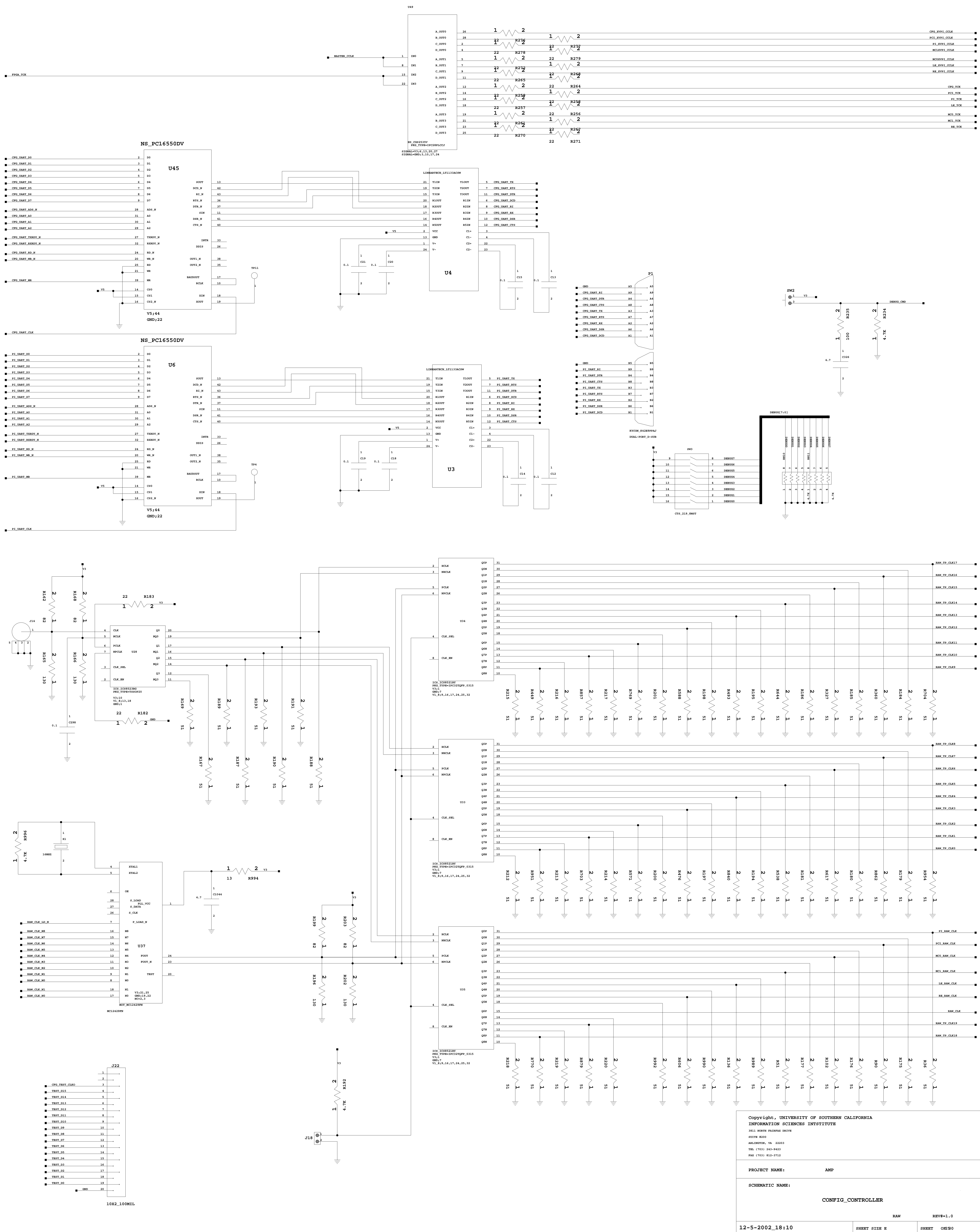


## CONFIGURATION CONTROLLER



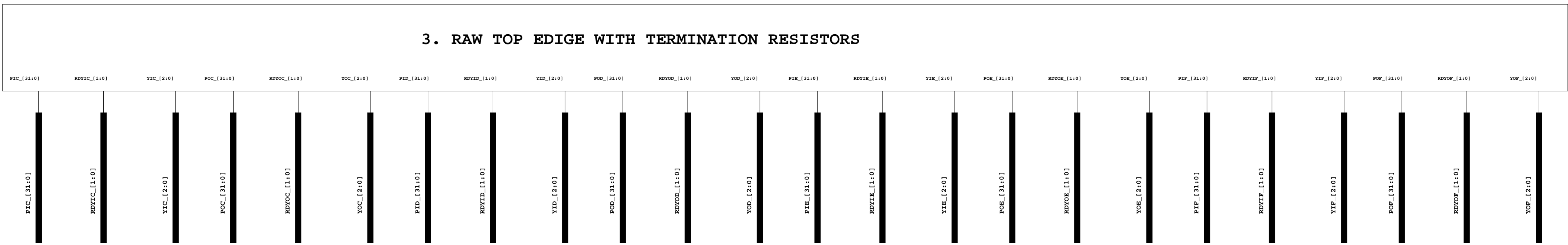
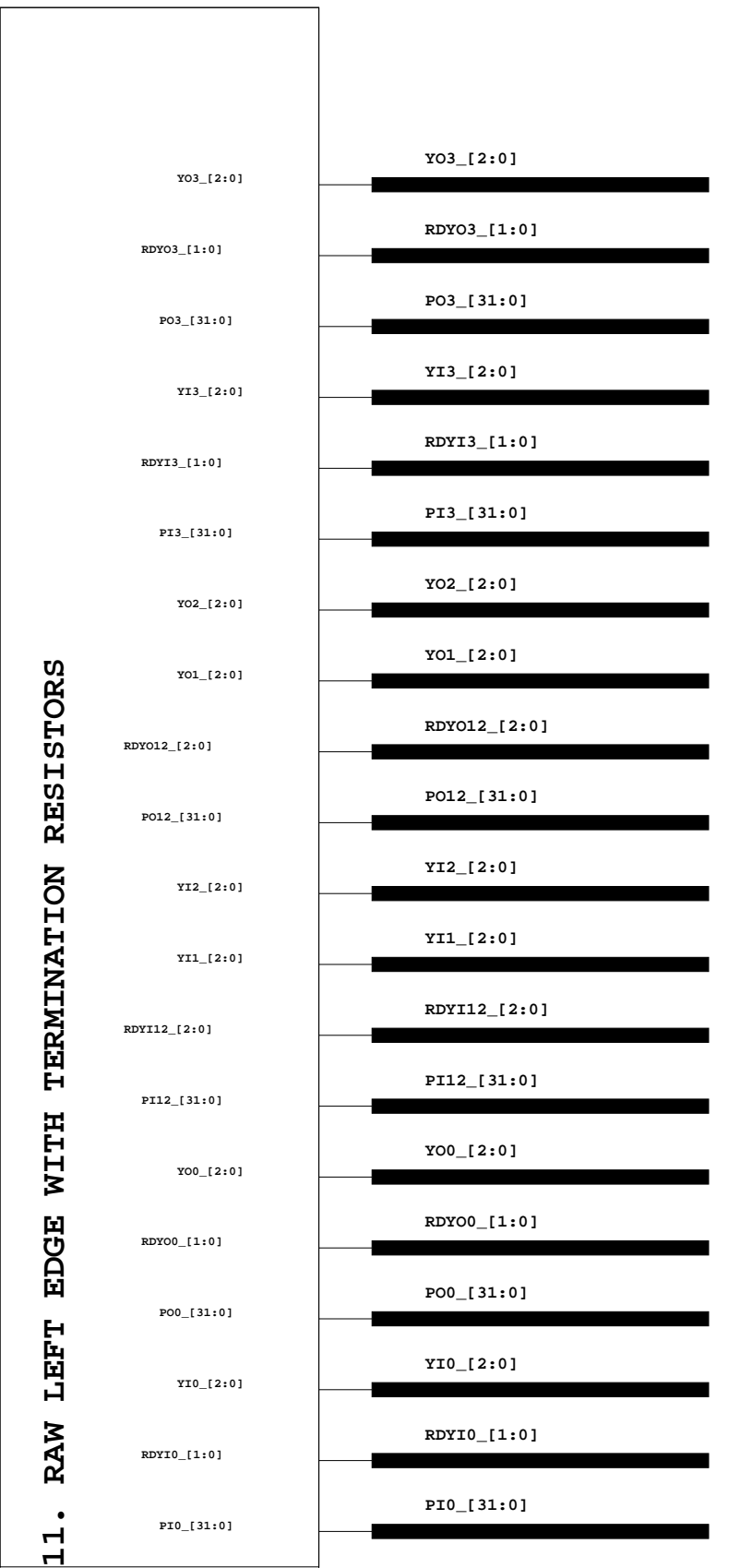
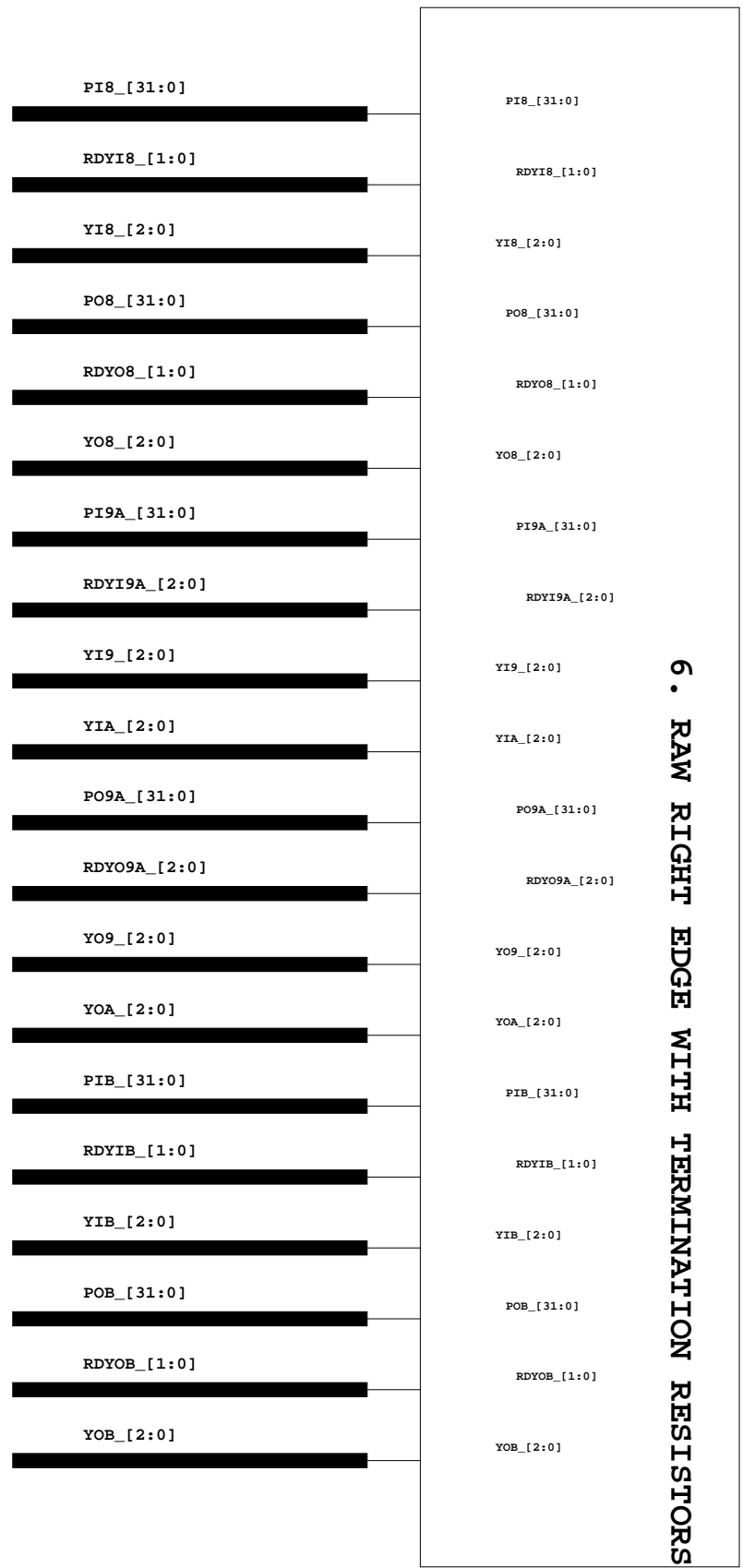
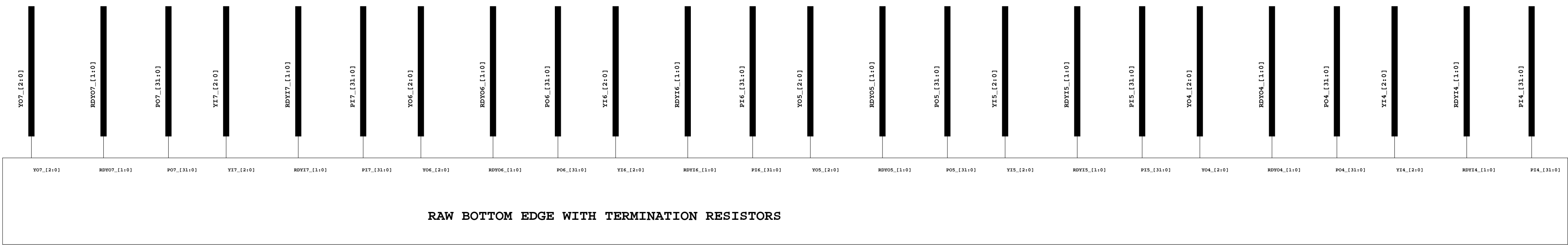


## CONFIGURATION CONTROLLER

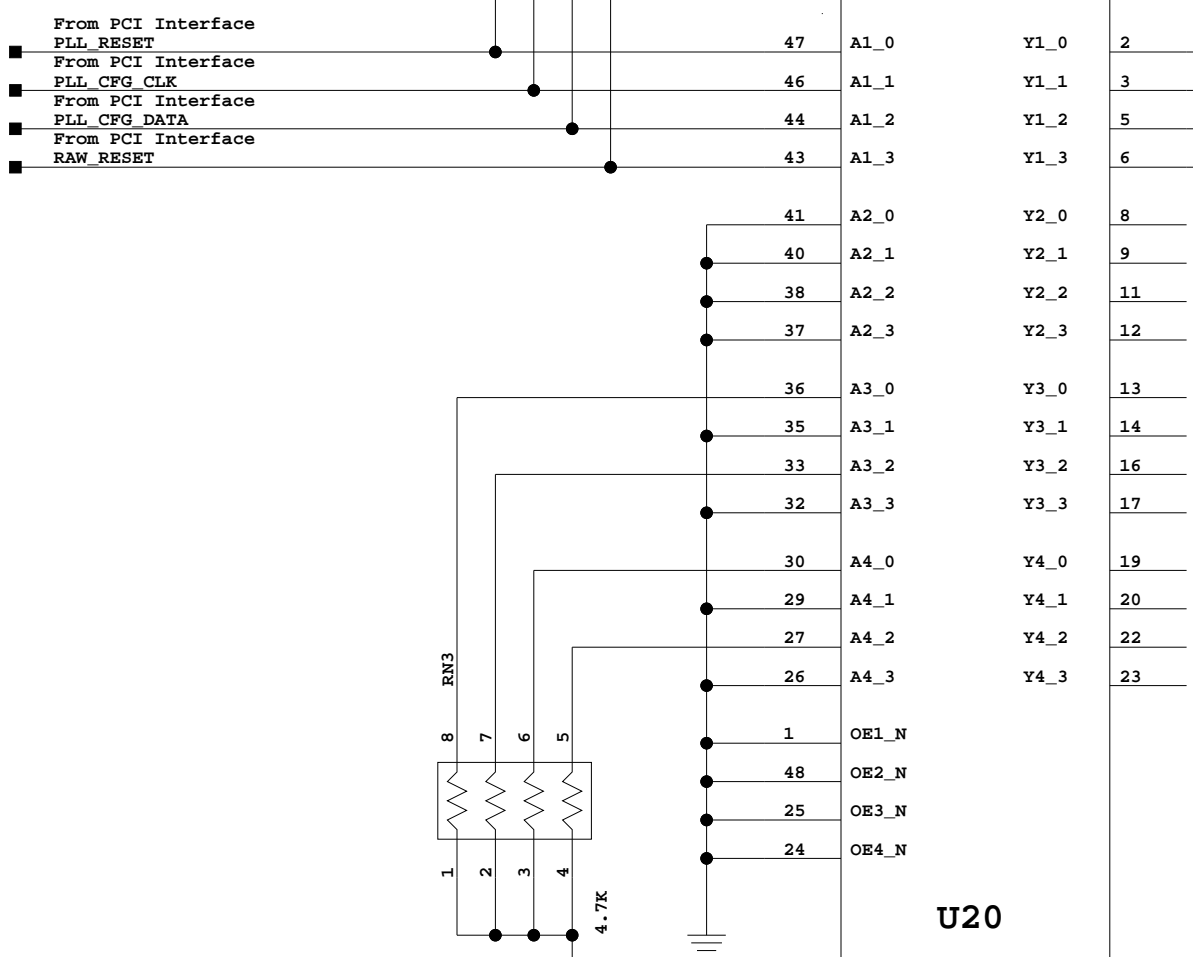




RAW CPU

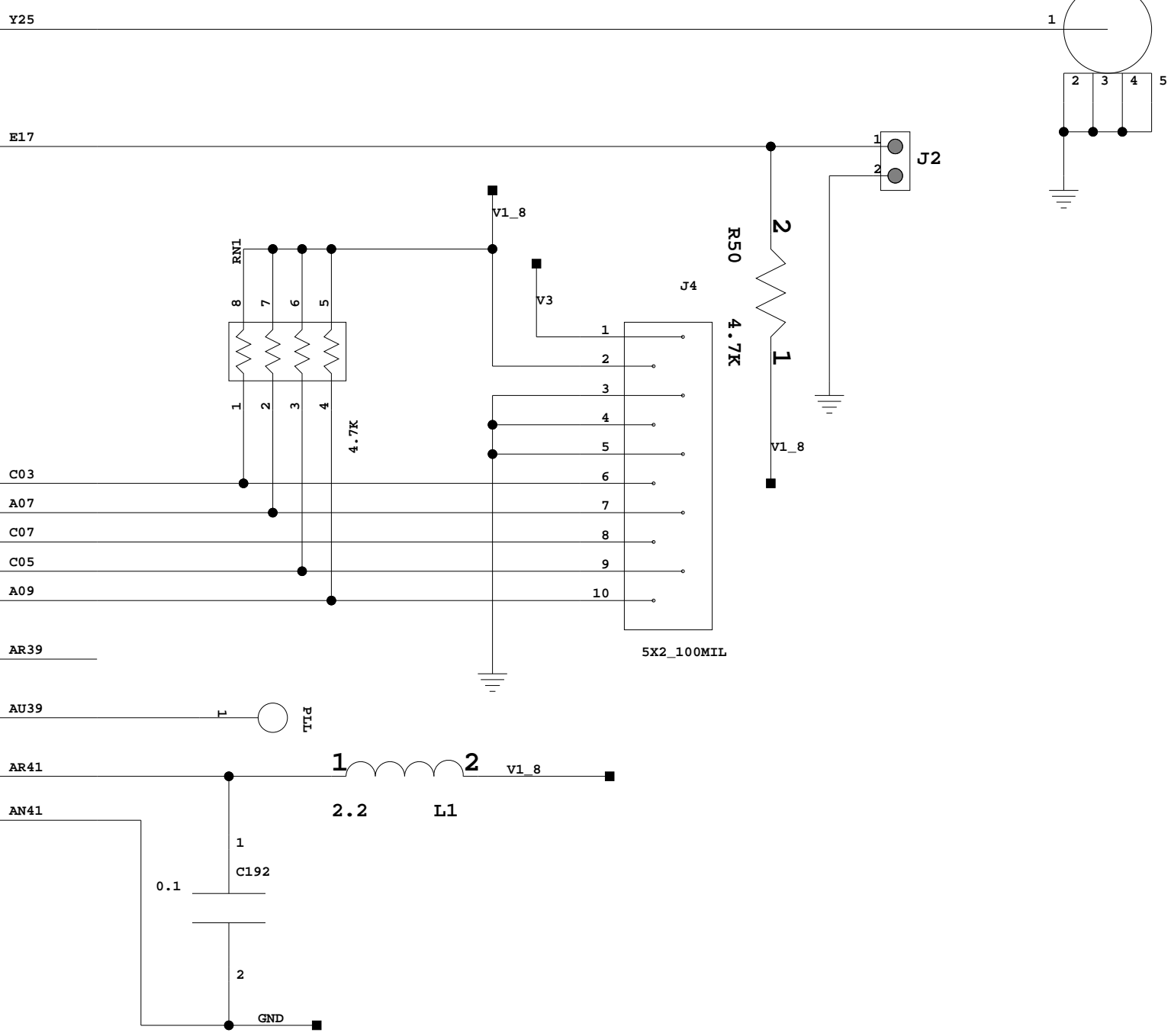
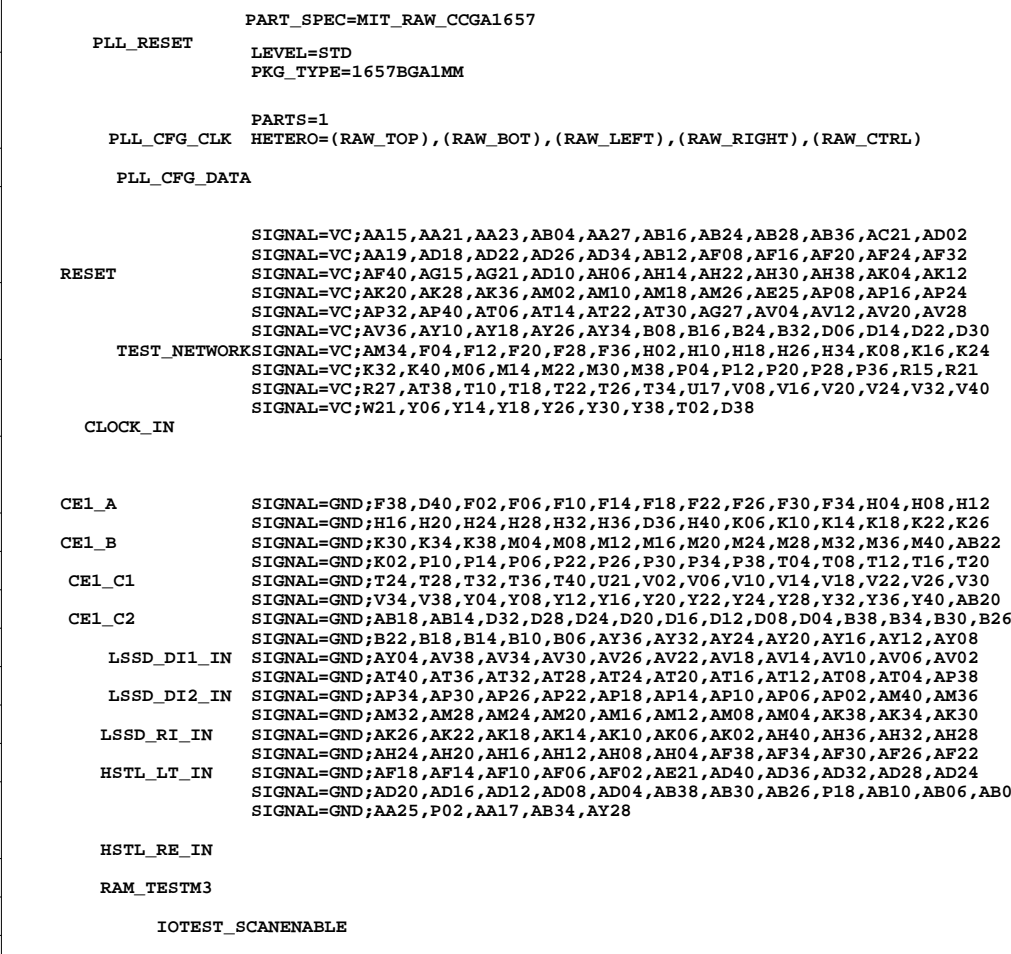


To PCI Interface  
TEST NETWORK  
From Configuration Controller, MTD logic level  
RAW\_C0



PAIDFIELD 74VCL6344  
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P11\_1(1:0) P12\_1(1:0) P13\_1(1:0)  
P14\_1(1:0) P15\_1(1:0) P16\_1(1:0)

U13



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PROJECT NAME: AMP  
SCHEMATIC NAME:

RAW\_CPU

RAW REV#1.0

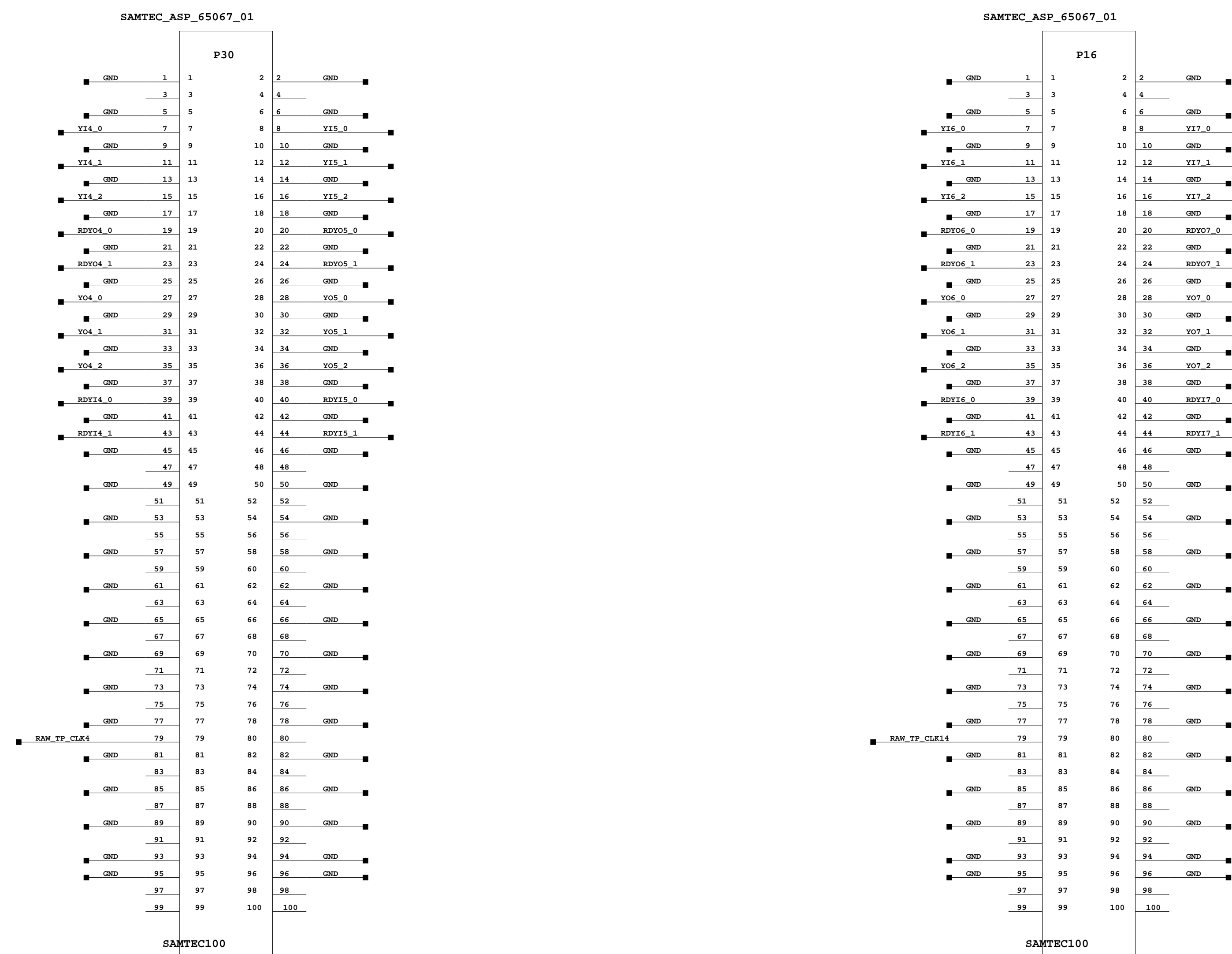
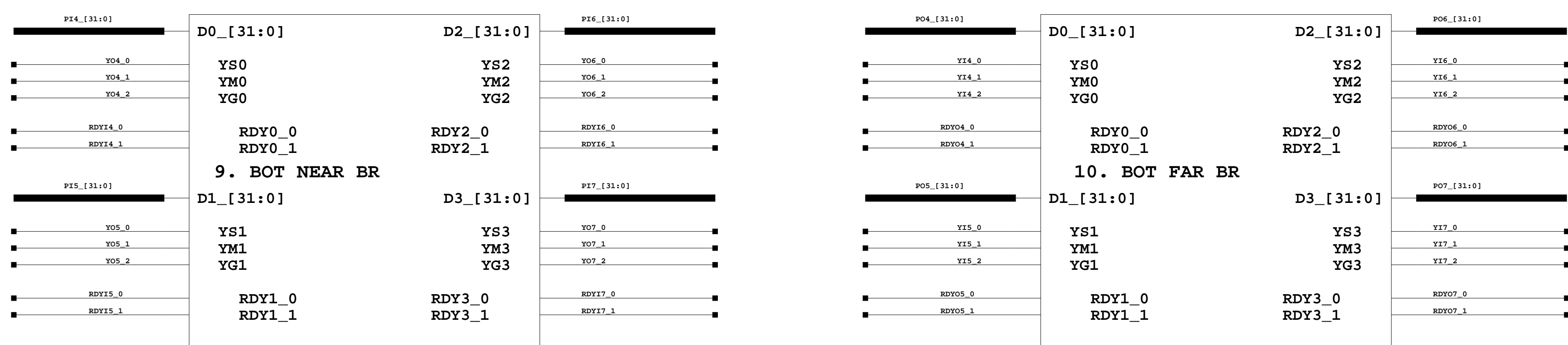
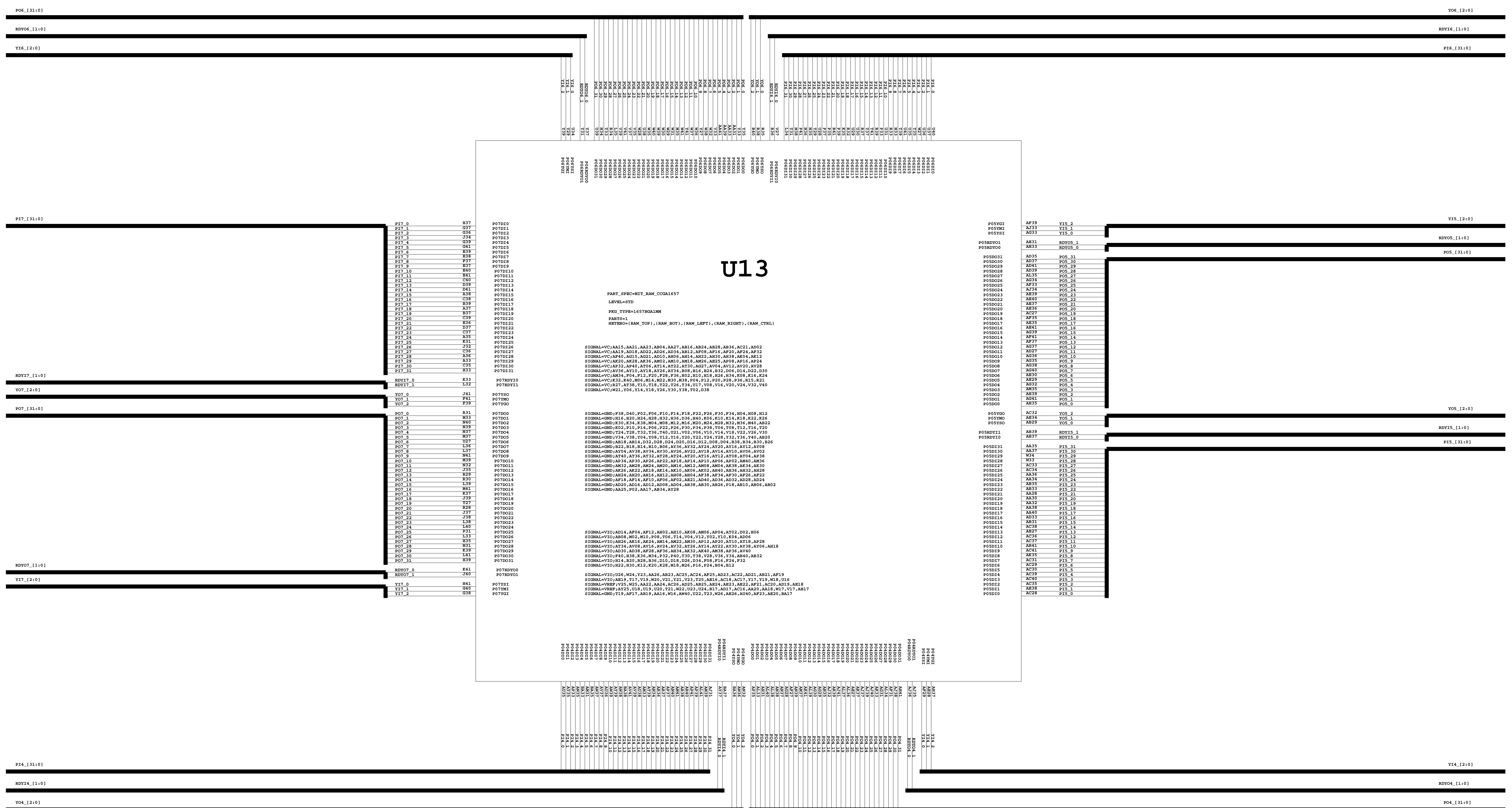
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SHEET SIZE E

SHEET 002 30

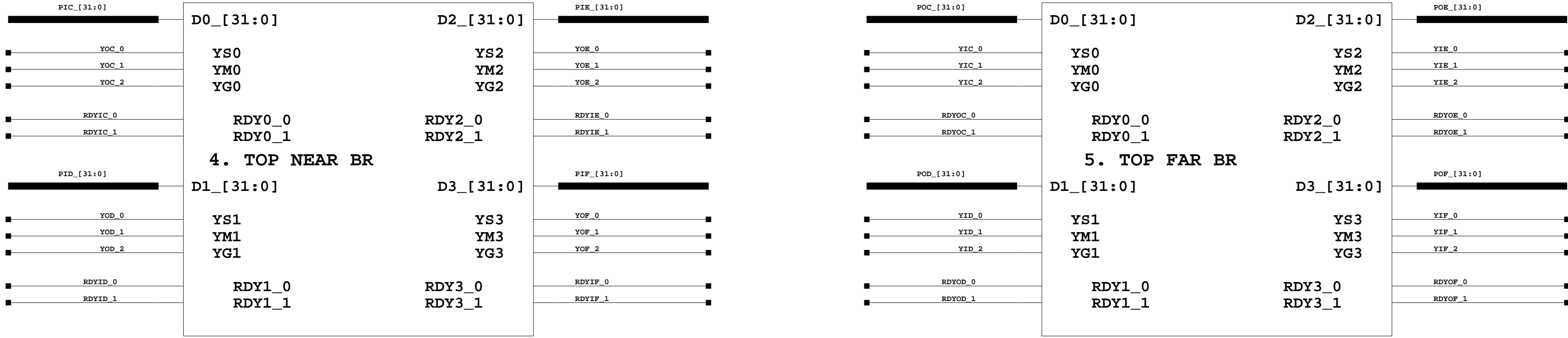
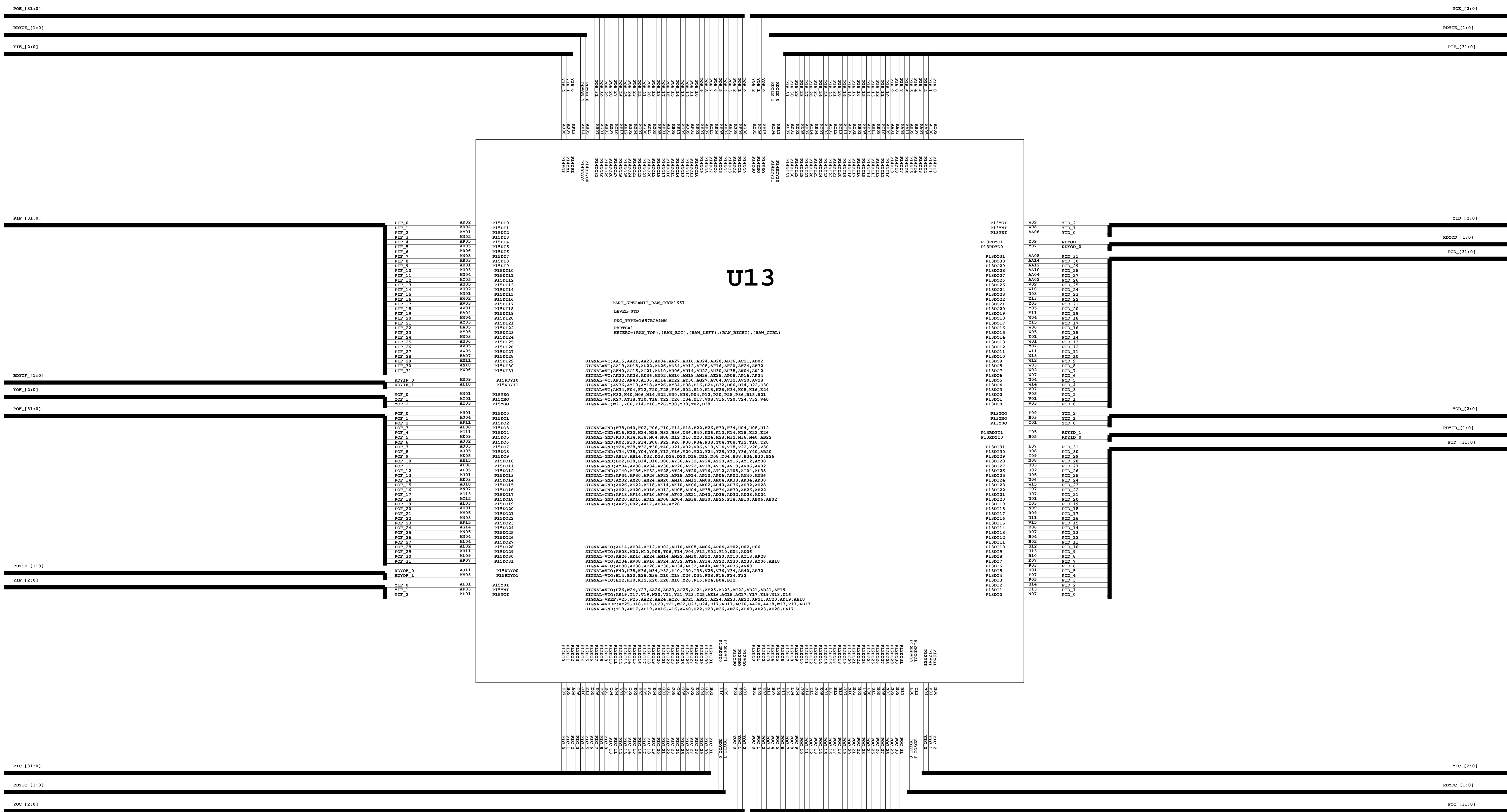


## RAW Bottom Edge With Resistors





RAW Top Edge With Resistors



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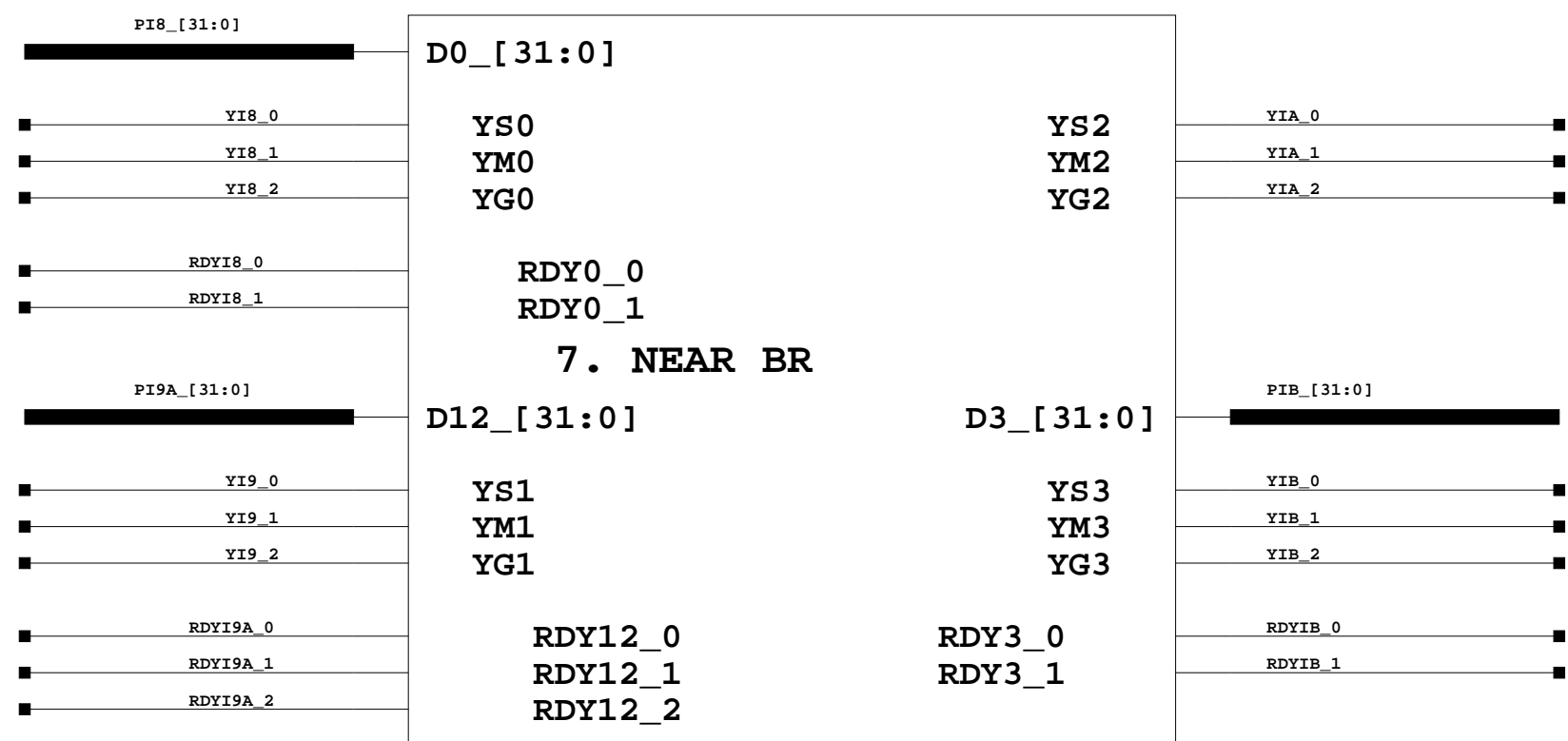
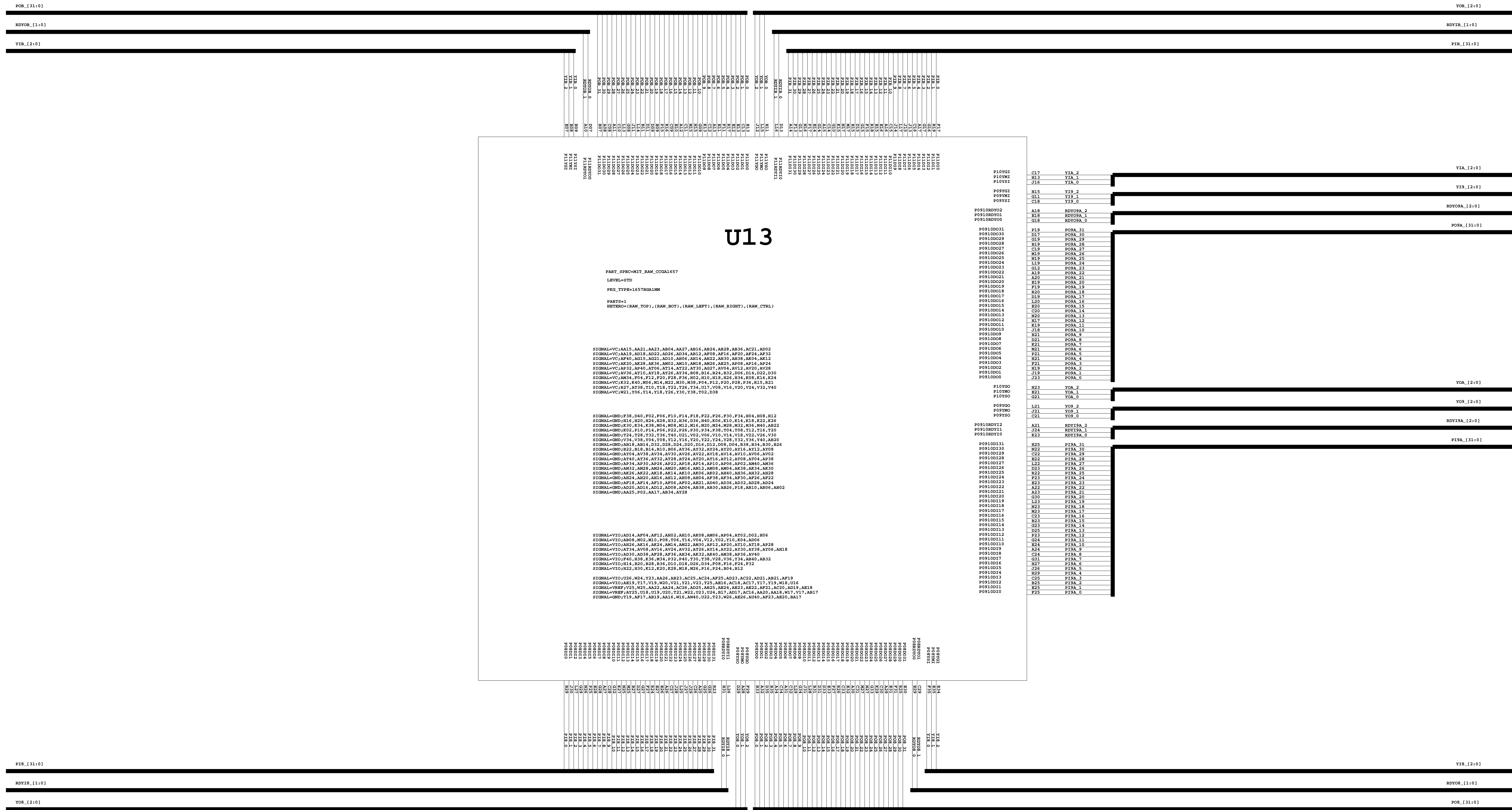
PROJECT NAME: AMP

SCHEMATIC NAME:

RAW\_BR\_TOP

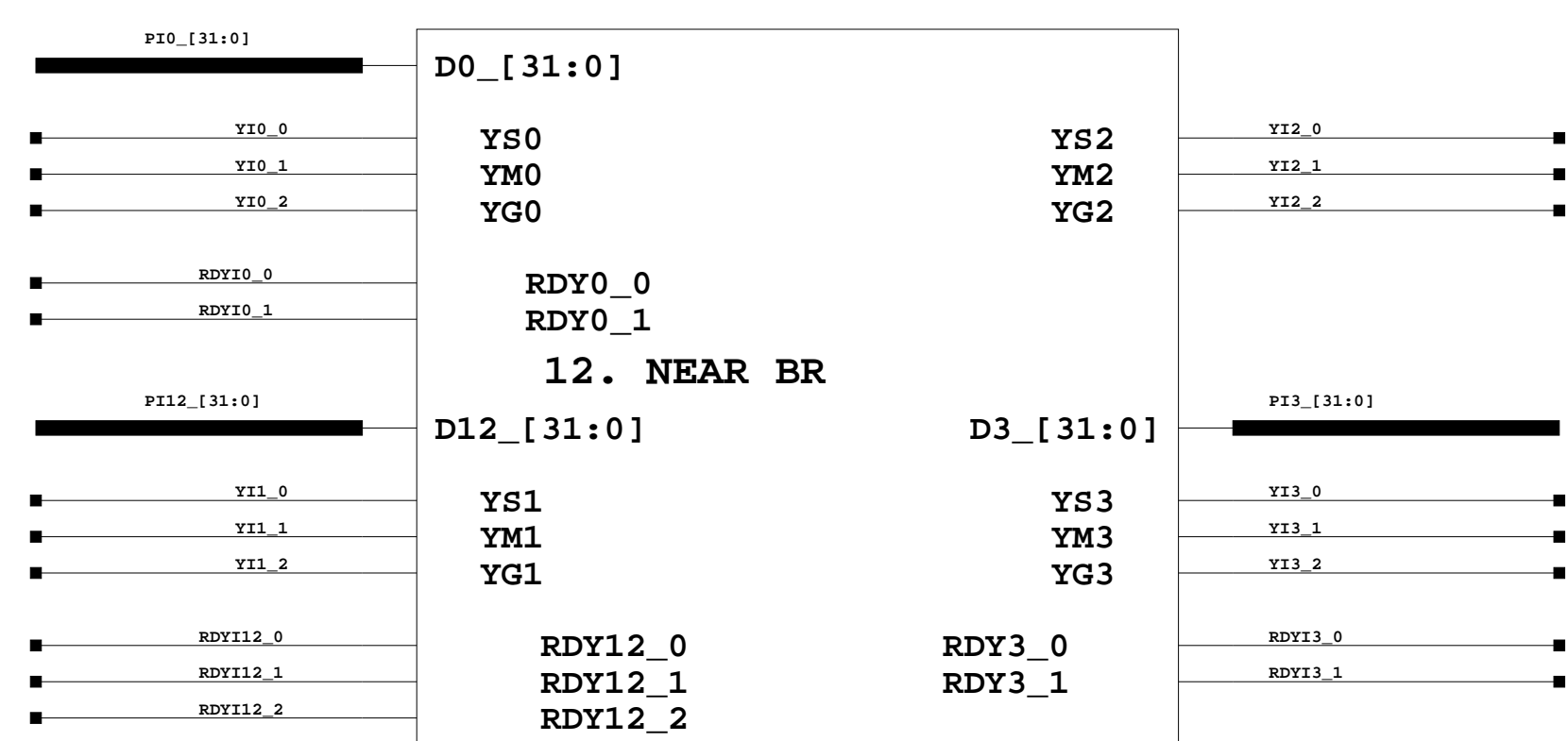
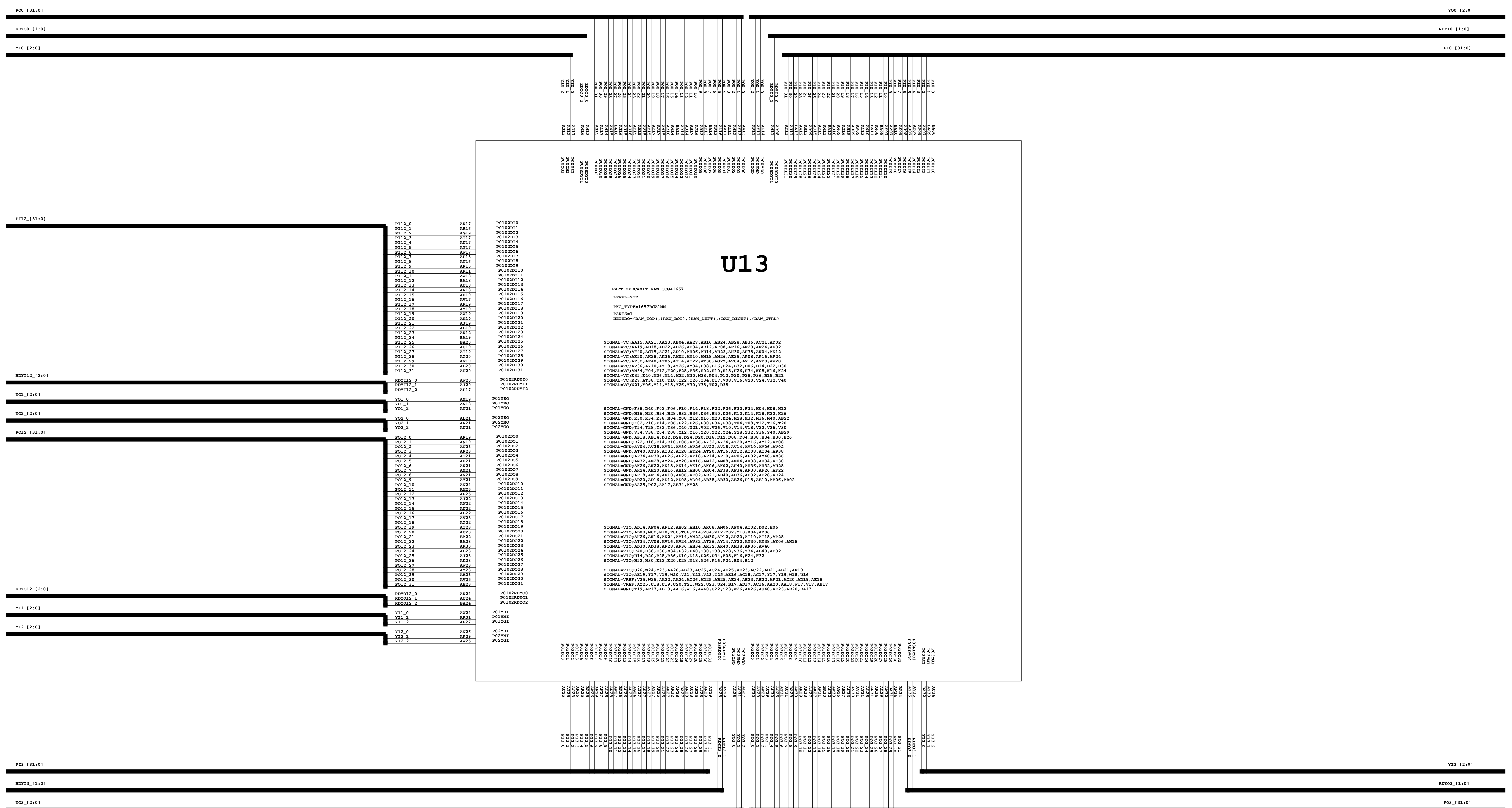


RAW Right Edge With Resistors



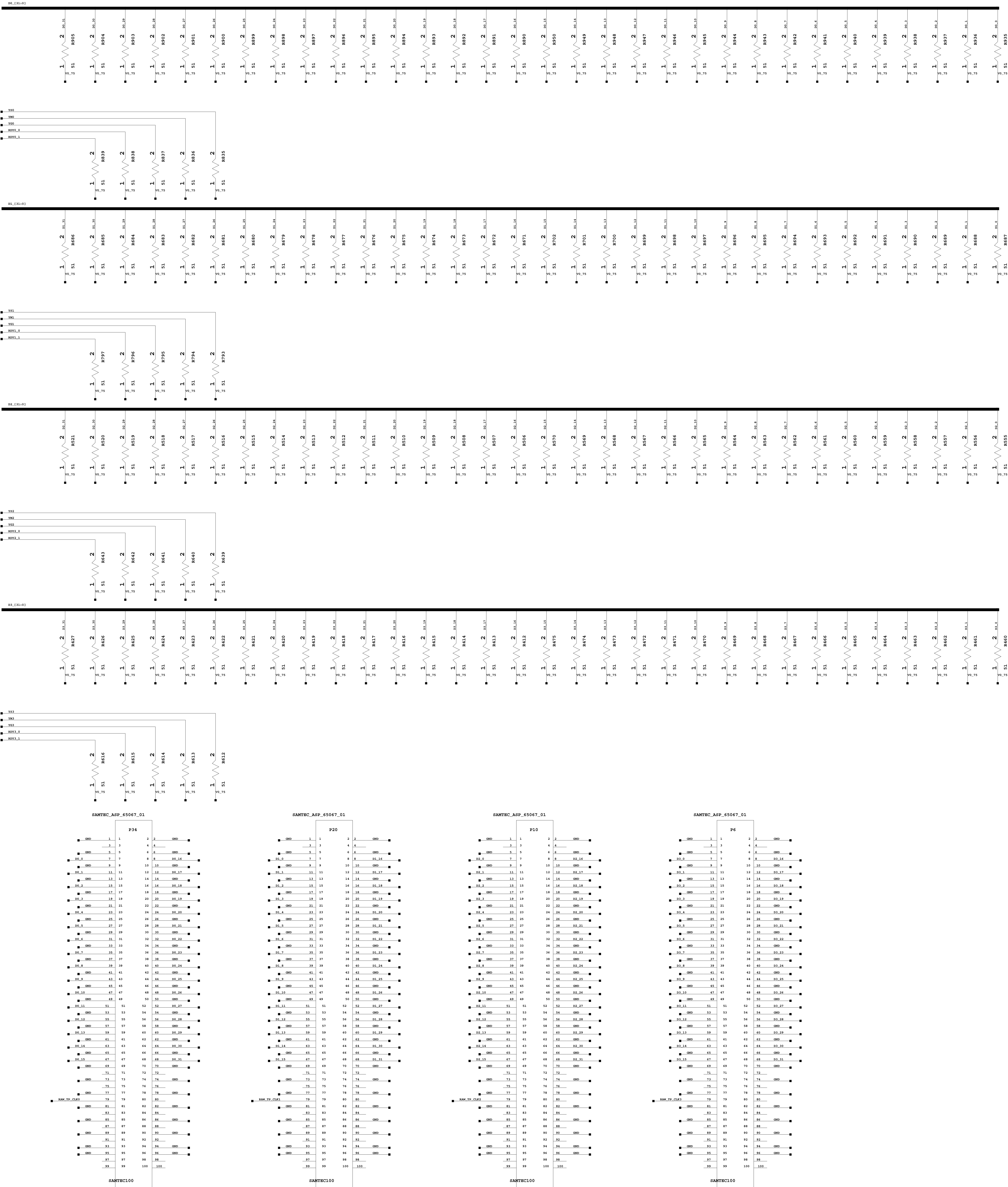


## RAW Left Edge With Resistors





RAW Bottom Edge Near Termination Resistors



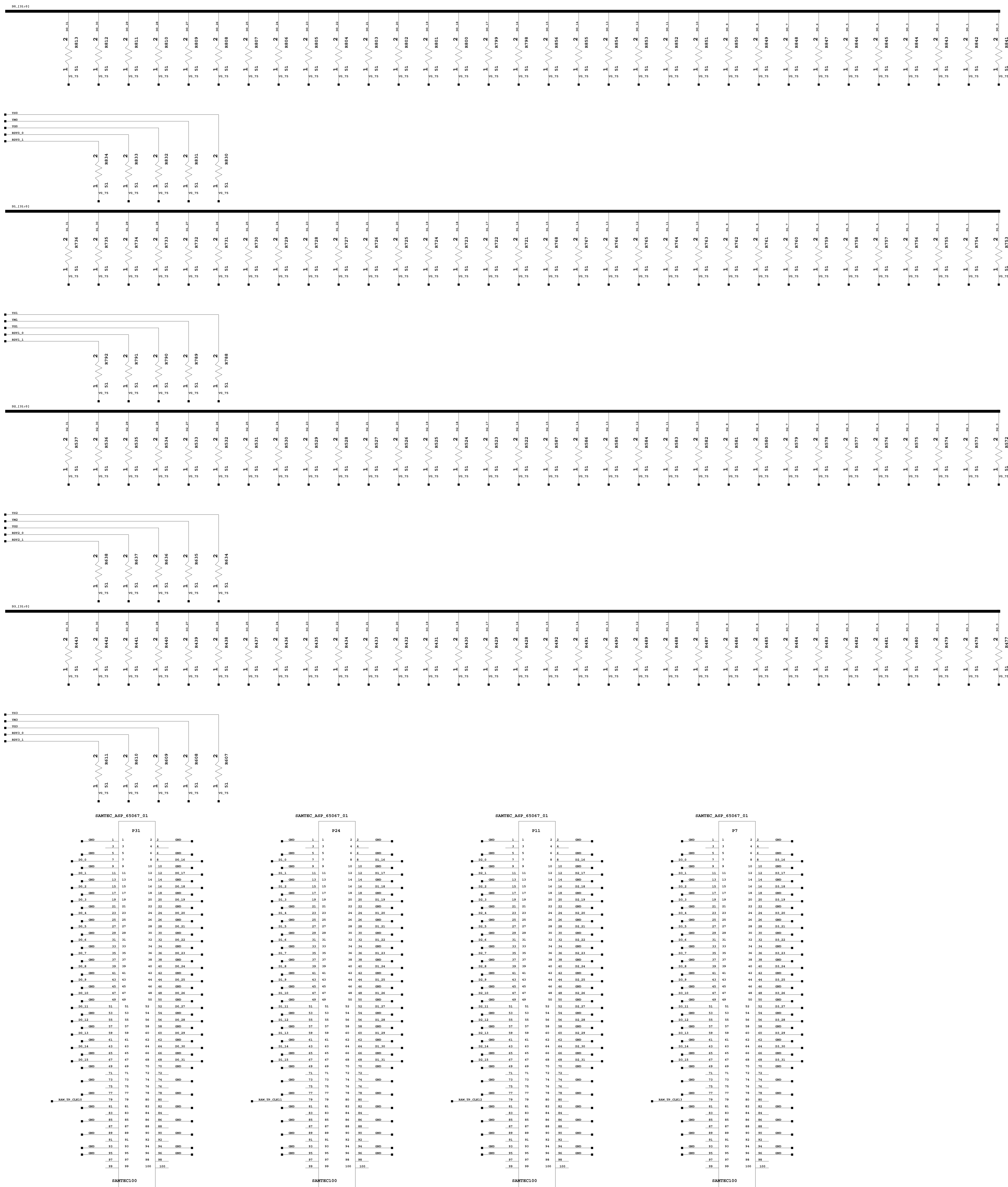
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PROJECT NAME: AMP

SCHEMATIC NAME: BR\_BOT

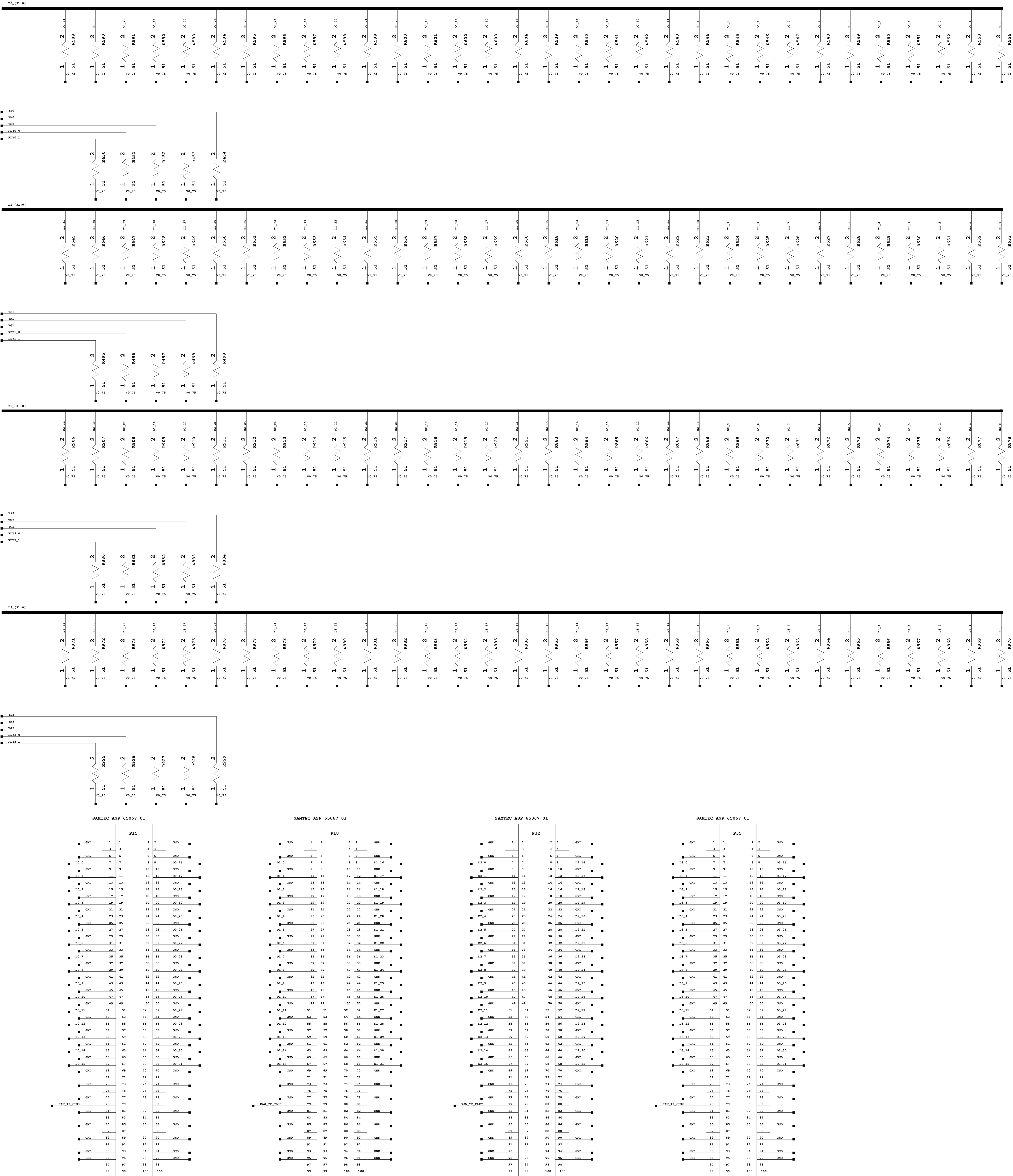


## RAW Bottom Edge Far Termination Resistors





RAW Top Edge Near Termination Resistors



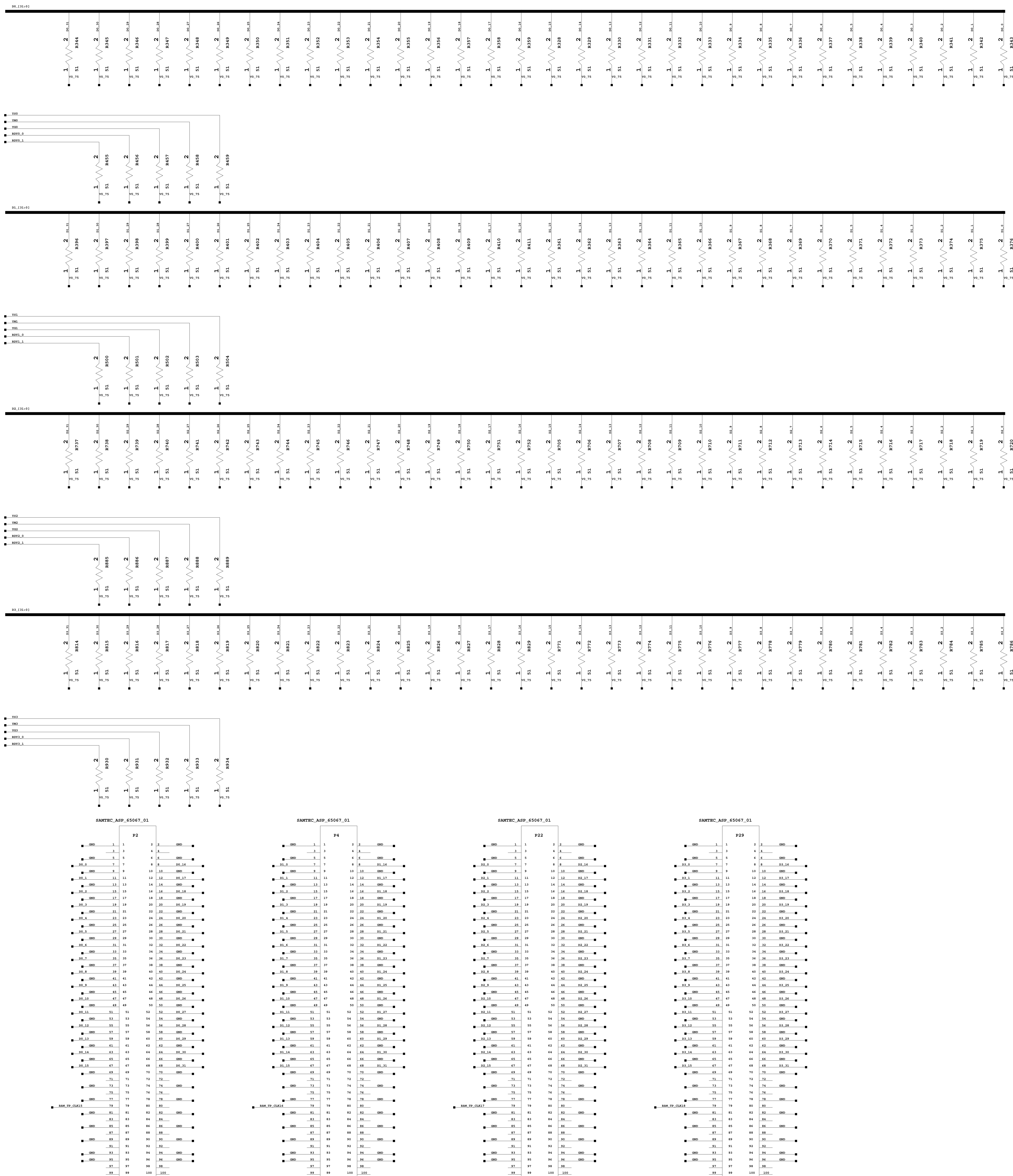
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PROJECT NAME: AMP

SCHEMATIC NAME: BR\_TOP



## RAW Top Edge Far Termination Resistors



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PROJECT NAME: AMP

SCHEMATIC NAME: XBR\_TOP

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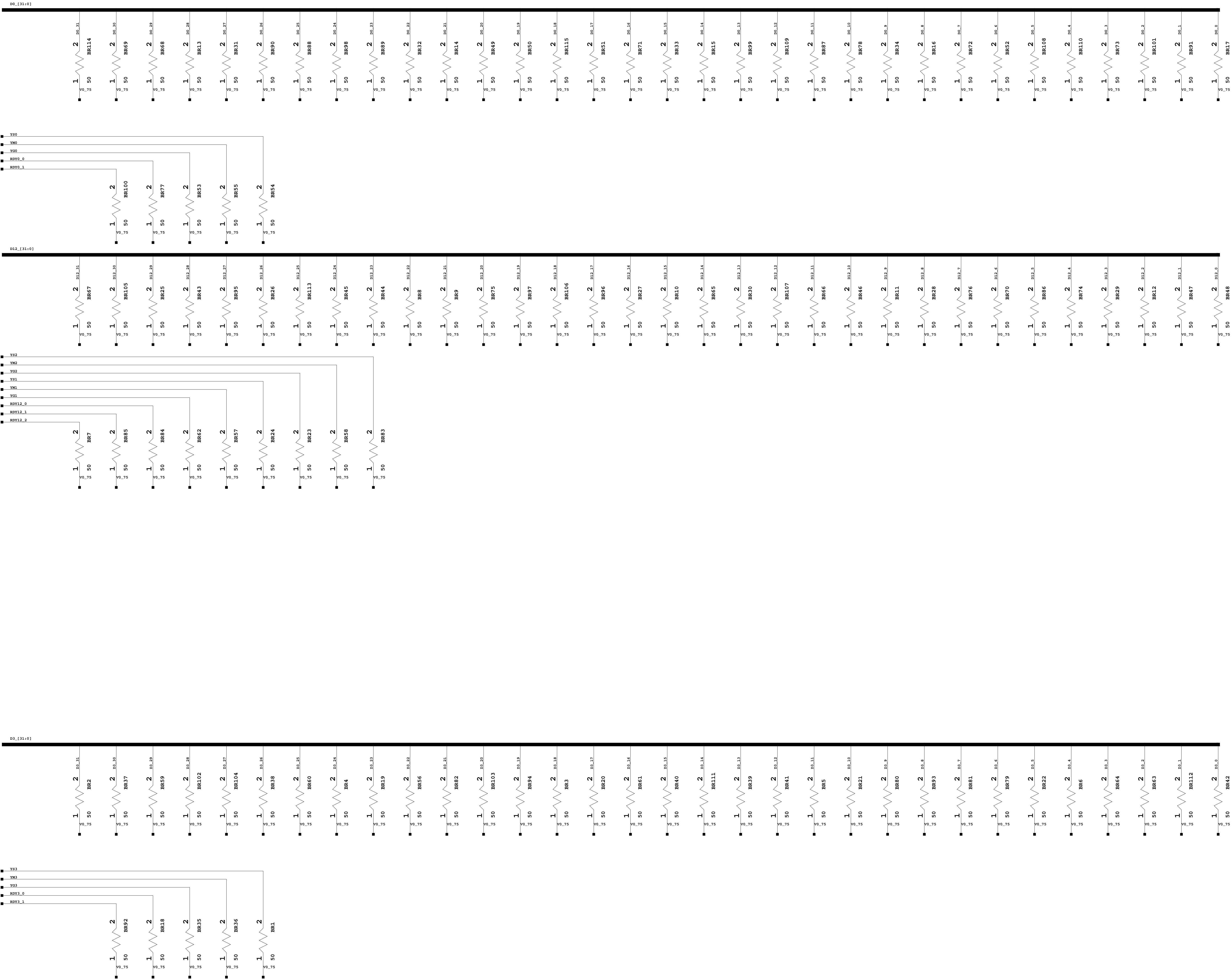
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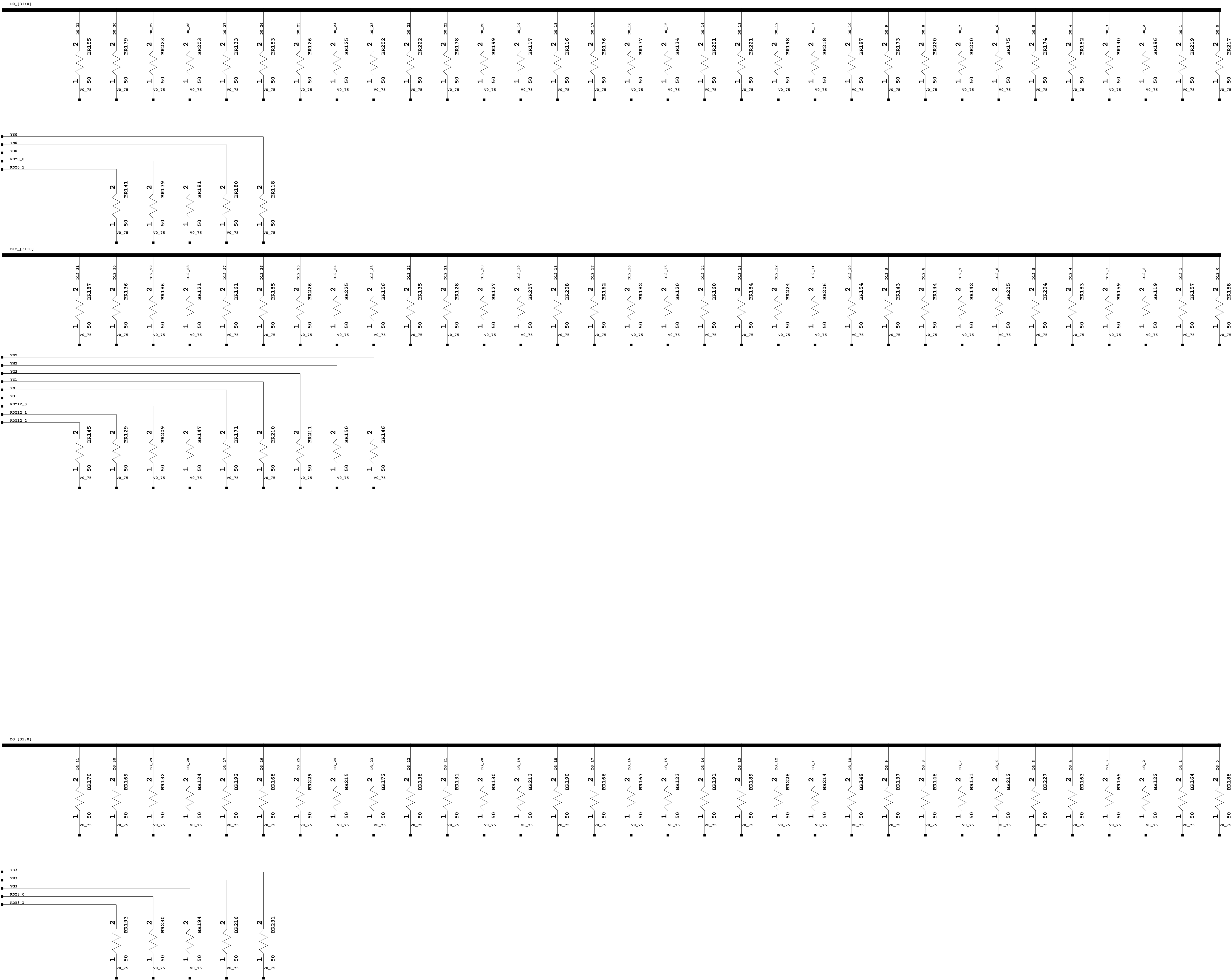


RAW Right Edge Near Termination Resistors





RAW Left Edge Near Termination Resistors



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PROJECT NAME:		AMP
SCHEMATIC NAME:		BR_LEFT
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