



***ASIC SA-27E Databook, Part I
Base Library and I/Os***

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Revision History

Date	Page	Description
6/4/2001	121, 123	Added GTL and 1.5V HSTL DC specifications
6/4/2001	771	Added VDD180DECAP, VDD180DECAP_PM
6/4/2001	662–667	Added BSSTL2C50, BSSTL2C50_PM, BSSTL2C56, BSSTL2C56_PM
6/4/2001	938, 941	Corrected BSSTL2C1T, BSSTL2C2T receiver truth tables
6/4/2001	943–948	Added BSSTL2C50T, BSSTL2C50T_PM, BSSTL2C56T, BSSTL2C56T_PM
3/1/2001	91, 100, 109	Added BATAUDMA, BATAUDMA_PM, BATAUDMAT, BATAUDMAT_PM, IHSTL18TERM, IHSTL18TERM_PM, ILVDSAO, ILVDSAO_PM, ILVDSDAO, and ILVDSDAO_PM
3/1/2001	116	Added "5.0V Tolerant 3.3V LVTTTL Receiver DC Voltage Specifications"
3/1/2001	420	Added CG_DELAY
3/1/2001	474, 475	Added TW_ONE_A, TW_ZERO_A
3/1/2001	481, 781	Corrected BAGP2X4X, BAGP2X4XT 4X driver and receiver delay data
3/1/2001	488	Added BATAUDMA, BATAUDMA_PM
3/1/2001	728	Corrected IHSTLTERM "Combined Driver-Termination Truth Table"
3/1/2001	729	Added IHSTL18TERM, IHSTL18TERM_PM
3/1/2001	731, 734	Corrected ILVDS, ILVDS_PM, ILVDSD, ILVDSD_PM wrap driver truth table
3/1/2001	737–742	Added ILVDSAO, ILVDSAO_PM and ILVDSDAO, ILVDSDAO_PM
3/1/2001	770–773	Updated VDD150DECAP, VDD150DECAP_PM, VDD250DECAP, VDD250DECAP_PM, and VDD330DECAP, VDD330DECAP_PM
3/1/2001	786	Added BATAUDMAT, BATAUDMAT_PM
1/29/2001	128–132	Added PCI-X specifications
1/29/2001	371	Updated LDR0001 setup and hold times

Date	Page	Description
1/10/2001	114	Updated "5.0V Tolerant 3.3V LVTTTL Driver DC Voltage Specifications" table
1/10/2001	116	Added "3.3V Tolerant 2.5V CMOS Receiver DC Voltage Specifications"
12/8/2000	223	Updated INVERT_U cell size
12/8/2000	98, 659–661	Added BSSTL2DIFF, BSSTL2DIFF_PM
12/8/2000	109, 732–733, 735–736	Added ILVDS, ILVDS performance level B
12/8/2000	111, 118, 752–754	Added OHSTL
10/31/2000	320–321	Updated CLKCHP waveform calculation and propagation delays table
10/31/2000	652–653, 655–656	Added V_{dd250} to BSSTL2C1 and BSSTL2C2 driver and receiver propagation delay tables
10/11/2000	36–51	Updated package menus
10/11/2000	70	Updated "Reliability"
10/11/2000	19	Added multiport compilable register arrays minimum voltage
9/20/2000	117, 136	Added "3.3V LVTTTL/5V Tolerant BP33 and IP33 Receiver Input Current/Voltage Curve", SSTL2 DC receiver specifications
9/20/2000	256–259	Added XOR8, XOR9
9/20/2000	446, 448, 450, 454, 455	Corrected F_LPH1001_LPC, F_LPH4001_LPC, F_LPH6001, F_MPH1001_LPC, and F_MPH4001_LPC D-FF operation truth tables
9/20/2000	341	Added DECAP
9/20/2000	607, 610	Added BI2C25, BI2C25_PM and BI2C33, BI2C33_PM
9/20/2000	677	Added BT3350LV, BT3350LV_PM
9/20/2000	694	Added BT3350LVDP, BT3350LVDP_PM
9/20/2000	712	Added BT3350LVPU, BT3350LVPU_PM
9/20/2000	758	Added OLVD18, OLVD18_PM
9/20/2000	764	Added OPECL

Date	Page	Description
9/20/2000	770–773	Added VDD150DECAP, VDD150DECAP_PM, VDD250DECAP, VDD250DECAP_PM, VDD330DECAP, VDD330DECAP_PM
9/20/2000	958	Added BT3350LVT, BT3350LVT_PM
9/20/2000	975	Added BT3350LVPDT, BT3350LVPDT_PM
9/20/2000	993	Added BT3350LVPUT, BT3350LVPUT_PM
9/20/2000	1042	Added IPECLDBDT, IPECLDBDT_PM
7/26/2000	62, 64, 66–66	Updated "Propagation Delays", "Example: Calculating a Propagation Delay", "Latch Setup and Hold Delays (ns)", "Capacitance (in units of Nstd) and Cell Sizes" and "Example: Calculating Propagation Delay and C_L " to reflect new timing models
7/26/2000	138–141	Added STI driver/receiver specifications
7/26/2000	145–1040	Updated timing models throughout
7/26/2000	222–223	Added INVERT performance level U
7/26/2000	230	Added NAND3 performance levels I, J, and K
7/26/2000	251–253, 260–262	Added XOR2, XNOR2 performance levels I, J
7/26/2000	303–304	Added OAI21 performance level H
7/26/2000	319	Updated CLKCHP description
7/26/2000	581–590	Added BGTLD, BGTLD_PM, BGTLS, BGTLS_PM, VGTLR1, VGTLR1_PM, VGTLR2, VGTLR2_PM
7/26/2000	599–604	Added BHSTLC1, BHSTLC1_PM and BHSTLC2, BHSTLC2_PM
7/26/2000	721	Added BUSB2
7/26/2000	749	Added ISTI18D, ISTI18D_PM
7/26/2000	767	Added OSTI18, OSTI18_PM
7/26/2000	879–883	Added BGTLDT, BGTLDT_PM and BGTLS, BGTLS_PM
7/26/2000	893–896	Added BHSTLC1T, BHSTLC1T_PM and BHSTLC2T, BHSTLC2T_PM
4/25/2000	52	Updated "IBM ASICs Design-for-Test Methodology"
4/25/2000	87	Added receiver hysteresis information

Date	Page	Description
4/25/2000	91, 97	Added BAGP4X, BAGP4X_PM, and BPCI5, BPCI5_PM to "Nontest Three-State Common I/Os"
4/25/2000	100	Added BAGP4XT, BAGP4XT_PM
4/25/2000	109–110	Added IHSTL, IHSTL_PM, IHSTLTERM, IHSTLTERM_PM, IPECL, IPECL_PM, IPECLD, IPECLD_PM, IHSTLT, IHSTLT_PM, IPECLT, IPECLT_PM, and IPECLDT, IPECLDT_PM to "Receivers, Standard Cell"
4/25/2000	111	Added "Drivers, Standard Cell"
4/25/2000	112, 1047	Added VDD150_PM_A
4/25/2000	113, 115	Corrected "2.5V CMOS Driver DC Voltage Specifications" and "2.5V CMOS Receiver DC Voltage Specifications"
4/25/2000	114–115	Updated driver minimum DC currents
4/25/2000	118–118	Added PECL receivers and LVDS drivers to "I/O Voltage Requirements"
4/25/2000	125–127	Added OLVDs and OPLVDs driver specification tables
4/25/2000	134–136	Added "PECL Receiver Specifications" and "PECL Receiver Pulse Width Variation Definition"
4/25/2000	483–487	Added BAGP4X, BAGP4X_PM, VAGP4XR1, VAGP4XR1_PM, and VAGP4XR2, VAGP4XR2_PM
4/25/2000	605–606	Added VHSTLR1, VHSTLR1_PM and VHSTLR2, VHSTLR2_PM
4/25/2000	649–650	Added BPCI5, BPCI5_PM
4/25/2000	724–728	Added IHSTL, IHSTL_PM and IHSTLTERM, IHSTLTERM_PM
4/25/2000	743–763	Added IPECL, IPECL_PM, IPECLD, IPECLD_PM, OLVDs, OLVDs_PM, and OPLVDs, OPLVDs_PM
4/25/2000	783–785	Added BAGP4XT, BAGP4XT_PM
4/25/2000	935–936	Added BPCI5T, BPCI5T_PM
4/25/2000	1016–1017	Added IHSTLT, IHSTLT_PM
4/25/2000	1038–1041	Added IPECLT, IPECLT_PM and IPECLDT, IPECLDT_PM
4/25/2000	774	Updated THERMAL, THERMAL_PM
2/11/2000	43–44	Removed regulated supply offering from staggered wire bond EPBGA and HPBGA package menus
2/11/2000	65, 66	Updated estimated values for C_{wire} and metal wiring capacitance



Date	Page	Description
2/11/2000	479	Added BAGP2X4X, BAGP2X4X_PM 4X driver and receiver propagation delays tables
2/11/2000	779	Added BAGP2X4XT, BAGP2X4XT_PM driver and receiver propagation delays tables

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BSSTL2DIFF, BSSTL2DIFF_PM	659
BT3320, BT3320_PM	668
BT3320PD, BT3320PD_PM	685
BT3320PDT, BT3320PDT_PM	966
BT3320PU, BT3320PU_PM	703
BT3320PUT, BT3320PUT_PM	984
BT3320T, BT3320T_PM	949
BT3335, BT3335_PM	671
BT3335PD, BT3335PD_PM	688
BT3335PDT, BT3335PDT_PM	969
BT3335PU, BT3335PU_PM	706
BT3335PUT, BT3335PUT_PM	987
BT3335T, BT3335T_PM	952
BT3350, BT3350_PM	674
BT3350LV, BT3350LV_PM	677
BT3350LVPD, BT3350LVPD_PM	694
BT3350LV PDT, BT3350LV PDT_PM	975
BT3350LVPU, BT3350LVPU_PM	712
BT3350LVPUT, BT3350LVPUT_PM	993
BT3350LVT, BT3350LVT_PM	958
BT3350PD, BT3350PD_PM	691
BT3350PDT, BT3350PDT_PM	972
BT3350PU, BT3350PU_PM	709
BT3350PUT, BT3350PUT_PM	990
BT3350T, BT3350T_PM	955
BT3365, BT3365_PM	679
BT3365PD, BT3365PD_PM	697



BT3365PDT, BT3365PDT_PM	978
BT3365PU, BT3365PU_PM	715
BT3365PUT, BT3365PUT_PM	996
BT3365T, BT3365T_PM	960
BT3390, BT3390_PM	682
BT3390PD, BT3390PD_PM	700
BT3390PDT, BT3390PDT_PM	981
BT3390PU, BT3390PU_PM	718
BT3390PUT, BT3390PUT_PM	999
BT3390T, BT3390T_PM	963
BUFFER	315
BUFFER_G	179
BUSB2	721
CG_AND	419
CG_DELAY	420
CG_OR	421
CLK	317
CLKCHP	319
CLKG	322
CLKGATE	327
CLKGI	324
CLKI	318
CLKSPC	331
CLKSPC_G	181
CLKSPL	335
COMP2	339
D_F_LMX0001	425
D_F_LMX0001_LPC	426
D_F_LPH0001	427
D_F_LPH0001_G	209
D_F_LPH0001_LPC	428
D_F_LPH0002	429
D_F_LPH2021_LPC	430
D_F_LPH4041_LPC	431
D_F_LPH8081	432
D_F_MPH0001_LPC	433
D_F_MPH2021_LPC	434
D_F_MPH4041_LPC	435
D_LDE0001	422
D_LDF0001	423
D_LDR0001	424
DEC24_DP	408
DEC38_DP	409

DECAP	341
DELAY_G	184
DELAY4	342
DELAY6	343
DELAYMUX0	346
DELAYMUXN	344
F_LMX0001	436
F_LMX0001_LPC	438
F_LPH0001	440
F_LPH0001_G	210
F_LPH0001_LPC	442
F_LPH0002	444
F_LPH1001_LPC	446
F_LPH4001_LPC	448
F_LPH6001	450
F_MPH0001_LPC	452
F_MPH0101_LPC	453
F_MPH1001_LPC	454
F_MPH4001_LPC	455
GND_PM_A	1047
IC18D1PUT, IC18D1PUT_PM	1003
IC18D2PUT, IC18D2PUT_PM	1005
IC18DLTPUT, IC18DLTPUT_PM	1006
IC18LTPUT, IC18LTPUT_PM	1007
IC18MCT, IC18MCT_PM	1008
IC18PDT, IC18PDT_PM	1009
IC18PUT, IC18PUT_PM	1010
IC18REPDT, IC18REPDT_PM	1012
IC18RIT, IC18RIT_PM	1013
IC18T, IC18T_PM	1002
IC18TEPDT, IC18TEPDT_PM	1015
IHSTL, IHSTL_PM	724
IHSTL18TERM, IHSTL18TERM_PM	729
IHSTLT, IHSTLT_PM	1016
IHSTLTERM, IHSTLTERM_PM	727
ILVDS, ILVDS_PM	731
ILVDSAO, ILVDSAO_PM	737
ILVDSD, ILVDSD_PM	734
ILVDSDAO, ILVDSDAO_PM	740
ILVDSDT, ILVDSDT_PM	1020
ILVDST, ILVDST_PM	1018
INVERT	222
INVERT_G	149



INVERTBAL	224
IP25D1T, IP25D1T_PM	1023
IP25D2T, IP25D2T_PM	1024
IP25LTT, IP25LTT_PM	1025
IP25MCT, IP25MCT_PM	1026
IP25RET, IP25RET_PM	1027
IP25RIT, IP25RIT_PM	1028
IP25T, IP25T_PM	1022
IP33D1T, IP33D1T_PM	1031
IP33D2T, IP33D2T_PM	1032
IP33LTT, IP33LTT_PM	1033
IP33MCT, IP33MCT_PM	1034
IP33RET, IP33RET_PM	1035
IP33RIT, IP33RIT_PM	1036
IP33T, IP33T_PM	1030
IPECL, IPECL_PM	743
IPECLD, IPECLD_PM	746
IPECLDBDT, IPECLDBDT_PM	1042
IPECLDT, IPECLDT_PM	1040
IPECLT, IPECLT_PM	1038
ISTI18D, ISTI18D_PM	749
L_LTL0001	456
L_MPH0101_LPC	457
L2S0101_LPC	363
LDE0001	366
LDF0001	368
LDR0001	370
LMX0001	372
LMX0001_LPC	374
LPH0001	376
LPH0001_G	203
LPH0001_LPC	378
LPH0002	380
LPH0101	382
LPH0101_G	205
LPH0101_LPC	384
LPH1001_LPC	386
LPH4001_LPC	388
LPH6001	390
LSC0001_LPC	392
LTL0001	394
MCMUX	357
MPH0001_LPC	396

MPH0101_LPC	398
MPH1001_LPC	400
MPH4001_LPC	402
MUX21	348
MUX21_G	185
MUX21BAL	350
MUX21I	352
MUX41	355
MUX41I_DP	411
MUX81I_DP	413
NAND2	225
NAND2_G	150
NAND2BAL	228
NAND3	230
NAND3_G	152
NAND4	233
NAND4_G	153
NOR2	235
NOR2_G	154
NOR3	238
NOR3_G	156
NOR4	240
NOR4_G	157
OA21	293
OA21_G	173
OA22	296
OA22_G	174
OA222	299
OA2222	301
OAI21	303
OAI21_G	175
OAI22	305
OAI22_G	176
OAI222	307
OAI2222	309
OHSTL, OHSTL_PM	752
OLVDS, OLVDS_PM	755
OLVDS18, OLVDS18_PM	758
OPECL	764
OPLVDS, OPLVDS_PM	761
OR2	242
OR2_G	158
OR3	245

OR3_G	160
OR4	248
OR4_G	161
OSTI18, OSTI18_PM	767
PG_LMX0001	458
PG_LMX0001_LPC	460
PG_LPH0001	462
PG_LPH0001_LPC	466
PG_LPH0002	464
PG_LPH1001_LPC	468
PG_LPH4001_LPC	470
PG_LPH6001	472
PSHRDI1_G	187
PSHRDI2_G	189
PSHRLT_G	191
PSHRMC_G	197
PSHRRE_G	193
PSHRRI_G	195
PSRO2PD_A	775
PSRO2PU_PM_A	776
TERM	359
TERM_G	199
THERMAL, THERMAL_PM	774
TTMUX	358
TW_ONE_A	474
TW_ZERO_A	475
VAGP4XR1, VAGP4XR1_PM	486
VAGP4XR2, VAGP4XR2_PM	487
VDD_PM_A	1047
VDD150_PM_A	1047
VDD150DECAP, VDD150DECAP_PM	770
VDD180DECAP, VDD180DECAP_PM	771
VDD250_PM_A	1047
VDD250DECAP, VDD250DECAP_PM	772
VDD330_PM_A	1048
VDD330DECAP, VDD330DECAP_PM	773
VGTLR1, VGTLR1_PM	589
VGTLR2, VGTLR2_PM	590
VHSTL18R1, VHSTL18R1_PM	597
VHSTL18R2, VHSTL18R2_PM	598
VHSTLR1, VHSTLR1_PM	605
VHSTLR2, VHSTLR2_PM	606
VSSTL2R1, VSSTL2R1_PM	657



VSSTL2R2, VSSTL2R2_PM	658
XNOR2	260
XNOR2_G	164
XNOR3	263
XOR2	251
XOR2_G	162
XOR3	254
XOR8	256
XOR9	258

Product Overview



Product Summary

Product Introduction

This databook describes the IBM Microelectronics SA-27E ASIC family, which consists of gate array and standard cell products implemented in a 0.18 μm lithography process. SA-27E utilizes six layers of metal wiring and offers a variety of die sizes capable of handling up to 1124 signal I/Os. Available macros include 1-port and 2-port compilable memory arrays, compilable ROMs, embedded DRAM, 2-port, 3-port, and 4-port compilable register arrays, and a phase-locked loop.

Product Offerings

SA-27E offers as many as 17 die sizes in up to six levels of metal. These die sizes provide a range of wirable gate counts from approximately 334k to 22M. Die/package menus show the supported die/package options and the maximum signal I/Os available for each option (refer to tables 2 through 17).

The lower portion of the die/package menus shows the estimated usable gate count for each die size as a function of metal levels. The actual usable gates will vary depending on design content. Contact your IBM representative for more information.

Table 1. SA-27E General Characteristics

Technology	CMOS 7SF
$L_{\text{effective}}$	0.11 μm
Supply voltage	+1.8V $\pm$ 0.15V standard range, optional 2nd supply for I/Os
Ambient operating temperature range ¹	-40°C to 100°C
Junction temperature range ¹	-55°C to 125°C
Storage temperature range ¹	-65°C to 150°C
Wiring levels	Four - Five - Six
Performance	33 ps (NAND2, fanout = 2, nominal)
Power	0.012 $\mu\text{W}/\text{MHz}/\text{gate}$ (activity factor = approximately 0.1)
1. Certain macros, cores, and embedded arrays have narrower temperature range limits than those listed for the general SA-27E technology. Contact your IBM representative for current macro, core, and embedded DRAM temperature range specifications.	



Table 2. In-line Wire Bond Die/Package Menu: PQFP, LQFP, TQFP, HPQFP, HLQFP (Multiple Supply)

0.50 mm pitch PQFP and HPQFP 4.2 mm max height	Max Signal I/O for Die-Package Combination																		
32 x 32 mm: 240 total leads						196	196	196	196	196	196	196	196	196	196	196	196	196	
28 x 28 mm: 208 total leads					172	172	172	172	172	172	172	172	172	172	172	172	172	172	
0.50 mm pitch LQFP and HLQFP 1.7 mm max height	Max Signal I/O for Die-Package Combination																		
24 x 24 mm: 176 total leads				144	144	144	144	144	144	144	144	144	144	144	144	144	144	144	
20 x 20 mm: 144 total leads		120	120	120	120	120	120	120	120	120	120	120	120	120	120	120			
14 x 14 mm: 100 total leads		84	84	84	84	84	84	84	84	84	84								
0.50 mm pitch TQFP 1.2 mm max height	Max Signal I/O for Die-Package Combination																		
20 x 20 mm: 144 total leads		120	120	120	120	120	120	120	120	120	120	120							
14 x 14 mm: 100 total leads		84	84	84	84	84	84	84	84	84	84								
12 x 12 mm: 80 total leads	68	68	68	68	68	68	68	68											
Die Metal Layers	Wirable Gates ² (Thousands) for Die-Size Metal Layer Combinations																		
4	334	508	609	837	965	1248	1403	1740	1923	2315	2524	2971	3207	3708	3973	4528	4819	5429	5747
5	430	592	695	956	1100	1430	1600	1990	2200	2650	2890	3400	3670	4240	4540	5180	5510	6210	6570
6	430	654	783	1080	1240	1580	1720	2110	2340	2810	3070	3610	3890	4500	4830	5500	5850	6590	6980
1. In-line wire bond footprint, 67.20 μm pitch. Package height is measured from seating plane to highest point on top surface of plastic body. 2. Actual usable gate count varies depending on the design content. 3. QFP package offerings shown support core and four additional power zones. 4. PQFP and HPQFP package offerings are JEDEC level 3 moisture sensitivity. LQFP, HLQFP, and TQFP package offerings are JEDEC level 4 moisture sensitivity. All QFP package offerings are reliability grade 3. 5. Contact your IBM representative for additional and most up-to-date information, including custom offerings.																			



Table 3. In-line Wire Bond Die/Package Menu: PQFP, LQFP, TQFP, HPQFP, HLQFP (Regulated Supply)

0.50 mm pitch PQFP and HPQFP 4.2 mm max height	Max Signal I/O for Die-Package Combination																		
32 x 32 mm: 240 total leads						204	204	204	204	204	204	204	204	204	204	204	204	204	
28 x 28 mm: 208 total leads					180	180	180	180	180	180	180	180	180	180	180	180	180	180	
0.50 mm pitch LQFP and HLQFP 1.7 mm max height	Max Signal I/O for Die-Package Combination																		
24 x 24 mm: 176 total leads				152	152	152	152	152	152	152	152	152	152	152	152	152	152	152	
20 x 20 mm: 144 total leads		128	128	128	128	128	128	128	128	128	128	128	128	128	128	128			
14 x 14 mm: 100 total leads		88	88	88	88	88	88	88	88	88	88								
0.50 mm pitch TQFP 1.2 mm max height	Max Signal I/O for Die-Package Combination																		
20 x 20 mm: 144 total leads		128	128	128	128	128	128	128	128	128	128								
14 x 14 mm: 100 total leads		88	88	88	88	88	88	88	88	88	88								
Die Metal Layers	Wirable Gates ² (Thousands) for Die-Size Metal Layer Combinations																		
4	334	508	609	837	965	1248	1403	1740	1923	2315	2524	2971	3207	3708	3973	4528	4819	5429	5747
5	430	592	695	956	1100	1430	1600	1990	2200	2650	2890	3400	3670	4240	4540	5180	5510	6210	6570
6	430	654	783	1080	1240	1580	1720	2110	2340	2810	3070	3610	3890	4500	4830	5500	5850	6590	6980
1. In-line wire bond footprint, 67.20 μm pitch. Package height is measured from seating plane to highest point on top surface of plastic body. 2. Actual usable gate count varies depending on the design content. 3. QFP package offerings shown support a regulated supply. 4. PQFP and HPQFP package offerings are JEDEC level 3 moisture sensitivity. LQFP, HLQFP, and TQFP package offerings are JEDEC level 4 moisture sensitivity. All QFP package offerings are reliability grade 3. 5. Contact your IBM representative for additional and most up-to-date information, including custom offerings.																			



Table 4. In-line Wire Bond Die/Package Menu: TFBGA¹ (Multiple Supply)

0.80 mm pitch TFBGA 1.2 mm max height		Max Signal I/O for Die-Package Combination																	
14 x 14 mm: 220 total balls						180	180	180	180	180									
14 x 14 mm: 192 total balls				156	156	156	156	156	156	156									
12 x 12 mm: 180 total balls					144	144	144	144	144	144									
12 x 12 mm: 160 total balls				132	132	132	132	132	132	132									
10 x 10 mm: 112 total balls	88	88	88	88	88	88	88	88	88	88									
0.50 mm pitch TFBGA 1.2 mm max height		Max Signal I/O for Die-Package Combination																	
12 x 12 mm: 220 total balls						180	180	180	180	180									
10 x 10 mm: 180 total balls					144	144	144	144	144	144									
8 x 8 mm: 132 total balls	104	104	104	104	104	104	104	104	104	104									
8 x 8 mm: 96 total balls	80	80	80	80	80	80	80	80	80	80									
Die Metal Layers		Wireable Gates ⁴ (Thousands) for Die-Size Metal Layer Combinations																	
4	334	508	609	837	965	1248	1403	1740	1923	2315	2524	2971	3207	3708	3973	4528	4819	5429	5747
5	430	592	695	956	1100	1430	1600	1990	2200	2650	2890	3400	3670	4240	4540	5180	5510	6210	6570
6	430	654	783	1080	1240	1580	1720	2110	2340	2810	3070	3610	3890	4500	4830	5500	5850	6590	6980
1. TFBGA is a custom offering. Contact your IBM representative for information. 2. In-line wire bond footprint, 67.20 µm pitch. 3. Package height is measured from seating plane to highest point on top surface of plastic body. 4. Actual usable gate count varies depending on the design content. 5. TFBGA package offerings shown support core and four additional power zones. 6. TFBGA package offerings are JEDEC level 3 moisture sensitivity. TFBGA package offerings shown are reliability grade 3. 7. Contact your IBM representative for additional and most up-to-date information, including custom offerings.																			



Table 5. In-line Wire Bond Die/Package Menu: TFBGA¹ (Regulated Supply)

0.80 mm pitch TFBGA 1.2 mm max height		Max Signal I/O for Die-Package Combination																	
14 x 14 mm: 220 total balls					192	192	192	192	192										
14 x 14 mm: 192 total balls			168	168	168	168	168	168	168										
12 x 12 mm: 180 total balls				156	156	156	156	156	156										
12 x 12 mm: 160 total balls			140	140	140	140	140	140	140										
10 x 10 mm: 112 total balls	96	96	96	96	96	96	96	96	96										
0.50 mm pitch TFBGA 1.2 mm max height		Max Signal I/O for Die-Package Combination																	
12 x 12 mm: 220 total balls					192	192	192	192	192										
10 x 10 mm: 180 total balls			156	156	156	156	156	156	156										
8 x 8 mm: 132 total balls	112	112	112	112	112														
8 x 8 mm: 96 total balls	84	84	84	84	84														
Die Metal Layers		Wireable Gates ⁴ (Thousands) for Die-Size Metal Layer Combinations																	
4	334	508	609	837	965	1248	1403	1740	1923	2315	2524	2971	3207	3708	3973	4528	4819	5429	5747
5	430	592	695	956	1100	1430	1600	1990	2200	2650	2890	3400	3670	4240	4540	5180	5510	6210	6570
6	430	654	783	1080	1240	1580	1720	2110	2340	2810	3070	3610	3890	4500	4830	5500	5850	6590	6980
1. TFBGA is a custom offering. Contact your IBM representative for information. 2. In-line wire bond footprint, 67.20 μm pitch. 3. Package height is measured from seating plane to highest point on top surface of plastic body. 4. Actual usable gate count varies depending on the design content. 5. TFBGA package offerings shown support a regulated supply. 6. TFBGA package offerings are JEDEC level 3 moisture sensitivity. TFBGA package offerings are reliability grade 3. 7. Contact your IBM representative for additional and most up-to-date information, including custom offerings.																			



Table 6. In-line Wire Bond Die/Package Menu: PBGA (Regulated Supply)

1.27 mm pitch PBGA (2SOP, 2S2P)		Thermal Balls	Max Signal I/O for Die-Package Combination															
37.5 x 37.5 mm: 529 total balls		49															384	384
35 x 35 mm: 388 total balls		36													304	304	304	304
35 x 35 mm: 313 total balls		n/a												280	280	280	280	280
27 x 27 mm: 292 total balls		36										231	231	231	231	231	231	231
Die Metal Layers			Wireable Gates ² (Thousands) for Die-Size Metal Layer Combinations															
4			965	1248	1403	1600	1740	1923	2315	2524	2971	3207	3708	3973	4528	4819	5429	5747
5			1100	1430	1600	1990	2200	2650	2890	3400	3670	4240	4540	5180	5510	6210	6570	
6			1240	1580	1720	2110	2340	2810	3070	3610	3890	4500	4830	5500	5850	6590	6980	

1. In-line wire bond footprint, 67.20 μ m effective pitch.

2. Actual usable gate count varies depending on the design content.

3. PBGA supports a regulated supply only.

4. PBGA package offerings are JEDEC level 3 moisture sensitivity. PBGA package offerings are reliability grade 3.

5. PBGA package offerings can be either 2SOP or 2S2P designs.

6. Thermal balls are optional for PBGA. Total ball count includes thermal balls.

7. Contact your IBM representative for additional and most up-to-date information, including custom offerings.



Table 7. In-line Wire Bond Die-Package Menu: EPBGA (Multiple or Regulated Supply)

1.27 mm pitch EPBGA (252P)	Ball Rows	Thermal Balls	Max Signal I/O for Die-Package Combination									
40 x 40 mm: 569 total balls	5	49									392	392
37.5 x 37.5 mm: 529 total balls	5	49									360	360
35 x 35 mm: 456 total balls	5	36							316	316	316	316
31 x 31 mm: 385 total balls	5	25						268	268	268	268	268
27 x 27 mm: 316 total balls	5	16	228	228	228	228	228	228	228	228	228	228
1.00 mm pitch EPBGA (252P)	Ball Rows	Thermal Balls										
37.5 x 37.5 mm: 612 total balls	4	100									392	392
35 x 35 mm: 580 total balls	4	100									360	360
31 x 31 mm: 480 total balls	4	64							316	316	316	316
27 x 27 mm: 388 total balls	4	36						268	268	268	268	268
23 x 23 mm: 324 total balls	4	36	216	216	216	216	216	216	216	216	216	216
1.00 mm pitch EPBGA (252P)	Ball Rows	Thermal Balls										
31 x 31 mm: 564 total balls	5	64									384	384
27 x 27 mm: 456 total balls	5	36							316	316	316	316
23 x 23 mm: 376 total balls	5	36					256	256				
Die Metal Layers			Wireable Gates ² (Thousands) for Die-Size Metal Layer Combinations									
4			1923	2315	2524	2971	3207	3708	3973	4528	4819	5747
			2200	2650	2890	3400	3670	4240	4540	5180	5510	6570
6			2340	2810	3070	3610	3890	4500	4830	5500	5850	6980
1. In-line wire bond footprint, 67.20 μm effective pitch. Total ball counts include thermal balls. 2. Actual usable gate count varies depending on the design content. 3. EPBGA package offerings support core and four additional power zones, or a regulated supply. 4. EPBGA package offerings are JEDEC level 3 moisture sensitivity. EPBGA package offerings are reliability grade 3. 5. Contact your IBM representative for additional and most up-to-date information, including custom offerings.												



Table 8. In-line Wire Bond Die-Package Menu: HPBGA (Multiple or Regulated Supply)

1.27 mm pitch HPBGA (2S2P)		Ball Rows	Max Signal I/O for Die-Package Combination															
31 x 31 mm: 304 total balls		4								228	228							
42.5 x 42.5 mm: 540 total balls		5														404	404	
40 x 40 mm: 520 total balls		5														392	392	
37.5 x 37.5 mm: 480 total balls		5													360	360	360	
35 x 35 mm: 420 total balls		5												316	316			
1.00 mm pitch HPBGA (2S2P)		Ball Rows	Max Signal I/O for Die-Package Combination															
37.5 mm x 37.5 mm: 512 total balls		4														392	392	
35 mm x 35 mm: 480 total balls		4														360	360	
31 mm x 31 mm: 416 total balls		4											316	316	316	316	316	
27 mm x 27 mm: 352 total balls		4									268	268						
31 mm x 31 mm: 500 total balls		5														384	384	
Die Metal Layers		Wirable Gates ² (Thousands) for Die-Size Metal Layer Combinations																
4		965	1248	1403	1740	1923	2315	2524	2971	3207	3708	3973	4528	4819	5429	5747		
5		1100	1430	1600	1990	2200	2650	2890	3400	3670	4240	4540	5180	5510	6210	6570		
6		1240	1580	1720	2110	2340	2810	3070	3610	3890	4500	4830	5500	5850	6590	6980		
1. In-line wire bond footprint, 67.20 μm effective pitch. 2. Actual usable gate count varies depending on the design content. 3. HPBGA package offerings support core and four additional power zones, or a regulated supply. 4. HPBGA package offerings are JEDEC level 3 moisture sensitivity. HPBGA package offerings are reliability grade 3. 5. Contact your IBM representative for additional and most up-to-date information, including custom offerings.																		

1. In-line wire bond footprint, 67.20 µm effective pitch.
2. Actual usable gate count varies depending on the design content.
3. HPBGA package offerings support core and four additional power zones, or a regulated supply.
4. HPBGA package offerings are JEDEC level 3 moisture sensitivity. HPBGA package offerings are reliability grade 3.
5. Contact your IBM representative for additional and most up-to-date information, including custom offerings.



Table 9. Staggered Wire Bond Die-Package Menu: EPBGA (Multiple Supply)

1.27 mm pitch EPBGA (2S2P)		Thermal Balls	Max Signal I/O for Die-Package Combination																	
40 x 40 mm: 569 total balls	5	49													392	392	392	392	392 ³	392 ³
37.5 x 37.5 mm: 529 total balls	5	49														360	360	360	360	360 ³
35 x 35 mm: 456 total balls	5	36							316	316	316	316	316	316	316	316	316 ³	316 ³	316 ³	316 ³
31 x 31 mm: 385 total balls	5	25							268	268	268	268	268	268	268	268	268 ³	268 ³	268 ³	268 ³
27 x 27 mm: 316 total balls	5	16	228	228	228	228	228 ³	228 ³	228 ³	228 ³	228 ³	228 ³	228 ³	228 ³	228 ³	228 ³	228 ³	228 ³	228 ³	228 ³
1.00 mm pitch EPBGA (2S2P)		Thermal Balls	Max Signal I/O for Die-Package Combination																	
37.5 x 37.5 mm: 612 total balls	4	100															392	392	392	392 ³
35 x 35 mm: 580 total balls	4	100														360	360	360	360	360 ³
31 x 31 mm: 480 total balls	4	64							316	316	316	316	316	316	316	316	316 ³	316 ³	316 ³	316 ³
27 x 27 mm: 388 total balls	4	36							268	268	268	268	268	268	268	268	268 ³	268 ³	268 ³	268 ³
23 x 23 mm: 324 total balls	4	36	216	216	216	216	216 ³	216 ³	216 ³	216 ³	216 ³	216 ³	216 ³	216 ³	216 ³	216 ³	216 ³	216 ³	216 ³	216 ³
31 x 31 mm: 564 total balls	5	64															384	384	384	384 ³
27 x 27 mm: 456 total balls	5	36							316	316	316	316	316	316	316	316	316 ³	316 ³	316 ³	316 ³
23 x 23 mm: 376 total balls	5	36							256	256	256	256	256	256	256	256 ³	256 ³			
Die Metal Layers		Wireable Gates ⁴ (Thousands) for Die-Size Metal Layer Combinations																		
5		846	1084	1259	1546	1754	2089	2330	2715	2988	3422	3727	4210	4549	5081	5452				
6		967	1240	1440	1770	2000	2390	2660	3100	3420	3910	4260	4810	5200	5810	6230				
1. Staggered wire bond footprint, 40.32 µm effective pitch. 2. Total ball counts include thermal balls. 3. Custom offering. Contact your IBM representative for more information. 4. Actual usable gate count varies depending on the design content. 5. EPBGA package offerings shown support core and four additional power zones. 6. EPBGA package offerings are JEDEC level 3 moisture sensitivity. EPBGA package offerings are reliability grade 3. 7. Contact your IBM representative for additional and most up-to-date information.																				



Table 10. Staggered Wire Bond Die-Package Menu: HPBGA (Multiple Supply)

1.27 mm pitch HPBGA (2S2P)		Max Signal I/O for Die-Package Combination												Ball Rows	
		228	228	228	228	228 ²	228 ²	228 ²							
31 mm x 31 mm: 304 total balls	4														436
45 x 45 mm: 580 total balls	5														404 ² 392 ²
42.5 x 42.5 mm: 540 total balls	5										404	404	404		404 ² 392 ²
40 x 40 mm: 520 total balls	5										392	392	392		392 ² 360 ²
37.5 x 37.5 mm: 480 total balls	5								360	360	360	360	360 ²		360 ² 316 ²
35 x 35 mm: 420 total balls	5								316	316	316	316	316 ²		
1.00 mm pitch HPBGA (2S2P)		Max Signal I/O for Die-Package Combination												Ball Rows	
40 mm x 40 mm: 560 total balls	4														420
37.5 mm x 37.5 mm: 512 total balls	4									392	392	392	392		392 ² 360 ²
35 mm x 35 mm: 480 total balls	4								360	360	360	360	360 ²		360 ² 316 ²
31 mm x 31 mm: 416 total balls	4								316	316	316	316 ²	316 ²		316 ² 268 ²
27 mm x 27 mm: 352 total balls	4								268	268	268	268 ²	268 ²		
35 mm x 35 mm: 580 total balls	5														436
31 mm x 31 mm: 500 total balls	5										384	384	384		384
27 mm x 27 mm: 420 total balls	5								316	316	316	316			
Die Metal Layers		Wireable Gates ³ (Thousands) for Die-Size Metal Layer Combinations													
		846	1084	1259	1546	1754	2089	2330	2715	2988	3422	3727	4210	4549	5081
5															5452
6		967	1240	1440	1770	2000	2390	2660	3100	3420	3910	4260	4810	5200	5810
															6230

1. Staggered wire bond footprint, 40.32 µm effective pitch.
2. Custom offering. Contact your IBM representative for more information.
3. Actual usable gate count varies depending on the design content.
4. HPBGA package offerings shown support core and four additional power zones.
5. HPBGA package offerings are JEDEC level 3 moisture sensitivity. HPBGA package offerings are reliability grade 3.
6. Contact your IBM representative for additional and most up-to-date information.



Table 11.1. Peripheral C4 Plastic Flip Chip Die-Package Menu: FC-PBGA

1.27 mm pitch FC-PBGA		Max Signal I/O for Die-Package Combination															
42.5 x 42.5 mm: 1088 total balls						648	704	728	728	704							
40 x 40 mm: 960 total balls						536	592	648	640	640	592						
37.5 x 37.5 mm: 840 total balls						536	572	572	532	532							
35 x 35 mm: 728 total balls				424	480	491	451	451	451								
33 x 33 mm: 624 total balls		312	368	416	416	400	400										
27 x 27 mm: 399 total balls	256	260	260	260													
1.00 mm pitch FC-PBGA		Max Signal I/O for Die-Package Combination															
42.5 x 42.5 mm: 1680 total balls									760	816	872						
40 x 40 mm: 1520 total balls								648	704	760	816	872					
37.5 x 37.5 mm: 1295 total balls							592	648	704	760	816	788					
35 x 35 mm: 1155 total balls					480	536	592	648	704	720	720						
33 x 33 mm: 1023 total balls				424	480	536	592	648	624								
27 x 27 mm: 675 total balls	256	312	368	424	432	432											
Die Metal Layers		Wireable Gates ¹ (Millions) for Die-Size Metal Layer Combinations															
5	1.50	2.076	2.745	3.508	4.364	5.314	6.357	7.493	8.723	10.05	11.46	12.97	14.58	16.27	18.06	19.95	21.92
6	1.55	2.14	2.84	3.59	4.45	5.41	6.46	7.61	8.85	10.18	11.60	13.12	14.73	16.44	18.24	20.13	22.12

1. Actual usable gate count varies depending on the design content.

2. FC-PBGA package offerings support core and four additional power zones.

3. FC-PBGA package offerings are JEDEC level 4 moisture sensitivity. FC-PBGA package offerings are reliability grade 3.

4. Max T_j = 115°C.

5. Up to eight on-package 47 nF decoupling capacitors can be supported.

6. The FC-PBGA package is only available with a lid.

7. Contact your IBM representative for additional and most up-to-date information, including custom offerings.

Table 12. Area Array C4 Organic Die-Package Menu: Single Dense Footprint HyperBGA™

1.27 mm pitch HyperBGA	Max Signal I/O for Die-Package Combination												
42.5 x 42.5 mm: 1088 total balls							640	748	748	748	748	748	748
40 x 40 mm: 960 total balls							640	664	664	664	664		
37.5 x 37.5 mm: 840 total balls							576	576	576	576	576		
35 x 35 mm: 728 total balls							500	500	500	500	500		
33 x 33 mm: 624 total balls						412	456	456	456	456			
1.00 mm pitch HyperBGA	Max Signal I/O for Die-Package Combination												
42.5 x 42.5 mm: 1657 total balls								756	872	996	1124	1124	1124
40 x 40 mm: 1497 total balls								756	872	996	1024	1024	1024
37.5 x 37.5 mm: 1272 total balls								756	872	876	876	876	876
35 x 35 mm: 1132 total balls								756	780	780	780	780	
33 x 33 mm: 937 total balls							640	644	644	644			
Die Metal Layers	Wirable Gates ¹ (Millions) for Die-Size Metal Layer Combinations												
6	2.673	3.396	4.212	5.117	6.308	7.686	9.182	10.78	12.33	13.98	15.74	17.82	20.01
- Actual usable gate count varies depending on the design content. - HyperBGA package offerings are JEDEC level 4 moisture sensitivity. HyperBGA package offerings are reliability grade 3 (grade 1 offerings in limited availability). - HyperBGA package offerings support core and four additional power zones. - Up to 8 on-package 56 nF decoupling capacitors can be supported. - The HyperBGA package is only available with a lid. - Contact your IBM representative for additional and most up-to-date information, including custom offerings.													





Table 13. Area Array C4 Organic Die-Package Menu: Double Dense Footprint HyperBGA

1.27 mm pitch HyperBGA	Max Signal I/O for Die-Package Combination									
		548	702	748	748	748	748			
42.5 x 42.5 mm: 1088 total balls										
40 x 40 mm: 960 total balls			548	664	664	664	664			
37.5 x 37.5 mm: 840 total balls			548	576	576	576	576			
35 x 35 mm: 728 total balls			410	500	500	500	500			
33 x 33 mm: 624 total balls	288	410	456	456	456	456	456			
1.00 mm pitch HyperBGA	Max Signal I/O for Die-Package Combination									
								884	1000	1124
42.5 x 42.5 mm: 1657 total balls										
40 x 40 mm: 1497 total balls								884	1000	1024
37.5 x 37.5 mm: 1272 total balls			548	702	748	748	748			
35 x 35 mm: 1132 total balls			548	702	748	748	748			
33 x 33 mm: 937 total balls			548	644	644	644	644			
Die Metal Layers		Wireable Gates ¹ (Millions) for Die-Size Metal Layer Combinations								
6		2.673	3.396	4.212	5.117	6.308	7.686	9.182	10.78	12.33
									13.98	15.74
									17.82	20.01
										22.32

1. Actual usable gate count varies depending on the design content.
2. HyperBGA package offerings are JEDEC level 4 moisture sensitivity. HyperBGA package offerings are reliability grade 3 (grade 1 offerings in limited availability).
3. HyperBGA package offerings support core and four additional power zones.
4. Up to 8 on-package 56 nF decoupling capacitors can be supported.
5. The HyperBGA package is only available with a lid.
6. Contact your IBM representative for additional and most up-to-date information, including custom offerings.



Table 14. Peripheral C4 Ceramic Flip Chip Die-Package Menu: CBGA

1.27 mm pitch CBGA		Max Signal I/O for Die-Package Combination: 9-layer Package													
32.5 x 32.5 mm: 624 total balls			340	384	432	467	467	467	467	467	467	467	467	467	467
25 x 32.5 mm: 474 total balls		288	340	353	353	353	353	353	353						
25 x 25 mm: 360 total balls	240	271	271												
21 x 21 mm: 255 total balls	191	191													
1.27 mm pitch CBGA		Max Signal I/O for Die-Package Combination: 10-Layer Package													
32.5 x 32.5 mm: 624 total balls			368	424	467										
25 x 32.5 mm: 474 total balls		312													
25 x 25 mm: 360 total balls	256														
1.00 mm pitch CBGA		Max Signal I/O for Die-Package Combination: 9-layer Package													
32.5 x 32.5 mm: 937 total balls							528	576	624	692	701	701	701	701	701
25 x 32.5 mm: 720 total balls					432	480	528	540	540	540					
25 x 25 mm: 552 total balls			340	384	412	412	412								
1.00 mm pitch CBGA		Max Signal I/O for Die-Package Combination: 10-Layer Package													
32.5 x 32.5 mm: 937 total balls							592	648	701	701	701	701	701		
25 x 32.5 mm: 720 total balls					480	536	540								
25 x 25 mm: 552 total balls			368	412											
Die Metal Layers 9- and 10-Layer Package		Wireable Gates ¹ (Millions) for Die-Size Metal Layer Combinations													
5	1.50	2.076	2.745	3.508	4.364	5.314	6.357	7.493	8.723	10.05	11.46	12.97	14.58		
6	1.55	2.14	2.84	3.59	4.45	5.41	6.46	7.61	8.85	10.18	11.60	13.12	14.73		

1. Actual usable gate count varies depending on the design content.
2. CBGA package offerings are JEDEC level 1 or JEDEC level 2 moisture sensitivity. CBGA package offerings are reliability grade 3 (grade 1 offerings in limited availability).
3. CBGA package offerings support core and four additional power zones.
4. Direct lid attach (DLA) available for thermal enhancement. DLA is not qualified for use on die sizes smaller than 6.5 mm.
5. Up to 8 on-package 56 nF decoupling capacitors can be supported.
6. Contact your IBM representative for additional and most up-to-date information, including custom offerings.



Table 15. Peripheral C4 Ceramic Flip Chip Die-Package Menu: CCGA

1.27 mm pitch CCGA		Max Signal I/O for Die-Package Combination: 9-layer Package															
42.5 x 42.5 mm: 1088 total columns						624	692	720	768	815	815	815	815	815	815	815	815
32.5 x 42.5 mm: 824 total columns			432	480	528	576	619	619									
32.5 x 32.5 mm: 624 total columns	340	384	432	467	467	467	467	467	467	467	467						
1.27 mm pitch CCGA		Max Signal I/O for Die-Package Combination: 10-Layer Package															
42.5 x 42.5 mm: 1088 total columns						704	760	815	815								
32.5 x 42.5 mm: 824 total columns			480	536	592	619											
32.5 x 32.5 mm: 624 total columns	368	424	467														
1.00 mm pitch CCGA		Max Signal I/O for Die-Package Combination: 9-layer Package															
42.5 x 42.5 mm: 1657 total columns									768	816	864	912	960	1008			
32.5 x 42.5 mm: 1247 total columns									624	692	720	768	816	864	912	931	931
32.5 x 32.5 mm: 937 total columns								528	576	624	692	701	701	701			
1.00 mm pitch CCGA		Max Signal I/O for Die-Package Combination: 10-Layer Package															
42.5 x 42.5 mm: 1657 total columns												872	928	984	1040	1096	1152
32.5 x 42.5 mm: 1247 total columns											704	760	816	872	928	931	931
32.5 x 32.5 mm: 937 total columns											592	648	701	701			
Die Metal Layers 9- and 10-Layer Package		Wirable Gates ¹ (Millions) for Die-Size Metal Layer Combinations															
5	2.745	3.508	4.364	5.314	6.357	7.493	8.723	10.05	11.46	12.97	14.58	16.27	18.06	19.95	21.92		
6	2.84	3.59	4.45	5.41	6.46	7.61	8.85	10.18	11.60	13.12	14.73	16.44	18.24	20.13	22.12		
1. Actual usable gate count varies depending on the design content. 2. CCGA package offerings are JEDEC level 1 moisture sensitivity. CCGA package offerings are reliability grade 3 offerings (grade 1 offerings in limited availability). 3. Direct lid attach (DLA) is available for thermal enhancement. 4. CCGA package offerings support core and four additional power zones. 5. Up to 8 on-package 56 nF decoupling capacitors can be supported. 6. Contact your IBM representative for additional and most up-to-date information., including custom offerings.																	

Table 16. Area Array C4 Ceramic Die-Package Menu: Single Dense Footprint CBGA and CCGA

1.27 mm pitch CBGA	Number of Layers	Max Signal I/O for Die-Package Combination							
32.5 x 32.5 mm: 624 total balls	13	456	456	456	456	456			
1.27 mm pitch CCGA	Number of Layers	Max Signal I/O for Die-Package Combination							
42.5 x 42.5 mm: 1088 total columns	17		748	748	748	748	748	748	748
32.5 x 42.5 mm: 824 total columns	15		512	512	512	512			
32.5 x 32.5 mm: 624 total columns	13	456	456	456	456	456			
1.00 mm pitch CCGA	Number of Layers	Max Signal I/O for Die-Package Combination							
42.5 x 42.5 mm: 1657 total columns	19			872	996	1124	1124	1124	1124
32.5 x 42.5 mm: 1247 total columns	19		756	846	846	846	846	846	846
Die Metal Layers		Wirable Gates ¹ (Millions) for Die-Size Metal Layer Combinations							
6		9.182	10.78	12.33	13.98	15.74	17.82	20.01	22.32
- Actual usable gate count varies depending on the design content. - CBGA package offerings are JEDEC level 1 or JEDEC level 2 moisture sensitivity. CCGA package offerings are JEDEC level 1 moisture sensitivity. CBGA and CCGA package offerings are reliability grade 3 (grade 1 offerings in limited availability). - CBGA and CCGA package offerings support core and four additional power zones. - Direct lid attach (DLA) is available for thermal enhancement. - Up to 8 on-package 56 nF decoupling capacitors can be supported. - Number of ceramic layers depends on the die footprint. - Contact your IBM representative for additional and most up-to-date information, including custom offerings.									



Table 17. Area Array C4 Ceramic Die-Package Menu: Double Dense Footprint CBGA and CCGA

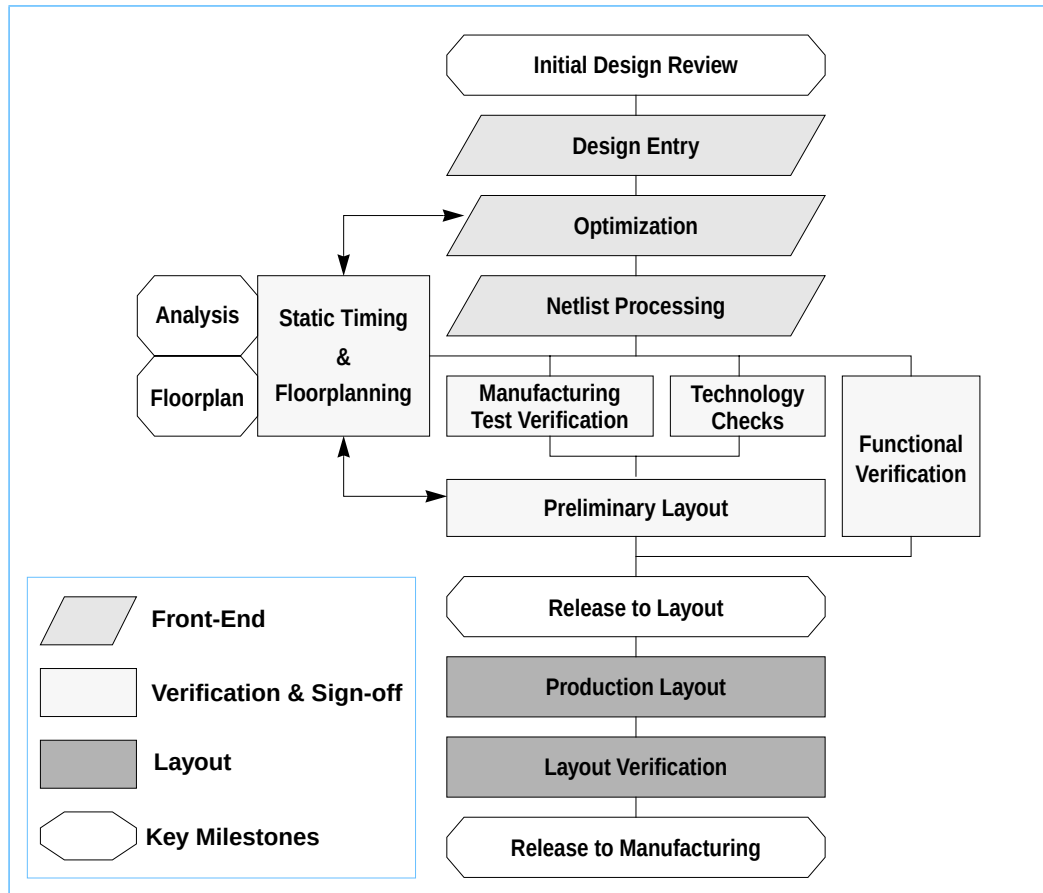
1.27 mm pitch CBGA	Number of Layers	Max Signal I/O for Die-Package Combination											
32.5 x 32.5 mm: 624 total balls	16	288	410	456	456	456	456						
25 x 32.5 mm: 474 total balls	14	288	327	327	327	327	327	327	327				
25 x 25 mm: 360 total balls	12	244	244	244	244	244	244	244					
1.00 mm pitch CBGA	Number of Layers	Max Signal I/O for Die-Package Combination											
32.5 x 32.5 mm: 937 total balls	19			548	644	644	644	644	644				
25 x 32.5 mm: 720 total balls	15	288	410	496	496	496	496	496	496				
25 x 25 mm: 552 total balls	14	288	380	380	380	380	380						
1.27 mm pitch CCGA	Number of Layers	Max Signal I/O for Die-Package Combination											
42.5 x 42.5 mm: 1088 total columns	18			548	702	748	748	748					
32.5 x 42.5 mm: 824 total columns	17			548	564	564	564	564					
32.5 x 32.5 mm: 624 total columns	16	288	410	456	456	456	456						
1.00 mm pitch CCGA	Number of Layers	Max Signal I/O for Die-Package Combination											
42.5 x 42.5 mm: 1657 total columns	19						760	962	1124	1124	1124		
32.5 x 42.5 mm: 1247 total columns	18					748	748	748	748				
32.5 x 32.5 mm: 937 total columns	19			548	644	644	644	644	644				
Die Metal Layers		Wireable Gates ¹ (Millions) for Die-Size Metal Layer Combinations											
6		2.673	3.396	4.212	5.117	6.308	7.686	9.182	10.78	12.33	13.98	15.74	
1. Actual usable gate count varies depending on the design content. 2. CBGA package offerings are JEDEC level 1 or JEDEC level 2 moisture sensitivity. CCGA package offerings are JEDEC level 1 moisture sensitivity. CBGA and CCGA package offerings are reliability grade 3 (grade 1 offerings in limited availability). 3. CBGA and CCGA package offerings support core and four additional power zones. 4. Direct lid attach (DLA) is available for thermal enhancement. 5. Up to 8 on-package 56 nF decoupling capacitors can be supported. 6. Number of ceramic layers depends on the die footprint. 7. Contact your IBM representative for additional and most up-to-date information, including custom offerings.													



IBM ASIC Design Flow

High quality and fast time-to-market can be realized by using IBM's full-scan design-for-test methodology, level-sensitive scan design (LSSD). See "Supported Design-for-Test Techniques" on page 72 or contact your IBM representative for more information.

Figure 1. IBM ASICs Design-for-Test Methodology



Cell Library Guide

Cell Naming Conventions

There are three main parts to the cell name: function, library, and performance level.

Function describes the basic Boolean function for the primitive, complex, unique, latch, and I/O cells. A detailed table of the library functions appears at the end of this section. Details on macro naming conventions (compilable register array, embedded DRAM, compilable memory array, PLL, etc.) can be found in the appropriate macro chapter.

Library refers to either the gate array, standard cell, or data path libraries. If there is an “_G” (underscore G) in the cell name, it is from the gate array library. Cells from the standard cell library do not have “_G” in their names.

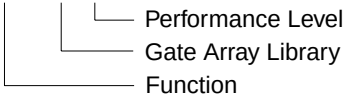
Performance Level is designated A through Y with an underscore separating the performance level from the library type. In this databook, each cell datasheet represents all of the cell performance levels, so the performance level designation is not part of the datasheet cell name.

The full cell name is: **Function_Library_Performance Level**. The examples that follow show some cell names from this databook.

Cell Name: AND3_G_E

Description: 3-Way AND, Gate Array, Performance Level E

AND3_G_E

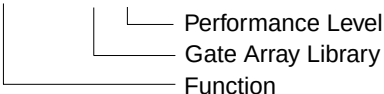


Performance Level
Gate Array Library
Function

Cell Name: LPH0001_G_H

Description: Polarity Hold Latch, LSSD, +L2 Output, Gate Array, Performance Level H

LPH0001_G_H



Performance Level
Gate Array Library
Function

Library Functions

The following tables describe the library functions in more detail.

Table 18. Function Name Descriptions: Primitive, Complex, and Unique Cells

Cell	Description
ADDF	Full adder. Two-bit adder with carry-in and carry-out.
ANDn	Logical AND of n inputs.
AOabcd	Logical OR of 2 to 4 AND groups. Parameters a–d specify the number of inputs in each AND group in descending order.
AOlabcd	Logical NOR of 2 to 4 AND groups. See AOabcd.
BUFFER	Noninverting buffer.
CLK	Noninverting clock buffer.
CLKCHP	Clock chopper with LSSD test features.
CLKG	Large noninverting clock buffer.
CLKGATE	Noninverting clock buffer with gating function.
CLKGI	Large inverting clock buffer.
CLKI	Inverting clock buffer.
CLKSPL	Clock splitter.
CLKSPC	Core clock splitter.
COMPn	n-bit compare.
DECab	a to b decode.
DELAYn	Delay line.
DELAYMUX0	Programmable fine delay element
DELAYMUXN	Programmable delay element
INVERT	Logical invert of the input.
INVERTBAL	Balanced inverter.
MCMUX	2:1 mode control MUX
MUXn1	n to 1 noninverting multiplexer.
MUXn1BAL	Balanced n to 1 noninverting multiplexer.
NANDn	Logical NAND of n inputs.
NANDnBAL	Balanced n-way NAND.

Table 18. Function Name Descriptions: Primitive, Complex, and Unique Cells (Continued)

Cell	Description
NORn	Logical NOR of n inputs.
OAabcd	Logical AND of 2 to 4 OR groups. See AOabcd.
OAlabcd	Logical NAND of 2 to 4 OR groups. See AOabcd.
ORn	Logical OR of n inputs.
TERM	Terminator.
TTMUX	2:1 Termination test MUX.
XNORn	Logical exclusive NOR of n inputs.
XORn	Logical exclusive OR of n inputs.

Table 19. Function Name Descriptions: Latches

Character Position	Description ¹
1st through 3rd characters (if the 8th through 11th characters are “_LPC,” this is a low-power clocking version)	LPHxxxx: LSSD polarity hold, low-power version LMXxxxx: LSSD D latch w/2:1 MUX, low-power version LSC: LSSD scan only L2S: LSSD L2* (star); Port on L1 (master) and L2 (slave) LDE: LSSD D flip-flop mimic, built-in clock splitter LDF: Falling edge-triggered LSSD D flip-flop mimic LDR: Rising edge-triggered LSSD D flip-flop mimic MPHxxxx_LPC: LSSD D MUX latch, low-power version LTLxxxx: Retiming latch
4th character	<u>L1 (master) asynchronous set/reset</u> 0: No L1 set or reset 1: Positive L1 set 2: Negative L1 set 3: Positive L1 reset 4: Negative L1 reset 5: Positive L1 set, positive L1 reset 6: Positive L1 set, negative L1 reset 7: Negative L1 set, positive L1 reset 8: Negative L1 set, negative L1 reset
1. Not all combinations exist in the IBM ASIC SA-27E library.	

Table 19. Function Name Descriptions: Latches (Continued)

Character Position	Description ¹
5th character	L1 (master) outputs available 0: No L1 output 1: Plus L1 output 2: Minus L1 output 3: Plus and minus L1 outputs
6th character	L2 (slave) asynchronous set/reset 0: No L2 set or reset 1: Positive L2 set 2: Negative L2 set 3: Positive L2 reset 4: Negative L2 reset 5: Positive L2 set, positive L2 reset 6: Positive L2 set, negative L2 reset 7: Negative L2 set, positive L2 reset 8: Negative L2 set, negative L2 reset
7th character	L2 (slave) outputs available 0: No L2 output 1: Plus L2 output 2: Minus L2 output 3: Plus and minus L2 outputs
1. Not all combinations exist in the IBM ASIC SA-27E library.	

Table 20. Function Name Descriptions: I/Os

Character Position	Description
1st character	Generic I/O type B: Bidirectional I/O O: Output I: Receiver
2nd through 4th characters	Interface levels C18: 1.8V CMOS. Switches from 0 to 1.8V and has ESD diodes to ground and V_{dd} . C25: 2.5V CMOS. Switches from 0 to 2.5V and has ESD diodes to ground and V_{dd250} . P25: 2.5V CMOS, 3.3V protected. Switches from 0 to 2.5V and has ESD diode to ground and stacked diodes to V_{dd} . T33: 3.3V LVTTL. Switches from 0 to 3.3V and has ESD diodes to ground and V_{dd330} . Exception: Some I/O cells have the family name in character positions two through seven, such as cell BHSTL18C1 for the High Speed Transceiver Logic Class 1 family.
5th and 6th characters (5th through 7th characters for IC18DLTPUT)	Driver output (first character a "B") The impedance value listed for each I/O is the approximate impedance of an I/O at nominal process, 50°C and nominal supply. This information is provided for designers interested in driving a known transmission line impedance: 20: 20 ohm output 35: 35 ohm output 50: 50 ohm output 65: 65 ohm output 90: 90 ohm output, etc. Receiver output (first character an "I") D1: DI1 receiver D2: DI2 receiver DLT: Embedded DRAM leakage test LT: Leakage test RE: Reference enable RI: RI receiver TE: Test enable

Table 20. Function Name Descriptions: I/Os (Continued)

Character Position	Description
7th and 8th characters (8th and 9th characters for IC18DLTPUT)	Identifies attached pull-up or pull-down resistors (if applicable) PU: Pull-up PD: Pull-down
"_PM" suffix	Identifies driver, receiver, or bi-di as "perimeter." Driver, receiver, or bi-di without the suffix is area array.
"T" suffix	Identifies driver, receiver, or bi-di as "test" function. This is for test I/Os only. Test I/Os are the 64 I/Os that are contacted during reduced pin count testing. Boundary-scan is not required.

Optional Outputs

Some multiple output cells have optional output pins. Table 21 and Table 22 list these cells and their optional pin groups. Each group lists the affected pins and the minimum and maximum number of pins that can be used.

For example, an instantiation of a full adder can use SUM, or COUT, or both SUM and COUT.

Table 21. SA-27E Library Cells with "Optional" Outputs

Function	Cell Name	Outputs	(Pin Group): (Minimum # pins, Maximum # pins)
Full Adder	ADDF	SUM, COUT	(SUM, COUT): (1,2)
Clock Splitter	CLKSPC, CLKSPL	ZB, ZC	(ZB, ZC): (1,2)
L2* Latch	L2S0101	L1, L2	(L1): (0,1)

Table 22. SA-27E I/O Cells with "Optional" Outputs

Function	Cell Name	Outputs	(Pin Group): (Minimum # pins, Maximum # pins)
Nontest CIO	BCxxxx, BPxxxx, BTxxxx, BCxxxxPD, BTxxxxPD, BCxxxxPU, BTxxxxPU	PAD, Z, ZH, ZDI, ZRI	(Z, ZH): (1,2) (PAD, ZDI, ZRI): (3,3)
Test CIO	BCxxxxT, BPxxxxT, BTxxxxT, BCxxxxPDT, BTxxxxPDT, BCxxxxPUT, BTxxxxPUT	PAD, Z, ZH, ZDI	(Z, ZH): (0,2) (PAD, ZDI): (2,2)

Unused Inputs

Input pins that are not used should be connected to their noncontrolling state. The customer should connect any unused input to either net "ONE," "VDD," "ZERO," or "GND." Any inputs connected to these nets will be tied to the V_{dd} or ground rail, respectively, during chip wiring.

How to Use Logic Symbols

The logic symbols shown in this databook are representative of the symbols available in the SA-27E ASIC design kit. The design kit symbols contain the cell name, as well as the inputs and outputs that are shown in this databook. The I/O chapters show logic schematics instead of symbols to better represent the internal logic of the I/Os.

How to Use Truth Tables

The truth table shown in Table 23 is an example of a typical cell. The legend shown in Table 24 lists the symbols used to define several possible logic states in the cell function.

Table 23. Truth Table Example

Inputs				Output
A1	A2	B1	B2	Z
0	X	0	X	0
0	X	X	0	0
X	0	0	X	0
X	0	X	0	0
1	1	X	X	1
X	X	1	1	1

Table 24. Truth Table Legend

Logic Symbol	Meaning
0	Forcing logic 0
1	Forcing logic 1
X	Forcing logic 0 or logic 1 (don't care of "0" or "1")
Hi-Z	High impedance
H	Weak logic 1 (high impedance terminated to 1)
L	Weak logic 0 (high impedance terminated to 0)
-	Don't care of any state (1, 0, H, L, etc.)
NC	No change
TG	Toggle
R	Rise
F	Fall

Performance Levels

Most cells offer multiple performance levels. The performance levels are identified by A through Y. Each performance level can occupy a different number of cell units. An "A" performance level is used to drive the smallest loads efficiently; a "Y" performance level is used for driving the highest loads efficiently. Performance level can also be used to denote non-overlap, and not drive strength of clock splitters or delay elements. Delay tables and input pin capacitances are provided for each performance level of a given cell. Table 25 can be used as an estimate for maximum capacitive load for each performance level. This table is based on internal library elements, excluding the CLKGATE, CLKG, and CLKGI cells.

Table 25. Maximum Load Capacitances by Performance Level

Maximum Load Capacitance (fF)	Performance Level														
	A	B	C	D	E	F	H	I	J	K	L	M	N	O	P
Standard cell library	50	65	125	185	250	405	525	735	1025	1350	1520	2200	2500	3000	-
Gate array library	-	-	-	-	350	-	690	-	1380	-	2075	-	2770	-	3450

Propagation Delay

The propagation delay information provided for each cell in this databook is for **estimation** purposes only. The delays shown are calculated for different process, temperature, and voltage conditions.

Propagation delays are presented for each cell as a function of the number of standard loads (N_{std} or D_{std}). The propagation delay equation is a linear equation derived using input transition times listed in Table 26. For internal cells and receivers, one standard load is approximately equivalent to the average input capacitance of the “A” pin of a gate array NAND2, performance level E. This average input capacitance between best case and worst case is 0.006 pF; for off-chip drivers, one standard load is called D_{std} and is equivalent to 1.000 pF. After computing the total output capacitance in terms of standard loads, the delays can be calculated.

Table 26. Input Transition Times and Standard Load Equivalences

Cell Types	Slow	Nominal	Fast	Equivalences	
				N_{std}	D_{std}
Primitive, complex, and unique cells (except CLKG, CLKGATE, and CLKGI)	0.20 ns	0.20 ns	0.20 ns	0.006 pF	n/a
Latches	0.20 ns	0.20 ns	0.20 ns	0.006 pF	n/a
CLKG, CLKGATE, CLKGI, and pad drivers	0.20 ns	0.20 ns	0.20 ns	n/a	1.000 pF
Receivers	1.00 ns	1.00 ns	1.00 ns	0.006 pF	n/a

How to Use Propagation Delay Tables

The delay table is used to estimate delays for a given path in different environmental conditions. The terms below are used in the delay tables.

<i>Path</i>	=	<i>Input pin to output pin logic path</i>
<i>Performance level</i>	=	<i>A, B, C, D, E, F, etc.</i>
<i>Parameter</i> t_{PLH}	=	<i>Propagation delay, low-to-high (output)</i>
t_{PHL}	=	<i>Propagation delay, high-to-low (output)</i>
<i>Equation</i>	=	<i>Method of solving for table values. See "Propagation Delay Equation" on page 63.</i>

Table 27. Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.080 + 0.011N _{std}	0.066 + 0.008N _{std}	0.053 + 0.006N _{std}
		t _{PHL}	0.078 + 0.013N _{std}	0.054 + 0.008N _{std}	0.039 + 0.006N _{std}
B-Z		t _{PLH}	0.090 + 0.011N _{std}	0.074 + 0.008N _{std}	0.060 + 0.006N _{std}
		t _{PHL}	0.074 + 0.013N _{std}	0.049 + 0.008N _{std}	0.034 + 0.006N _{std}
A-Z	H	t _{PLH}	0.074 + 0.006N _{std}	0.063 + 0.004N _{std}	0.052 + 0.003N _{std}
		t _{PHL}	0.073 + 0.007N _{std}	0.051 + 0.004N _{std}	0.038 + 0.003N _{std}
B-Z		t _{PLH}	0.084 + 0.006N _{std}	0.071 + 0.004N _{std}	0.058 + 0.003N _{std}
		t _{PHL}	0.068 + 0.007N _{std}	0.046 + 0.004N _{std}	0.033 + 0.003N _{std}
A-Z	J	t _{PLH}	0.074 + 0.003N _{std}	0.062 + 0.002N _{std}	0.051 + 0.001N _{std}
		t _{PHL}	0.073 + 0.003N _{std}	0.051 + 0.002N _{std}	0.038 + 0.002N _{std}
B-Z		t _{PLH}	0.084 + 0.003N _{std}	0.070 + 0.002N _{std}	0.058 + 0.001N _{std}
		t _{PHL}	0.068 + 0.003N _{std}	0.045 + 0.002N _{std}	0.032 + 0.002N _{std}
A-Z	L	t _{PLH}	0.074 + 0.002N _{std}	0.061 + 0.001N _{std}	0.051 + 0.001N _{std}
		t _{PHL}	0.072 + 0.002N _{std}	0.050 + 0.001N _{std}	0.037 + 0.001N _{std}
B-Z		t _{PLH}	0.084 + 0.002N _{std}	0.069 + 0.001N _{std}	0.058 + 0.001N _{std}
		t _{PHL}	0.068 + 0.002N _{std}	0.045 + 0.001N _{std}	0.032 + 0.001N _{std}

Propagation Delay Equation

The propagation delay equation is shown for three different process conditions: slow, medium, and fast. The simplified timing model is described by the basic equation:

$$\text{Delay } (t_{PLH} \text{ or } t_{PHL}) = \text{intercept} + (\text{slope} \times N_{std})$$

or for pad drivers only:

$$\text{Delay } (t_{PLH} \text{ or } t_{PHL}) = \text{intercept} + (\text{slope} \times D_{std})$$

where:

intercept = Intrinsic delay (ns)

slope = Delay rate per standard load (ns/ N_{std})

N_{std} = Number of standard loads. See "Wire Routing and Fanout" on page 65.

D_{std} = Number of standard loads for drivers. See "Wire Routing and Fanout" on page 65.

Scaling Delay for Temperature and Voltage

To scale the propagation delay for different temperatures and voltages, use the following rough **approximation**:

$$\text{Delay} = [\text{Intercept} + (\text{slope} \times N_{std})] \times [1 + T_{mult} \times (T - T_{base})] \times [1 + V_{mult} \times (V_{base} - V)]$$

where:

$$T_{mult} = 0.002 / ^\circ\text{C}$$

T = Temperature of interest, in $^\circ\text{C}$

T_{base} = T_j shown in propagation delay table

T_{base} (slow process) = 125°C

T_{base} (nominal process) = 25°C

T_{base} (fast process) = 0°C

$$V_{mult} = 0.6/V$$

V = Voltage of interest, in volts

V_{base} = V_{dd} shown in propagation delay table:

V_{base} (slow process) = 1.65V

V_{base} (nominal process) = 1.8V

V_{base} (fast process) = 1.95V

Example: Calculating a Propagation Delay

Refer to Table 27, "Propagation Delays," on page 62. For a fast process and path A–Z of performance level E, with $N_{std} = 2.0$ standard loads, voltage = 1.9V, and temperature = 85°C, the propagation delay is calculated as follows:

$$\begin{aligned}
 t_{PLH} &= [0.053 + (0.006)(2.0)]ns \times [1 + (0.002^\circ C \times (85^\circ C - 0^\circ C))] \times [1 + (0.6/V \times (1.95V - 1.9V))] \\
 &= 0.065 ns \times 1.17 \times 1.03 \\
 &= 0.0783 ns \\
 t_{PHL} &= [0.039 + (0.006)(2.0)]ns \times [1 + (0.002^\circ C \times (85^\circ C - 0^\circ C))] \times [1 + (0.6/V \times (1.95V - 1.9V))] \\
 &= 0.051 ns \times 1.17 \times 1.03 \\
 &= 0.0615 ns
 \end{aligned}$$

Setup and Hold Delays

Table 28 shows a sample of latch setup and hold delays using the standard cell latch LPH0001_LPC. Setup and hold times are calculated using worst case conditions, with the clock and data slew rate at 0.2 ns.

Table 28. Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.214454	0.215784	0.215233
Hold	-0.103317	-0.105301	-0.102132

¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

Wire Routing and Fanout

The input capacitance for each cell pin is unique and is shown in terms of the number of standard loads (N_{std}) for each input pin. The total load capacitance (C_L) that an output must drive is the sum of the input capacitances on the output net and the capacitance of the metal interconnect (C_{wire}). C_L can be calculated by the following equation:

$$C_{gate} = \sum \text{input pin capacitances}$$

$$C_{wire} = \text{See Table 29.}$$

$$C_L = C_{gate} + C_{wire}$$

Table 29. Estimated Values for Package C_{wire} (Avg. fanout = 2.58; in units of N_{std})

Levels of Metal ¹	Package Footprint ²	10,000 Cells	100,000 Cells	500,000 Cells	1,000,000 Cells
6lm	c4a	2.7	4.3	6.0	7.3
6mz		2.7	4.3	6.0	7.3
5mz	c4p	2.7	4.3	6.0	7.7
6mz		2.7	4.3	6.0	7.3
4mz	wb	2.7	4.3	6.0	8.2
5mz		2.7	4.3	6.0	7.3
6mz		2.7	4.3	6.0	7.3

1. Last metal level.
2. c4a = area array C4 package. c4p = peripheral C4 package. wb = wire bond package.

The capacitance of a length of wire in standard loads is shown in Table 30.

Table 30. Estimated Capacitance for Metal Wiring (units N_{std}/mm)

Levels of Metal	M1	M2	M3	M4	M5	mz ¹ , lm ¹
5mz	47.6	42.6	42.6	42.6		45.8
6mz	44.8	42.6	42.6	42.6	42.6	45.8
6lm	47.6	42.6	42.6	42.6	38.6	40.2

1. Last metal level

How to Use Capacitance Tables

The input and internal capacitance values represent an average between best case and worst case **estimated** capacitance when using the input rise times listed in Table 26, "Input Transition Times and Standard Load Equivalences," on page 61. For this instance, the internal capacitance is reported at a transition time of 0.2 ns. Capacitance tables contain the following fields:

- Input pins* = Estimated average input pin capacitance (in units of N_{std}).
- A, B, C, D, E, etc.* = Performance level.
- Internal* = Estimated average internal capacitance of the device (in units of N_{std}). Used for power calculations.
- Cell units* = Area of cell, in number of cell units. A cell unit is 1 x 12 wiring channels for non-I/O cells; 120 x 576 for area array I/O cells or 96 x 576 for perimeter I/O cells. Each wiring channel is 0.56 μm wide.

Table 31. Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level			
	E	H	J	L
A	0.973	1.933	4.040	5.833
B	0.991	2.051	3.987	6.019
Internal	2.659	4.828	9.637	14.447
Cell Units	6 cells	9 cells	15 cells	21 cells

Table 31 is a sample of a NAND2_G. The average capacitance of input pins A and B at performance level E is approximately 1.0 standard load, which is equivalent to 0.006 pF.

Example: Calculating Propagation Delay and C_L

Refer to Table 27, Table 29, and Table 31.

From Table 29, C_{wire} for a logic chip (C4 package) with 500,000 cells and 6 levels of metal is estimated to be 6.0 standard loads.

For pin A of the cell represented in Table 31, C_{gate} is:

$$\begin{aligned} C_{gate} &= (\text{Input pin capacitance}) \\ &= 0.973 \text{ standard loads} \end{aligned}$$

The total load capacitance for this cell is:

$$\begin{aligned} C_L &= C_{gate} + C_{wire} \\ &= 0.973 + 6.0 \text{ standard loads} \\ &= 6.973 \text{ standard loads} \\ C_L &= 6.973 N_{std} \end{aligned}$$

Using Table 27, the propagation delay for path A–Z, fast process, temperature = 0°C is:

$$\begin{aligned} t_{PLH} &= \text{intercept} + (\text{slope} \times N_{std}) \\ &= [0.053 + (0.006)(6.973)]ns \\ &= 0.095 \text{ ns} \\ t_{PHL} &= \text{intercept} + (\text{slope} \times N_{std}) \\ &= [0.039 + (0.006)(6.973)]ns \\ &= 0.081 \text{ ns} \end{aligned}$$

Power Consumption

The power consumption of a CMOS design depends on the operating frequency, the load capacitances, and the activity factor of each design. The following equations provide an **estimation** of the power consumption of a design based on generalized or rule-of-thumb design parameters. More detailed calculations can be done using guidelines from an application note on power estimation available from your IBM representative.

Logic:

$$\begin{aligned} \text{Number of unit cells used} &= N_{logic} \\ \text{(this is the area of all standard-cell and gate-array elements)} & \\ \text{Total logic capacitance} &= C_{logic} \text{ (pF)} \\ \text{Operating frequency of logic} &= F_{logic} \text{ (MHz)} \\ \text{Activity factor of logic} &= A_{int} \text{ (0 to 1.0; 0.15 is typical)} \\ \text{Power for logic, } P_{logic} &= C_{logic} \times F_{logic} \times A_{int} \times V_{dd}^2 \text{ (}\mu\text{W)} \end{aligned}$$

The equation used to calculate chip power is given by:

$$P_{total} = P_{logic} + P_{IO} + P_{Arrays} \text{ (watts)}$$

C_{logic} can be approximated based on the number of gate array cells used:

$$C_{logic} = 0.011 \times N_{logic} \text{ (pF)}$$

The following equation gives a more accurate result if the individual components can be accurately defined:

$$C_{logic} = C_{input} + C_{internal} + C_{wire} \text{ (pF)}$$

where:

$$\begin{aligned} C_{input} &= \sum c_{in} \text{ (input pin capacitance)} \\ C_{internal} &= \sum c_{internal} \text{ (internal capacitance)} \\ C_{wire} &= \sum c_{wire} \text{ (wiring capacitance)} \end{aligned}$$

If different sections of the logic operate at different frequencies, the individual sections can be calculated separately and then added together.

The activity factor (A) depends on the type of net considered. For example, a clock net that switches up and down every cycle has an activity factor of 1.0. However, a latch output having only one transition per cycle has an activity factor of 0.5. The activity factor for most logic nets is much less than 0.5.

I/O:

Number of drivers	=	N_{IO}
Average load per driver	=	C_L (pF)
Operating frequency of drivers	=	F_{io} (MHz)
Activity factor of drivers	=	A_{io} (0 to 1.0)
Power for I/Os, P_{IO}	=	$(C_L + 10 \text{ pF}) \times N_{IO} \times F_{io} \times A_{io} \times V_{dd}^2$ (microwatts) (the 10 pF adder includes parasitic capacitance of die and package)

Others:

For information on estimating power consumption for compilable memory arrays, compilable register arrays, and other macros, see your IBM representative.

Example:

Logic: 595,000 logic cells operate at 100 MHz; activity factor is 0.10.

I/O: 200 I/O switching 50 pF at 75 MHz; activity factor is 0.2. $V_{dd} = 1.8V$.

$$\begin{aligned} P_{logic} &= (0.011 \text{ pF/cell} \times 595,000 \text{ cells}) \times 100 \text{ MHz} \times 0.10 \times (1.8V)^2 \\ &= 0.212 \text{ watts} \end{aligned}$$

$$\begin{aligned} P_{IO} &= (50 + 10) \text{ pF/(I/O)} \times 200 \text{ I/O} \times 75 \text{ MHz} \times 0.20 \times (1.8V)^2 \\ &= 0.583 \text{ watts} \end{aligned}$$

$$\begin{aligned} P_{total} &= 0.212 \text{ watts} + 0.583 \text{ watts} \\ &= 0.795 \text{ watts} \end{aligned}$$



Reliability

The SA-27E design system offers two reliability levels: grade 1 and grade 3, with grade 1 having the lowest failure rate. The different grades of reliability are achieved through the use of process screens and burn-in. Higher reliability drives increased manufacturing cost; therefore, reliability testing and burn-in are exercised only to meet specific customer requirements. SA-27E is supported for up to 100 kPOH. Applications requiring a longer lifetime should be reviewed with IBM ASICs product development on a case by case basis.

Reliability Objectives

The reliability objectives for the SA-27E design system product are competitive with similar products in the semiconductor industry. Contact your IBM representative for more information on product reliability under specific operating conditions not covered by Table 32. The two reliability grades are intended to provide our customers with the choice of reliability required for their application.

Exposure to the extreme limits of the junction temperature for extended periods of time can affect device reliability. Exceeding the minimum/maximum temperature limits could cause permanent damage. Operating the product at the extreme temperature limits for extended periods of time can degrade product reliability.

Note: *The reliability requirements for parts with embedded DRAM are being established and will be implemented to meet given applications and customers' reliability objectives.*

Table 32. SA-27E Reliability Offering

Reliability Grade ¹	EFR ² (FITs) ³	AFR (FITs) ⁴
1	25	10
3	250	100

1. Assumptions: 100 kPOH, 3000 on/off cycles, and a chip temperature of 60°C. This table does not include the card-attach failure rate.

2. EFR. Early failure rate (0.0 hours to one year of use) in FITs.

3. FIT. Failures in time: equivalent to ppm/kPOH. Values in this table are referenced to 60°C, and nominal use voltage.

4. AFR. Average failure rate (0.0 hours to 40 kPOH) in FITs.



Standardized Burn-In Equipment

To avoid the cost and delay of building custom burn-in boards, placement of critical signals must utilize predefined subsets of pins. For example, all burn-in signals must be placed within a set of 64 specific package pins identified on each package size. If a particular design is unable to meet the constraints for using standard burn-in boards, the reliability will be supported with custom boards at a higher cost and possibly delayed product shipment.

Test Methodology

The SA-27E ASIC product offers a flexible, cost-effective set of test solutions to meet a variety of customer requirements. Cost trade-offs can be demonstrated depending on the test options chosen.

Supported Design-for-Test Techniques

Level-Sensitive Scan Design (LSSD)

The addition of scan circuitry converts the test problem from a sequential one to a combinatorial one. IBM's full-scan design-for-test methodology, LSSD, is an IBM-developed double-latch methodology which requires that all latches within the design be accessible via scan. A key advantage of LSSD over generic scan is that the double-latch design enables transition-fault testing (also known as path delay testing) from latch to latch by allowing a double-latch to both time-launch and time-observe with independent clocks. LSSD enables automatic test pattern generation (ATPG) for both stuck-faults and transition-faults. Finally, it provides observability and conditioning capability for easy and rapid debug of systems and their components.

Boundary-Scan

Boundary-scan at the chip level can be utilized both to reduce tester I/O requirements and to perform interconnect testing at the board level. Boundary-scan allows testing of the interconnections of higher level assemblies with or without testing device internals. Boundary-scan is supported by both an LSSD and JTAG definition.

Array Built-in Self-Test (MABIST)

Embedded (memory) MABIST permits elimination of either I/O isolation requirements or extensive scan patterns for the testing of embedded memories. Microprogrammable MABIST engines allow variability in the patterns for unforeseen sensitivities. Memory access and cycle times can also be tested at speed. All SA-27E embedded compilable memory arrays include MABIST in their designs.

Test Methodology Descriptions

Structural Testing

The key benefits of structural test techniques are automatic test pattern generation, automatic diagnostic capability, higher achievable test coverage (for example, 99.9+-% stuck-fault and 95% transition-fault coverage), and faster turnaround time for ATPG and debug. The use of structural testing for large designs requires LSSD scan.

Deterministic Stuck-Fault (DSF) Test

DSF stored pattern tests use automatic generation of vector patterns to stimulate various stuck-at faults in the logic model for the chip. The chip logic model is generated from the individual logic models for each cell function in the ASIC library. This technique results in the least number of test vectors for the chip when compared to other structural test techniques. These patterns are used at wafer-level test and as a supplement to weighted random pattern test at package level.

Weighted Random Pattern (WRP) Test

WRP testing can significantly reduce test data volume compared to DSF test. Stuck-fault WRP uses the same fault model as the DSF test but takes the approach of generating “pseudo-random” and “weighted-random” patterns and marking off the faults excited by the pattern set. Only the weight sets, signatures, and seeds are stored.

LSSD Delay Test

LSSD delay test utilizes a double-latch design to both launch and capture transitions. The patterns and timings are created from a transition-fault model for the chip generated from the model libraries and physical layouts. For stored-vector delay test, the pattern volume typically increases 2x to 4x over stored-vector DSF test, while WRP delay test utilizes the same pattern set as stuck-fault WRP, with the addition of timings.

Reduced Pin Count Testing (RPCT)

RPCT is an extension of boundary-scan to allow the testing of very high pin count chips on low pin count testers. The device is internally tested through the “test” bus (for example, clocks, boundary-scan control lines) without contacting the other pins of the device.

RPCT limits the I/O requirement and cost for any number of device I/Os with the exception of parametrics. However, parametric testing for higher I/Os can be addressed by test equipment with many parametric channels or parametric multiplexing capability. Patterns are applied through the test bus, which condition the “external” pins for the parametric force and measurement.

Quiescent Power Supply Current (I_{ddq}) Test

I_{ddq} testing has been shown to improve product quality. A flexible implementation of I_{ddq} testing includes application of test vectors from a number of sources, the optimization of test vectors to achieve high coverage with few vectors, and the statistical monitoring of current measurements. I_{ddq} testing has been found to detect some delay faults and some faults that will later cause reliability failures; however, I_{ddq} testing does not cover all other fault types and, therefore, is viewed as a supplement rather than a replacement for other methodologies.

Minimum Design Requirements

The SA-27E test methodology requires adherence to the following minimum design requirements:

- LSSD design practices
- Boundary-scan
- Number of test I/Os (for example, clocks, boundary-scan control lines) not to exceed 64
- Bidirectional nontest I/Os to support I/O test

Scan chain length management is also important. Scan chain length directly impacts the test data volume and number of tester cycles needed to test the part. It is recommended that scan chain lengths be minimized and all scan chains be balanced.

LSSD Latches

Overview

This section summarizes LSSD latch cells, which are part of IBM's full-scan design-for-test methodology. For more detailed information, contact your IBM representative.

Definition

The L1 portion of the LSSD latches in this databook is the "master." The L2 portion of these latches is the "slave."

Table 33. Latch Type Descriptions

Latch Type		Description
LSSD latches	D latch	This is a standard L1/L2 LSSD latch that is fully testable through scan rings using A and B clocks. This latch is also known as "master-slave" and is level-sensitive.
	Scan-only	This is used only in the scan ring and only has a scan input.
	L2* latch	This is an L1/L2 LSSD latch that can accept data into L1 and L2 independently with two separate C clocks. However, in the scan mode, it is a normal L1/L2 LSSD latch (that is, A and B clocks are used to scan the data in and out). The L1 and L2 part of this latch can be used separately in any logic path.
Edge-triggered flip-flops	D-FF mimic	This is an edge-triggered flip-flop that contains a clock splitter. The E input (clock oscillator) is the input to the built-in clock splitter that generates internal clocks to L1 and L2. The B and C inputs must be held high during normal system operation. In scan mode, B and C inputs are controlled by the tester.

Table 34. Pin Naming Conventions for Latches

Pin		Description
Clock pins	A	A clock: scan clock to master
	B	B clock: shift clock to slave
	C	C clock for L1 (master)
	C1, C2	C clocks for L2S0101 latches
	E	Oscillator clock (D-FF mimic)
	EN	Clock enable

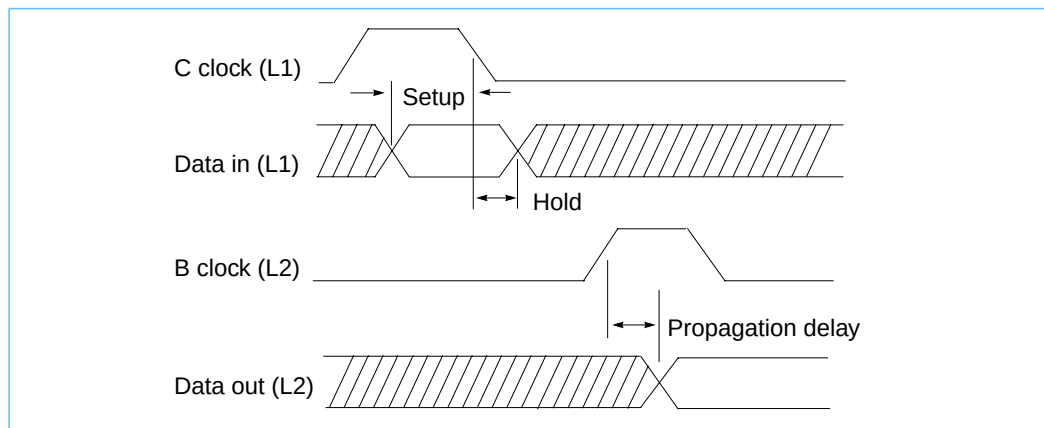
Table 34. Pin Naming Conventions for Latches (Continued)

Pin		Description
Data input pins	D	Data for L1 (master)
	D1, D2	Data for L2S0101 latches
Scan input pin	I	Scan-in
Set/reset pins	S1	Direct set for L1 (positive active)
	R1N	Direct reset for L1 (negative active)
	RXN	Direct reset for D-FF mimic (negative active)
	SXN	Direct set for D-FF mimic (negative active)
Data output pins	L1	+L1 output (in phase with respect to data input)
	L2	+L2 output (in phase with respect to data input)
	L2N	-L2 output (out of phase with respect to data input)

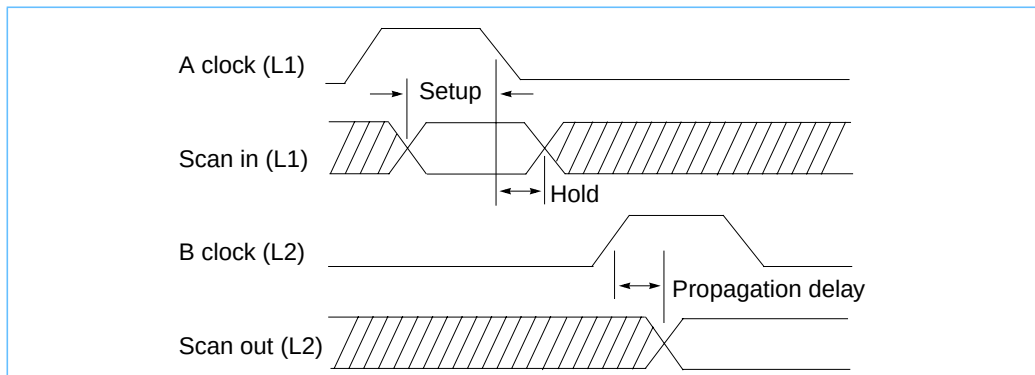
Latch Timing Diagrams

The following timing diagrams describe the critical timing components of LSSD latches (the L1/L2 pair):

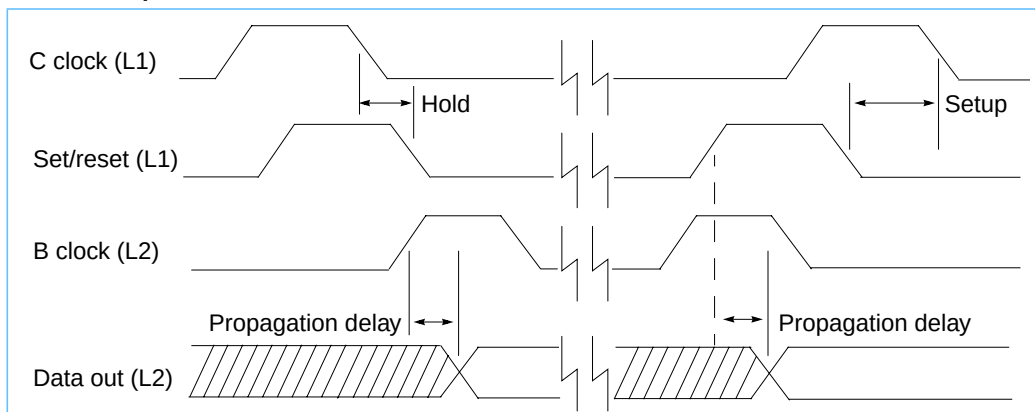
System Operation



Scan Operation



Set/Reset Operation



Direct Set and Reset

These two signals will set or reset L1, regardless of the state of the A and C clocks. The direct set or reset can be applied at any time during the cycle, and the set/reset condition will remain latched in L1 after the set/reset input is de-asserted, as long as the A and C clocks are both inactive (low). The set/reset state will not propagate to the L2 output unless the B clock is high.

Note: For *asynchronous* set/reset flip-flops, refer to D_F_LPH2021, D_F_LPH4041, and D_F_LPH8081.

Data Path and Bit Stacking

Overview

With each design kit, IBM provides a data path synthesis library that contains an extensive set of parameterizable logic functions. These functions (shifters, multiplexers, registers, comparators, adders, multipliers, and other arithmetic functions) can be included in a design by instantiation during synthesis. The use of these data path functions often results in higher performance and/or more efficient silicon utilization than can be obtained with conventional synthesis techniques. The functions are built from the technology library standard cells and can be placed and routed along with the rest of the gate-level design. These functions are also designed with data and control flows that better enable the creation of a structured placement (or “bit stack”).

Bit stacking is a placement technique that takes advantage of the regularity of structure in the logic design. In its simplest form, it involves repeated use of logical functions across bits of a bus: for example, n (number) of 2-to-1 multiplexer cells placed vertically in a column next to n registers of bus A and n registers of bus B, with data flowing horizontally and control flowing vertically. In more complex forms, cells are organized to optimize placement for flow between buses and subsets of buses. The output of the bit stacking process is a group of placed cells, fixed in location relative to an origin. These blocks can then be incorporated into the chip physical design.

Bit stacking work can be done by customers or by an IBM ASIC Design Center, and the path should be defined early in the design process. This type of placement can be ideal for highly-regular or often-repeated logic functions, but it should be justified by the floor-plan and wiring needs of the design because of the potential requirement for additional resources to complete the work.

For more information on the data path library and bit stacking, refer to the HTML documentation included with each design kit in the “synthesis/synopsys_dw/src” directory.

Pseudocells

Overview

Pseudocells are used in the process of mapping flip-flop and latch cells to IBM LSSD-compatible structures, using IBM BooleDozer-Lite design-for-test synthesis (DFTS). Because synthesis tools (other than IBM's BooleDozer™) expect to see latches and D flip-flops, the LSSD polarity-hold latches provided in the IBM ASIC libraries cannot be directly inferred. The solution for these libraries has been to create a family of functions, called "pseudocells." Pseudocells are not actually buildable, but allow synthesis tools to infer a netlist which can then be mapped into LSSD functions.

Pseudocell Types

Pseudocell names contain the name of the targeted LSSD latch, prefixed by characters denoting the pseudocell type. The following diagrams provide logic information for each pseudocell type.

"D_" Cells

These cells support the map of standard D flip-flops to IBM LSSD D-FF mimics. They may be mapped to their LSSD counterparts using IBM BooleDozer-Lite DFTS, or as a service provided by an IBM Design Center. Refer to Figure 2 through Figure 4.

Figure 2. Mapping "D_" Cell to LDExxxx Series Cell

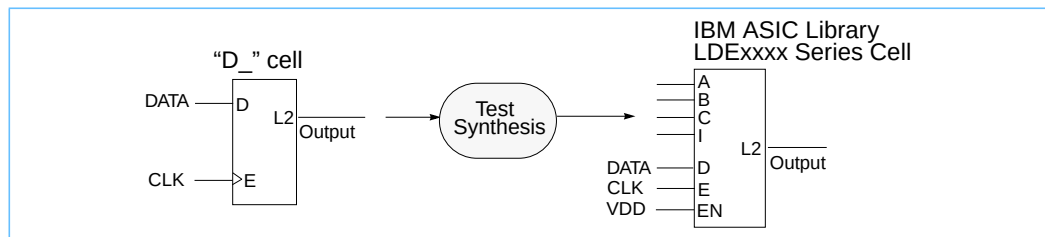


Figure 3. Mapping “D_” Cell to LDFxxxx Series Cell

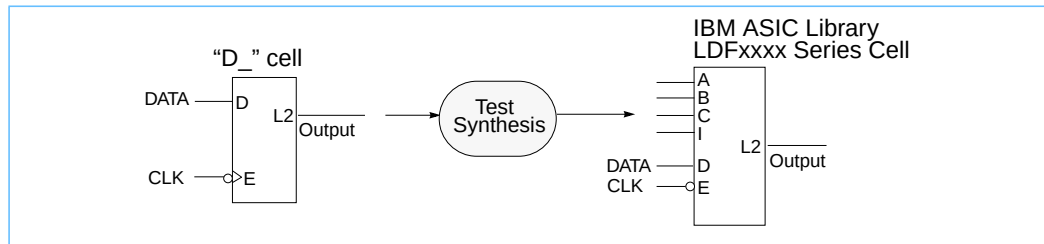
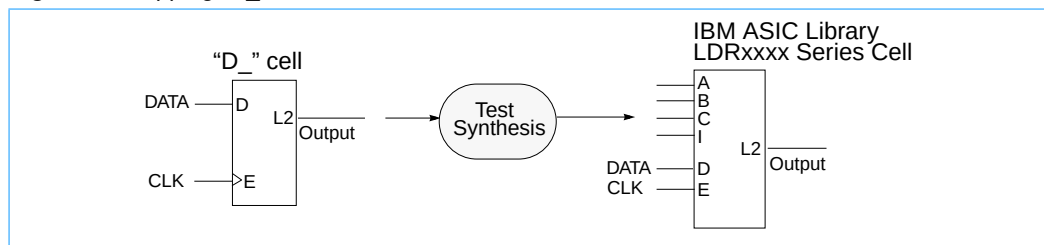


Figure 4. Mapping “D_” Cell to LDRxxxx Series Cell



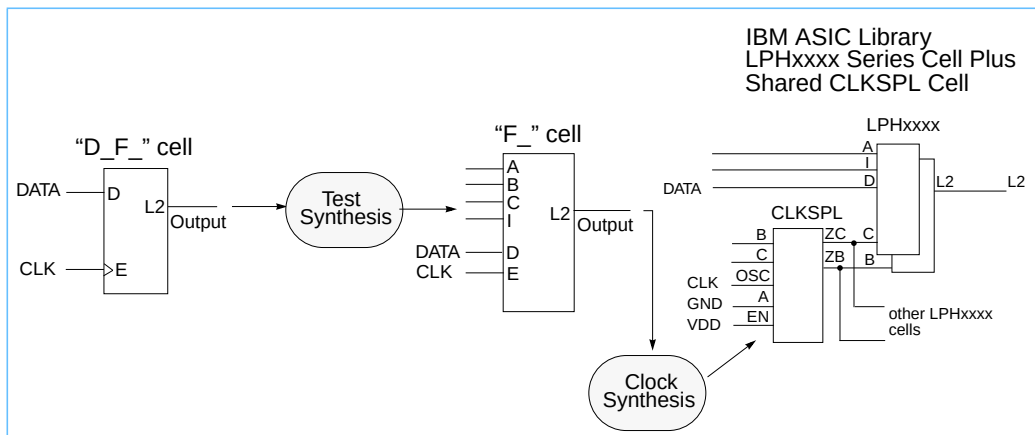
“D_F_” Cells

These cells support the map of standard D flip-flops to IBM LSSD latches. “D_F_” cells are similar to the “D_” cells, but ultimately map to LSSD latches and shared clock splitters. Refer to Figure 5 on page 81.

“F_” Cells

These cells support the map from scannable D flip-flops to IBM LSSD latches. An “F_” cell functions like a D-FF mimic cell, but maps into an LSSD latch and a shared clock splitter. This approach generally results in designs which consume less area than those starting with “D_” cells. Refer to Figure 5 on page 81. Either clock splitter, CLKSP1 (shown) or CLKSPC, may be used. When CLKSPC is used, its input pin PG1 is connected to V_{dd} .

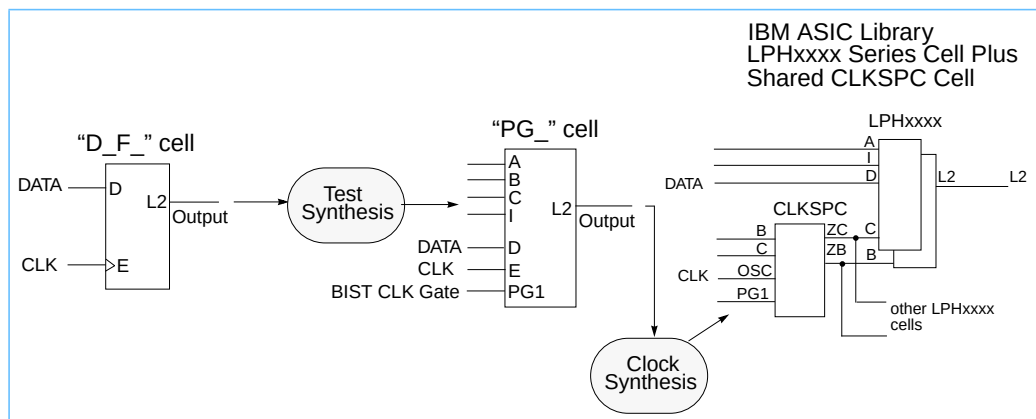
Figure 5. Mapping “D_F_” Cell to “F_” Cell to LPHxxxx Series Cell with Shared Clock Splitter Cell



“PG_” Cells

These cells support the map from scannable D flip-flops to IBM LSSD latches when logic built-in self test (LBIST) is inserted. A “PG_” cell functions like a D-FF mimic cell, but maps into an LSSD latch and a shared clock splitter (CLKSPC), which has a BIST clock gate pin, PG1. This approach generally results in designs which consume less area than those starting with “D_” cells. These cells may be mapped into their LSSD counterparts using the IBM ASIC Design Kit or as a service provided by the IBM Design Service group. Refer to Figure 6 on page 82.

Figure 6. Mapping “D_F_” Cell to “PG_” Cell to LPHxxxx Series Cell with Shared Clock Splitter Cell

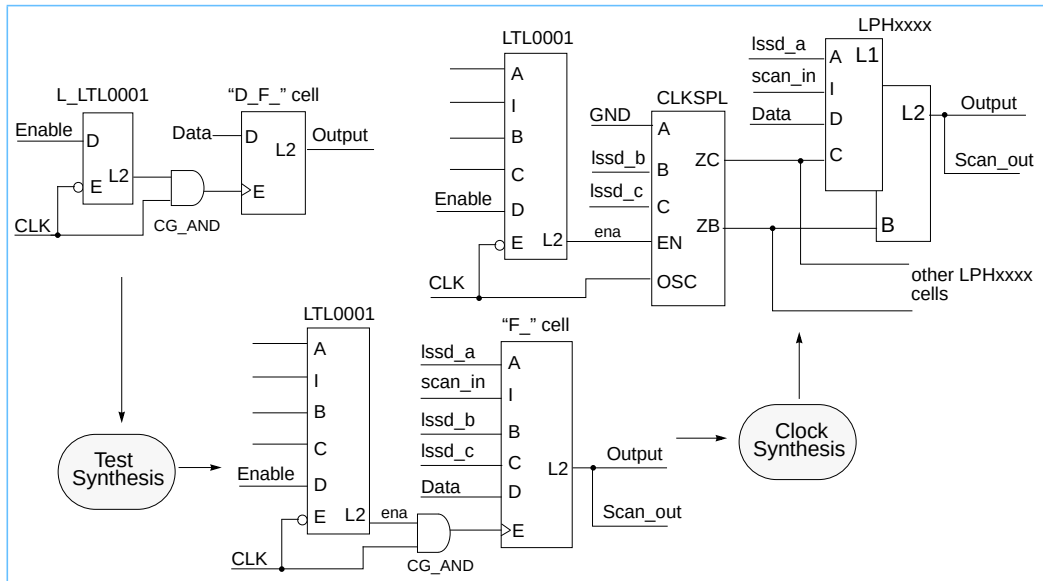


“CG_” (Clock Gating) Cells

There are two clock gating pseudocells in the library which are used to implement synthesized or inferred clock gating. They are the CG_AND and CG_OR cells. These cells are used by the Synopsys Power Compiler or IBM BooleDozer synthesis tools when requesting a clock gating implementation.

The CG_AND cell is used to hold the edge clock low, which prevents the L2 latch of the L1/L2 shift register latch from launching new data. This pseudocell is removed from the netlist during clock synthesis, where the equivalent gating function is implemented using the clock splitter cell (see Figure 7 on page 83). Using this technique, the enable signal must arrive while the clock is low and remain stable while the clock is high. A transparent latch is used with this gating technique to ensure that the enable signal remains stable while the clock is high. Setup and hold tests have been coded in these cells to mimic the actual requirements of the gating implementation at the clock splitter.

Figure 7. Mapping “D_F_” Cell with Clock AND Gating to LPHxxxx Cells with Shared Clock Splitter Cell



The CG_OR cell is used to hold the edge clock high, which prevents the L1 latch of the L1/L2 shift register latch from capturing new data. This pseudocell is removed from the netlist during clock synthesis, where the equivalent gating function is implemented using the clock splitter cell and an additional AND gate (see Figure 8 on page 84). Using this technique, the enable signal must arrive while the clock is high and remain stable while the clock is low. As a result, the enable signal has only half a cycle for its setup test. Setup and hold tests have been coded in these cells to mimic the actual requirements of the gating implementation at the clock splitter.

[illegible]

These cells support the map from latch-based level-sensitive designs to IBM LSSD latches. The Synopsys Test Compiler or IBM ASIC Design Kit can be used to perform this map, or it may be done by an IBM Design Services group. Refer to Figure 9.

The diagram illustrates the synthesis of a custom "L_" cell into a standard IBM ASIC Library LTL0001 Series Cell. On the left, the "L_" cell is shown with inputs DATA and ENABLE (active low, marked with a bubble) and an output L2. An arrow labeled "Test Synthesis" points to the right, where the IBM ASIC Library LTL0001 Series Cell is shown. This library cell has inputs A, B, C, I, DATA, and ENABLE (active low), and an output L2. The synthesis process maps the custom cell's functionality to the library cell's internal structure.

Product Overview

Input/Output Cells

Overview

This section summarizes the input/output (I/O) cells. Logical and electrical information is also shown. The performance and slew rate (di/dt) of the drivers are chosen by selecting the performance level.

Boundary-Scan Overview

This section provides a brief description of boundary-scan, how it works, and how to use it. For more information on boundary-scan and LSSD testing, obtain the appropriate application note from your IBM representative.

An LSSD boundary-scan network is a physical unit (chip, package, card, board, etc.) whose internal logic and array functions can be tested independent of its external connections, and vice versa. Boundary-scan permits complete functional tests (wafer, package, etc.) with tools having fewer pins than the product. Boundary-scan allows designers to exploit card-level self-test for system reliability and serviceability test and diagnostics, and greatly simplifies inter-card wiring tests.

Boundary-scan can be viewed conceptually as breaking a chip into two primary parts: boundary logic and internal logic. Two I/O types are available to bring signals into and out of each of these parts. The first I/O type, referred to here as 'nontest I/O,' must be wired directly to latches that make up the boundary logic. The second I/O type, referred to here as 'test I/O,' is used to bring test function inputs and outputs directly to and from the internal logic and nontest I/Os. A chip can use a maximum of 64 test I/Os, and must be placed in one of 64 I/O cells reserved on each die for test functions. Test I/Os can be multiplexed with normal ASIC I/O functions. Nontest I/Os usually are placed in the remaining cells but can be placed in the 64 reserved cells.

DI and RI Lines

Among the test function primary inputs required to implement boundary-scan are the RI (receiver inhibit) and DI (driver inhibit) inputs that gate I/Os during test. All ASICs must have DI1, DI2, and RI inputs.

The RI line gates all nontest receivers during test to prevent “X” states from entering the network. The output of the receiver is set to a known state (“0”) when the RI line is deactivated (“0”).

Each DI line is used to inhibit the outputs of all the drivers to which it connects. In addition, the DI signals provide simultaneous switching control during test by forcing the drivers to switch sequentially. Two DI lines are required to give separate test control for nontest and test drivers for off-package connection:

DI1	Nontest drivers
DI2	Test drivers (including bidirectionals)

Every SA-27E driver has a DI input (pin DI1, DI2) and DI output (pin ZDI). Likewise, nontest receivers and all receivers with pull-up resistors have an RI input (pin RI) and an RI output (pin ZRI).

The DI and RI signals are wired in a sequential ‘daisy chain’ fashion around the product. DI or RI inputs from any I/O will come from the ZDI or ZRI output of the previous I/O. The starting and ending points for these loops, one for each of the DI1, DI2, and RI, come from the DI and RI receiver cells. These cells are test receivers, and their function is selected through the cell name (see the logic tables for test receivers).

RI and DI lines are brought onto the chip through test receivers. DI1 receivers can be placed anywhere within the 64 valid locations for test function pins. DI2 receivers occupy fixed locations on each die that are among the 64 valid locations for test function pins.

Contact your IBM application engineer for more information on boundary-scan.

RG Lines

The RG (receiver gate) input is provided on many I/Os. This input is similar in function to the RI input, which is used to disable off-chip receivers during product testing. However, unlike the RI input pin, the RG input pin may be controlled by customer logic to gate individual receivers off to reduce power dissipation when signal propagation is not required. If the RG pin is not used, it must be tied to V_{dd} for proper receiver operation.

TS Lines

The TS (three-state) control input is provided on all drivers. This input pin is used to set the driver into a three-state mode when its function is not required. When the TS input is set to a “0”, the driver goes into a high-impedance state, and power consumption is significantly reduced.

Receiver Hysteresis

Hysteresis contributes to noise immunity. It describes how resistant a receiver is to noise impulses appearing at its input. Hysteresis is generated via the PAD to ZH path in typical SA-27E CIO and stand-alone receiver cells.

Noise immunity varies according to the combination of voltage, temperature, and process conditions. Noise immunity for SA-27E receivers is shown below.

Table 35. Receiver Noise Immunity

Receiver	Noise Immunity	Voltage Range
1.8V CMOS receiver	180–210 mV	1.65–1.95V
2.5V CMOS receiver	460–520 mV	2.3–2.7V
3.3V LVTTTL receiver	350–420 mV	3.0–3.6V
Note: Temperature 0°C–100°C, process slow–fast.		

Pull-Up Devices

Any I/O cell that has PU (pull-up) in the name signifies that the I/O contains an internal pull-up device. This pull-up assures that a logic “1” is applied to the internal receiver circuit when the input pin is left floating. However, it does not ensure a logic “1” level at the input pin. If the system design requires that the input pin be at a “1” level, users should supply an external pull-up resistor of their own.

Performance Level Usage for Drivers

The performance level selects output di/dt and performance level for drivers. Table 37 on page 91 and Table 38 on page 100 show the performance level and corresponding slew rates for the I/O cells.

I/O Pin Naming Conventions

These conventions cover most nontest and test driver, receiver, and common I/O cells.

Table 36. I/O Pin Naming Conventions

Pin	Description
A	Driver data input
DI	DI1-DI2 input, driver inhibit input (DI in)
LT	Leakage test (LT in)
MC	Mode control
PAD	Three-state driver output pin/receiver data input pin
RE	Receiver enable
RG	Receiver gate control (receiver disable)
RI	Receiver inhibit input (RI in)
TE	Test enable
TS	Three-state control
TT	Termination test input (TT in)
Z	Noninverting receiver output
ZDI	DI1 - DI2 output, driver inhibit output for daisy chain (DI out)
ZH	Hysteresis receiver output
ZLT	Leakage test output (LT out)
ZMC	Mode control output
ZRE	Receiver enable output
ZRI	Receiver inhibit output for daisy chain (RI out)
ZTE	Test enable output
ZTT	Termination test output (TT out)

High-Voltage Interface

Although the SA-27E nominal supply voltage is 1.8V, high-voltage I/O interface types are designed to withstand 2.5V, 3.3V, and 5.0V buses without damage.

BC25xx I/O cells	Can be used on 2.5V nets, and drive 2.5V levels. These cells require an on-chip 2.5V bus.
BP25xx I/O cells	3.3V tolerant. These cells can be used on 3.3V nets, but drive 2.5V levels. These cells do not require an on-chip 3.3V bus.
BP33xx I/O cells	5.0V tolerant. These cells can be used on 5.0V nets, and drive 3.3V levels. These cells do not require an on-chip 5.0V bus.
BT33xx I/O cells	Fully LVTTTL compliant. These cells can be used on 3.3V nets, and drive 3.3V levels. These cells require an on-chip 3.3V bus.

I/O Propagation Delays

The delay and timing information provided for each cell in this databook are for **estimation** purposes only. The delays shown are calculated for different process, temperature, and voltage conditions.

Propagation delays are presented for each cell as a function of standard loads. One standard load for drivers is referred to as D_{std} , and is not the same value of one standard load for receivers (Table 26, "Input Transition Times and Standard Load Equivalences," on page 61 shows the value of one standard load for drivers and receivers).

I/O Capacitance Tables

In this databook, capacitance tables for I/Os are shown in terms of N_{std} , or the number of standard loads. This means that to translate the capacitance tables to represent picofarads (pF), the value shown in the table needs to be multiplied by the value of one standard load, which for all capacitance tables is 0.006 pF. It should be noted that the delays for drivers were calculated using an external standard load (D_{std}) of 1.000 pF, and the delays for receivers were calculated using an internal standard load (N_{std}) of 0.006 pF.

I/O Impedance

The impedance value listed for each I/O is the approximate impedance of an I/O at nominal process, 50°C, and nominal supply voltage. The information is provided for designers interested in driving a known transmission line impedance.

DC or Limited-Function Test I/Os

Up to 56 limited-function test I/Os, more commonly called DC test I/Os, are available for interfacing to low-speed tester channels. These test-control signals are held either high or low during tests, and don't switch often. By using these limited-function DC test I/Os where applicable, more of the 64 high-function, high-speed AC test I/Os are available for scan chains, reducing test time.

DC test I/Os can be shared with functional signals in the same way that test I/Os are shared. Contact your IBM ASIC representative for more information on pin sharing.

The following signals can be considered DC test signals:

LT	Leakage test signal that inhibits current for I_{ddq} testing.
TE	Test enable signal used in some pin-sharing applications to establish test mode.
RE	Reference enable input used to provide an internally-generated voltage reference for I/O buffers requiring a reference voltage during die testing.
MC	Mode control input used to allow testing of certain I/O buffers that have multiple modes of operation.

AVDD (PLL) Analog voltage supplied by a tester channel during ASIC testing.

Notes:

1. A DC test pad can be used for any DC test signal or any nontest signal.
2. AC test pads can be used for AC test signals, DC test signals, or nontest signals.
3. Nontest pads can be used only for nontest signals.
4. Any nontest I/O library cell can be used for nontest signals, regardless of what type of pad is connect to the nontest I/O cell.
5. Any test I/O library cell can be used for AC test signals, with the exception that specific test receivers must be used for specific AC test signals (for example, DI1, DI2, and RI).

Specific test receivers must be used for DC test signals: LT, TE, RE, MC, etc. A receiver associated with a DC test signal can be connected to either a DC or AC test pad.



I/O Specifications

The following tables summarize the I/O library. The di/dt slew rates are listed if applicable.

Table 37. Nontest Three-State Common I/Os

I/O Name	Performance Level	Function
BAGP2X4X, BAGP2X4X_PM		AGP 2X/4X Dual Mode Nontest CIO
	A	140 mA/ns slew rate 2X mode, 130 mA/ns slew rate 4X mode
BAGP4X, BAGP4X_PM		1.5V AGP 4X Nontest 3-State CIO
	A	75 mA/ns slew rate
	B	85 mA/ns slew rate
	C	95 mA/ns slew rate
BATAUDMA, BATAUDMA_PM		3.3V (5V Protected) Nontest UDMA 33/66/100 Data and Strobe 3-State CIO
	C	variable slew rate
	D	
BC1820, BC1820_PM		1.8V CMOS Nontest 20 Ohm 3-State CIO
	A	55 mA/ns slew rate
	B	70 mA/ns slew rate
	C	90 mA/ns slew rate
BC1835, BC1835_PM		1.8V CMOS Nontest 35 Ohm 3-State CIO
	A	50 mA/ns slew rate
	B	65 mA/ns slew rate
	C	85 mA/ns slew rate
BC1850, BC1850_PM		1.8V CMOS Nontest 50 Ohm 3-State CIO
	A	45 mA/ns slew rate
	B	60 mA/ns slew rate
	C	80 mA/ns slew rate

Table 37. Nontest Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BC1865, BC1865_PM		1.8V CMOS Nontest 65 Ohm 3-State CIO
	A	45 mA/ns slew rate
	B	60 mA/ns slew rate
	C	80 mA/ns slew rate
BC1890, BC1890_PM		1.8V CMOS Nontest 90 Ohm 3-State CIO
	A	40 mA/ns slew rate
	B	60 mA/ns slew rate
	C	75 mA/ns slew rate
BC1820PD, BC1820PD_PM		1.8V CMOS Nontest 20 Ohm 3-State CIO w/Pull-Down
	A	55 mA/ns slew rate
	B	70 mA/ns slew rate
	C	90 mA/ns slew rate
BC1835PD, BC1835PD_PM		1.8V CMOS Nontest 35 Ohm 3-State CIO w/Pull-Down
	A	50 mA/ns slew rate
	B	65 mA/ns slew rate
	C	85 mA/ns slew rate
BC1850PD, BC1850PD_PM		1.8V CMOS Nontest 50 Ohm 3-State CIO w/Pull-Down
	A	45 mA/ns slew rate
	B	60 mA/ns slew rate
	C	80 mA/ns slew rate
BC1865PD, BC1865PD_PM		1.8V CMOS Nontest 65 Ohm 3-State CIO w/Pull-Down
	A	45 mA/ns slew rate
	B	60 mA/ns slew rate
	C	80 mA/ns slew rate
BC1890PD, BC1890PD_PM		1.8V CMOS Nontest 90 Ohm 3-State CIO w/Pull-Down
	A	40 mA/ns slew rate
	B	60 mA/ns slew rate
	C	75 mA/ns slew rate



Table 37. Nontest Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BC1820PU, BC1820PU_PM		1.8V CMOS Nontest 20 Ohm 3-State CIO w/Pull-Up
	A	55 mA/ns slew rate
	B	70 mA/ns slew rate
	C	90 mA/ns slew rate
BC1835PU, BC1835PU_PM		1.8V CMOS Nontest 35 Ohm 3-State CIO w/Pull-Up
	A	50 mA/ns slew rate
	B	65 mA/ns slew rate
	C	85 mA/ns slew rate
BC1850PU, BC1850PU_PM		1.8V CMOS Nontest 50 Ohm 3-State CIO w/Pull-Up
	A	45 mA/ns slew rate
	B	60 mA/ns slew rate
	C	80 mA/ns slew rate
BC1865PU, BC1865PU_PM		1.8V CMOS Nontest 65 Ohm 3-State CIO w/Pull-Up
	A	45 mA/ns slew rate
	B	60 mA/ns slew rate
	C	80 mA/ns slew rate
BC1890PU, BC1890PU_PM		1.8V CMOS Nontest 90 Ohm 3-State CIO w/Pull-Up
	A	40 mA/ns slew rate
	B	60 mA/ns slew rate
	C	75 mA/ns slew rate
BC2520, BC2520_PM		2.5V CMOS Nontest 20 Ohm 3-State CIO
	A	80 mA/ns slew rate
	B	100 mA/ns slew rate
	C	125 mA/ns slew rate
BC2535, BC2535_PM		2.5V CMOS Nontest 35 Ohm 3-State CIO
	A	70 mA/ns slew rate
	B	95 mA/ns slew rate
	C	120 mA/ns slew rate

Table 37. Nontest Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BC2550, BC2550_PM		2.5V CMOS Nontest 50 Ohm 3-State CIO
	A	65 mA/ns slew rate
	B	90 mA/ns slew rate
	C	115 mA/ns slew rate
BC2565, BC2565_PM		2.5V CMOS Nontest 65 Ohm 3-State CIO
	A	65 mA/ns slew rate
	B	85 mA/ns slew rate
	C	110 mA/ns slew rate
BC2590, BC2590_PM		2.5V CMOS Nontest 90 Ohm 3-State CIO
	A	65 mA/ns slew rate
	B	75 mA/ns slew rate
	C	95 mA/ns slew rate
BC2520PD, BC2520PD_PM		2.5V CMOS Nontest 20 Ohm 3-State CIO w/Pull-Down
	A	80 mA/ns slew rate
	B	100 mA/ns slew rate
	C	125 mA/ns slew rate
BC2535PD, BC2535PD_PM		2.5V CMOS Nontest 35 Ohm 3-State CIO w/Pull-Down
	A	70 mA/ns slew rate
	B	95 mA/ns slew rate
	C	120 mA/ns slew rate
BC2550PD, BC2550PD_PM		2.5V CMOS Nontest 50 Ohm 3-State CIO w/Pull-Down
	A	65 mA/ns slew rate
	B	90 mA/ns slew rate
	C	115 mA/ns slew rate
BC2565PD, BC2565PD_PM		2.5V CMOS Nontest 65 Ohm 3-State CIO w/Pull-Down
	A	65 mA/ns slew rate
	B	85 mA/ns slew rate
	C	110 mA/ns slew rate

Table 37. Nontest Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BC2590PD, BC2590PD_PM		2.5V CMOS Nontest 90 Ohm 3-State CIO w/Pull-Down
	A	65 mA/ns slew rate
	B	75 mA/ns slew rate
	C	95 mA/ns slew rate
BC2520PU, BC2520PU_PM		2.5V CMOS Nontest 20 Ohm 3-State CIO w/Pull-Up
	A	80 mA/ns slew rate
	B	100 mA/ns slew rate
	C	125 mA/ns slew rate
BC2535PU, BC2535PU_PM		2.5V CMOS Nontest 35 Ohm 3-State CIO w/Pull-Up
	A	70 mA/ns slew rate
	B	95 mA/ns slew rate
	C	120 mA/ns slew rate
BC2550PU, BC2550PU_PM		2.5V CMOS Nontest 50 Ohm 3-State CIO w/Pull-Up
	A	65 mA/ns slew rate
	B	90 mA/ns slew rate
	C	115 mA/ns slew rate
BC2565PU, BC2565PU_PM		2.5V CMOS Nontest 65 Ohm 3-State CIO w/Pull-Up
	A	65 mA/ns slew rate
	B	85 mA/ns slew rate
	C	110 mA/ns slew rate
BC2590PU, BC2590PU_PM		2.5V CMOS Nontest 90 Ohm 3-State CIO w/Pull-Up
	A	65 mA/ns slew rate
	B	75 mA/ns slew rate
	C	95 mA/ns slew rate
BGTLD, BGTLD_PM		Nontest GTL CIO for Double Termination
	A	75 mA/ns slew rate
	B	110 mA/ns slew rate

Table 37. Nontest Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BGTLS, BGTLS_PM		Nontest GTL CIO for Single Termination
	A	75 mA/ns slew rate
	B	125 mA/ns slew rate
BHSTL18C1, BHSTL18C1_PM		HSTL 1.8V Class 1 Nontest CIO
	A	75 mA/ns slew rate
	B	125 mA/ns slew rate
BHSTL18C2, BHSTL18C2_PM		HSTL 1.8V Class 2 Nontest CIO
	A	150 mA/ns slew rate
	B	150 mA/ns slew rate
BHSTLC1, BHSTLC1_PM		HSTL 1.5V Class 1 Nontest CIO
	A	100 mA/ns slew rate
	B	120 mA/ns slew rate
BHSTLC2, BHSTLC2_PM		HSTL 1.5V Class 2 Nontest CIO
	A	100 mA/ns slew rate
	B	120 mA/ns slew rate
BI2C25, BI2C25_PM		2.5V Nontest I2C CIO
	A	25 mA/ns slew rate
BI2C33, BI2C33_PM		3.3V Nontest I2C CIO
	A	20 mA/ns slew rate
BP2520, BP2520_PM		2.5V (3.3V Tolerant) CMOS Nontest 20 Ohm 3-State CIO
	A	90 mA/ns slew rate
	B	120 mA/ns slew rate
BP2535, BP2535_PM		2.5V (3.3V Tolerant) CMOS Nontest 35 Ohm 3-State CIO
	A	80 mA/ns slew rate
	B	120 mA/ns slew rate
BP2550, BP2550_PM		2.5V (3.3V Tolerant) CMOS Nontest 50 Ohm 3-State CIO
	A	80 mA/ns slew rate
	B	115 mA/ns slew rate

Table 37. Nontest Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BP2565, BP2565_PM		2.5V (3.3V Tolerant) CMOS Nontest 65 Ohm 3-State CIO
	A	80 mA/ns slew rate
	B	115 mA/ns slew rate
BP2590, BP2590_PM		2.5V (3.3V Tolerant) CMOS Nontest 90 Ohm 3-State CIO
	A	80 mA/ns slew rate
	B	110 mA/ns slew rate
BP3320, BP3320_PM		3.3V LVTTTL (5V Protected) Nontest 20 Ohm 3-State CIO
	A	100 mA/ns slew rate
	B	135 mA/ns slew rate
BP3335, BP3335_PM		3.3V LVTTTL (5V Protected) Nontest 35 Ohm 3-State CIO
	A	90 mA/ns slew rate
	B	125 mA/ns slew rate
BP3350, BP3350_PM		3.3V LVTTTL (5V Protected) Nontest 50 Ohm 3-State CIO
	A	80 mA/ns slew rate
	B	130 mA/ns slew rate
BP3365, BP3365_PM		3.3V LVTTTL (5V Protected) Nontest 65 Ohm 3-State CIO
	A	75 mA/ns slew rate
	B	105 mA/ns slew rate
BP3390, BP3390_PM		3.3V LVTTTL (5V Protected) Nontest 90 Ohm 3-State CIO
	A	75 mA/ns slew rate
	B	100 mA/ns slew rate
BPCIX3, BPCIX3_PM		3.3V PCI-X/PCI Nontest 3-State CIO
	A	180 mA/ns slew rate
BPCIX3PU, BPCIX3PU_PM		3.3V PCI-X/PCI Nontest 3-State CIO w/Pull-Up
	A	180 mA/ns slew rate
BPCI5, BPCI5_PM		3.3V/5V Tolerant PCI Nontest 3-State CIO
	A	190 mA/ns slew rate

Table 37. Nontest Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BSSTL2C1, BSSTL2C1_PM		SSTL 2.5V Class 1 Nontest 3-State CIO
	A	70 mA/ns slew rate
	B	95 mA/ns slew rate
BSSTL2C2, BSSTL2C2_PM		SSTL 2.5V Class 2 Nontest 3-State CIO
	A	110 mA/ns slew rate
	B	150 mA/ns slew rate
BSSTL2DIFF, BSSTL2DIFF_PM		2.5V BSSTL2DIFF Differential CIO Nontest
	A	140 mA/ns slew rate
BSSTL2C50, BSSTL2C50_PM		2.5V SSTL Nontest 3-State CIO With Half-Strength Driver
	A	120 mA/ns slew rate
	B	180 mA/ns slew rate
BSSTL2C56, BSSTL2C56_PM		2.5V SSTL Nontest 3-State CIO With Half-Strength Driver
	A	120 mA/ns slew rate
	B	170 mA/ns slew rate
BT3320, BT3320_PM		3.3V LVTTTL Nontest 20 Ohm 3-State CIO
	A	100 mA/ns slew rate
	B	135 mA/ns slew rate
BT3335, BT3335_PM		3.3V LVTTTL Nontest 35 Ohm 3-State CIO
	A	90 mA/ns slew rate
	B	125 mA/ns slew rate
BT3350, BT3350_PM		3.3V LVTTTL Nontest 50 Ohm 3-State CIO
	A	80 mA/ns slew rate
	B	130 mA/ns slew rate
BT3350LV, BT3350LV_PM		Low Voltage 3.3V LVTTTL Nontest 50 Ohm 3-State CIO
	A	90 mA/ns slew rate
BT3365, BT3365_PM		3.3V LVTTTL Nontest 65 Ohm 3-State CIO
	A	75 mA/ns slew rate
	B	105 mA/ns slew rate

Table 37. Nontest Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BT3390, BT3390_PM		3.3V LVTTTL Nontest 90 Ohm 3-State CIO
	A	75 mA/ns slew rate
	B	100 mA/ns slew rate
BT3320PD, BT3320PD_PM		3.3V LVTTTL Nontest 20 Ohm 3-State CIO w/Pull-Down
	A	100 mA/ns slew rate
	B	135 mA/ns slew rate
BT3335PD, BT3335PD_PM		3.3V LVTTTL Nontest 35 Ohm 3-State CIO w/Pull-Down
	A	90 mA/ns slew rate
	B	125 mA/ns slew rate
BT3350PD, BT3350PD_PM		3.3V LVTTTL Nontest 50 Ohm 3-State CIO w/Pull-Down
	A	80 mA/ns slew rate
	B	130 mA/ns slew rate
BT3350LVPD, BT3350LVPD_PM		Low Voltage 3.3V LVTTTL Nontest 50 Ohm 3-State CIO w/Pull-Down
	A	90 mA/ns slew rate
BT3365PD, BT3365PD_PM		3.3V LVTTTL Nontest 65 Ohm 3-State CIO w/Pull-Down
	A	75 mA/ns slew rate
	B	105 mA/ns slew rate
BT3390PD, BT3390PD_PM		3.3V LVTTTL Nontest 90 Ohm 3-State CIO w/Pull-Down
	A	75 mA/ns slew rate
	B	105 mA/ns slew rate
BT3320PU, BT3320PU_PM		3.3V LVTTTL Nontest 20 Ohm 3-State CIO w/Pull-Up
	A	100 mA/ns slew rate
	B	135 mA/ns slew rate
BT3335PU, BT3335PU_PM		3.3V LVTTTL Nontest 35 Ohm 3-State CIO w/Pull-Up
	A	90 mA/ns slew rate
	B	125 mA/ns slew rate

Table 37. Nontest Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BT3350PU, BT3350PU_PM		3.3V LVTTL Nontest 50 Ohm 3-State CIO w/Pull-Up
	A	80 mA/ns slew rate
	B	130 mA/ns slew rate
BT3350LVPU, BT3350LVPU_PM		Low Voltage 3.3V LVTTL Nontest 50 Ohm 3-State CIO w/Pull-Up
	A	90 mA/ns slew rate
BT3365PU, BT3365PU_PM		3.3V LVTTL Nontest 65 Ohm 3-State CIO w/Pull-Up
	A	75 mA/ns slew rate
	B	105 mA/ns slew rate
BT3390PU, BT3390PU_PM		3.3V LVTTL Nontest 90 Ohm 3-State CIO w/Pull-Up
	A	75 mA/ns slew rate
	B	105 mA/ns slew rate
BUSB2		USB Nontest 3-State CIO
	A	70 mA/ns slew rate (low speed); 80 mA/ns slew rate (full speed)

Table 38. Test Three-State Common I/Os

I/O Name	Performance Level	Function
BAGP2X4XT, BAGP2X4XT_PM		AGP 2X/4X Dual Mode Test CIO
	A	140 mA/ns slew rate 2X mode, 130 mA/ns slew rate 4X mode
BAGP4XT, BAGP4XT_PM		1.5V AGP 4X Test 3-State CIO
	A	75 mA/ns slew rate
	B	85 mA/ns slew rate
	C	95 mA/ns slew rate
BATAUDMAT, BATAUDMAT_PM		3.3V (5V Protected) Test UDMA 33/66/100 Data and Strobe 3-State CIO
	C	variable slew rate
	D	



Table 38. Test Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BC1820T, BC1820T_PM		1.8V CMOS Test 20 Ohm 3-State CIO
	A	55 mA/ns slew rate
	B	70 mA/ns slew rate
	C	90 mA/ns slew rate
BC1835T, BC1835T_PM		1.8V CMOS Test 35 Ohm 3-State CIO
	A	50 mA/ns slew rate
	B	65 mA/ns slew rate
	C	85 mA/ns slew rate
BC1850T, BC1850T_PM		1.8V CMOS Test 50 Ohm 3-State CIO
	A	45 mA/ns slew rate
	B	60 mA/ns slew rate
	C	80 mA/ns slew rate
BC1865T, BC1865T_PM		1.8V CMOS Test 65 Ohm 3-State CIO
	A	45 mA/ns slew rate
	B	60 mA/ns slew rate
	C	80 mA/ns slew rate
BC1890T, BC1890T_PM		1.8V CMOS Test 90 Ohm 3-State CIO
	A	40 mA/ns slew rate
	B	60 mA/ns slew rate
	C	75 mA/ns slew rate
BC1820PDT, BC1820PDT_PM		1.8V CMOS Test 20 Ohm 3-State CIO w/Pull-Down
	A	55 mA/ns slew rate
	B	70 mA/ns slew rate
	C	90 mA/ns slew rate
BC1835PDT, BC1835PDT_PM		1.8V CMOS Test 35 Ohm 3-State CIO w/Pull-Down
	A	50 mA/ns slew rate
	B	65 mA/ns slew rate
	C	85 mA/ns slew rate

Table 38. Test Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BC1850PDT, BC1850PDT_PM		1.8V CMOS Test 50 Ohm 3-State CIO w/Pull-Down
	A	45 mA/ns slew rate
	B	60 mA/ns slew rate
	C	80 mA/ns slew rate
BC1865PDT, BC1865PDT_PM		1.8V CMOS Test 65 Ohm 3-State CIO w/Pull-Down
	A	45 mA/ns slew rate
	B	60 mA/ns slew rate
	C	80 mA/ns slew rate
BC1890PDT, BC1890PDT_PM		1.8V CMOS Test 90 Ohm 3-State CIO w/Pull-Down
	A	40 mA/ns slew rate
	B	60 mA/ns slew rate
	C	75 mA/ns slew rate
BC1820PUT, BC1820PUT_PM		1.8V CMOS Test 20 Ohm 3-State CIO w/Pull-Up
	A	55 mA/ns slew rate
	B	70 mA/ns slew rate
	C	90 mA/ns slew rate
BC1835PUT, BC1835PUT_PM		1.8V CMOS Test 35 Ohm 3-State CIO w/Pull-Up
	A	50 mA/ns slew rate
	B	65 mA/ns slew rate
	C	85 mA/ns slew rate
BC1850PUT, BC1850PUT_PM		1.8V CMOS Test 50 Ohm 3-State CIO w/Pull-Up
	A	45 mA/ns slew rate
	B	60 mA/ns slew rate
	C	80 mA/ns slew rate
BC1865PUT, BC1865PUT_PM		1.8V CMOS Test 65 Ohm 3-State CIO w/Pull-Up
	A	45 mA/ns slew rate
	B	60 mA/ns slew rate
	C	80 mA/ns slew rate

Table 38. Test Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BC1890PUT, BC1890PUT_PM		1.8V CMOS Test 90 Ohm 3-State CIO w/Pull-Up
	A	40 mA/ns slew rate
	B	60 mA/ns slew rate
	C	75 mA/ns slew rate
BC2520T, BC2520T_PM		2.5V CMOS Test 20 Ohm 3-State CIO
	A	80 mA/ns slew rate
	B	100 mA/ns slew rate
	C	125 mA/ns slew rate
BC2535T, BC2535T_PM		2.5V CMOS Test 35 Ohm 3-State CIO
	A	70 mA/ns slew rate
	B	95 mA/ns slew rate
	C	120 mA/ns slew rate
BC2550T, BC2550T_PM		2.5V CMOS Test 50 Ohm 3-State CIO
	A	65 mA/ns slew rate
	B	90 mA/ns slew rate
	C	115 mA/ns slew rate
BC2565T, BC2565T_PM		2.5V CMOS Test 65 Ohm 3-State CIO
	A	65 mA/ns slew rate
	B	85 mA/ns slew rate
	C	110 mA/ns slew rate
BC2590T, BC2590T_PM		2.5V CMOS Test 90 Ohm 3-State CIO
	A	65 mA/ns slew rate
	B	75 mA/ns slew rate
	C	95 mA/ns slew rate
BC2520PDT, BC2520PDT_PM		2.5V CMOS Test 20 Ohm 3-State CIO w/Pull-Down
	A	80 mA/ns slew rate
	B	100 mA/ns slew rate
	C	125 mA/ns slew rate

Table 38. Test Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BC2535PDT, BC2535PDT_PM		2.5V CMOS Test 35 Ohm 3-State CIO w/Pull-Down
	A	70 mA/ns slew rate
	B	95 mA/ns slew rate
	C	120 mA/ns slew rate
BC2550PDT, BC2550PDT_PM		2.5V CMOS Test 50 Ohm 3-State CIO w/Pull-Down
	A	65 mA/ns slew rate
	B	90 mA/ns slew rate
	C	115 mA/ns slew rate
BC2565PDT, BC2565PDT_PM		2.5V CMOS Test 65 Ohm 3-State CIO w/Pull-Down
	A	65 mA/ns slew rate
	B	85 mA/ns slew rate
	C	110 mA/ns slew rate
BC2590PDT, BC2590PDT_PM		2.5V CMOS Test 90 Ohm 3-State CIO w/Pull-Down
	A	65 mA/ns slew rate
	B	75 mA/ns slew rate
	C	95 mA/ns slew rate
BC2520PUT, BC2520PUT_PM		2.5V CMOS Test 20 Ohm 3-State CIO w/Pull-Up
	A	80 mA/ns slew rate
	B	100 mA/ns slew rate
	C	125 mA/ns slew rate
BC2535PUT, BC2535PUT_PM		2.5V CMOS Test 35 Ohm 3-State CIO w/Pull-Up
	A	70 mA/ns slew rate
	B	95 mA/ns slew rate
	C	120 mA/ns slew rate
BC2550PUT, BC2550PUT_PM		2.5V CMOS Test 50 Ohm 3-State CIO w/Pull-Up
	A	65 mA/ns slew rate
	B	90 mA/ns slew rate
	C	115 mA/ns slew rate



Table 38. Test Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BC2565PUT, BC2565PUT_PM		2.5V CMOS Test 65 Ohm 3-State CIO w/Pull-Up
	A	65 mA/ns slew rate
	B	85 mA/ns slew rate
	C	110 mA/ns slew rate
BC2590PUT, BC2590PUT_PM		2.5V CMOS Test 90 Ohm 3-State CIO w/Pull-Up
	A	65 mA/ns slew rate
	B	75 mA/ns slew rate
	C	95 mA/ns slew rate
BGTLDT, BGTLDT_PM		Test GTL CIO for Double Termination
	A	75 mA/ns slew rate
	B	110 mA/ns slew rate
BGTLST, BGTLST_PM		Test GTL CIO for Single Termination
	A	75 mA/ns slew rate
	B	125 mA/ns slew rate
BHSTL18C1T, BHSTL18C1T_PM		HSTL 1.8V Class 1 Test CIO
	A	75 mA/ns slew rate
	B	125 mA/ns slew rate
BHSTL18C2T, BHSTL18C2T_PM		HSTL 1.8V Class 2 Test CIO
	A	150 mA/ns slew rate
	B	150 mA/ns slew rate
BHSTLC1T, BHSTLC1T_PM		HSTL 1.5V Class 1 Test CIO
	A	100 mA/ns slew rate
	B	120 mA/ns slew rate
BHSTLC2T, BHSTLC2T_PM		HSTL 1.5V Class 2 Test CIO
	A	100 mA/ns slew rate
	B	120 mA/ns slew rate

Table 38. Test Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BP2520T, BP2520T_PM		2.5V (3.3V Tolerant) CMOS Test 20 Ohm 3-State CIO
	A	90 mA/ns slew rate
	B	120 mA/ns slew rate
BP2535T, BP2535T_PM		2.5V (3.3V Tolerant) CMOS Test 35 Ohm 3-State CIO
	A	80 mA/ns slew rate
	B	120 mA/ns slew rate
BP2550T, BP2550T_PM		2.5V (3.3V Tolerant) CMOS Test 50 Ohm 3-State CIO
	A	80 mA/ns slew rate
	B	115 mA/ns slew rate
BP2565T, BP2565T_PM		2.5V (3.3V Tolerant) CMOS Test 65 Ohm 3-State CIO
	A	80 mA/ns slew rate
	B	115 mA/ns slew rate
BP2590T, BP2590T_PM		2.5V (3.3V Tolerant) CMOS Test 90 Ohm 3-State CIO
	A	80 mA/ns slew rate
	B	110 mA/ns slew rate
BP3320T, BP3320T_PM		3.3V LVTTL (5V Protected) Test 20 Ohm 3-State CIO
	A	100 mA/ns slew rate
	B	135 mA/ns slew rate
BP3335T, BP3335T_PM		3.3V LVTTL (5V Protected) Test 35 Ohm 3-State CIO
	A	90 mA/ns slew rate
	B	125 mA/ns slew rate
BP3350T, BP3350T_PM		3.3V LVTTL (5V Protected) Test 50 Ohm 3-State CIO
	A	80 mA/ns slew rate
	B	130 mA/ns slew rate
BP3365T, BP3365T_PM		3.3V LVTTL (5V Protected) Test 65 Ohm 3-State CIO
	A	75 mA/ns slew rate
	B	105 mA/ns slew rate

Table 38. Test Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BP3390T, BP3390T_PM		3.3V LVTTTL (5V Protected) Test 90 Ohm 3-State CIO
	A	75 mA/ns slew rate
	B	100 mA/ns slew rate
BPCIX3T, BPCIX3T_PM		3.3V PCI-X/PCI Test 3-State CIO
	A	180 mA/ns slew rate
BPCIX3PUT, BPCIX3PUT_PM		3.3V PCI-X/PCI Test 3-State CIO w/Pull-Up
	A	180 mA/ns slew rate
BPCI5T, BPCI5T_PM		3.3V/5.0V Tolerant, PCI Test 3-State CIO
	A	190 mA/ns slew rate
BSSTL2C1T, BSSTL2C1T_PM		SSTL 2.5V Class 1 Test 3-State CIO
	A	70 mA/ns slew rate
	B	95 mA/ns slew rate
BSSTL2C2T, BSSTL2C2T_PM		SSTL 2.5V Class 2 Test 3-State CIO
	A	110 mA/ns slew rate
	B	150 mA/ns slew rate
BSSTL2C50T, BSSTL2C50T_PM		2.5V SSTL Test 3-State CIO With Half-Strength Driver
	A	130 mA/ns slew rate
	B	170 mA/ns slew rate
BSSTL2C56T, BSSTL2C56T_PM		2.5V SSTL Test 3-State CIO With Half-Strength Driver
	A	130 mA/ns slew rate
	B	160 mA/ns slew rate
BT3320T, BT3320T_PM		3.3V LVTTTL Test 20 Ohm 3-State CIO
	A	100 mA/ns slew rate
	B	135 mA/ns slew rate
BT3335T, BT3335T_PM		3.3V LVTTTL Test 35 Ohm 3-State CIO
	A	90 mA/ns slew rate
	B	125 mA/ns slew rate

Table 38. Test Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BT3350T, BT3350T_PM		3.3V LVTTL Test 50 Ohm 3-State CIO
	A	80 mA/ns slew rate
	B	130 mA/ns slew rate
BT3350LVT, BT3350LVT_PM		Low Voltage 3.3V LVTTL Test 50 Ohm 3-State CIO
	A	90 mA/ns slew rate
BT3365T, BT3365T_PM		3.3V LVTTL Test 65 Ohm 3-State CIO
	A	75 mA/ns slew rate
	B	105 mA/ns slew rate
BT3390T, BT3390T_PM		3.3V LVTTL Test 90 Ohm 3-State CIO
	A	75 mA/ns slew rate
	B	100 mA/ns slew rate
BT3320PDT, BT3320PDT_PM		3.3V LVTTL Test 20 Ohm 3-State CIO w/Pull-Down
	A	100 mA/ns slew rate
	B	135 mA/ns slew rate
BT3335PDT, BT3335PDT_PM		3.3V LVTTL Test 35 Ohm 3-State CIO w/Pull-Down
	A	90 mA/ns slew rate
	B	125 mA/ns slew rate
BT3350PDT, BT3350PDT_PM		3.3V LVTTL Test 50 Ohm 3-State CIO w/Pull-Down
	A	80 mA/ns slew rate
	B	130 mA/ns slew rate
BT3350LVPDT, BT3350LVPDT_PM		Low Voltage 3.3V LVTTL Test 50 Ohm 3-State CIO w/Pull-Down
	A	90 mA/ns slew rate
BT3365PDT, BT3365PDT_PM		3.3V LVTTL Test 65 Ohm 3-State CIO w/Pull-Down
	A	75 mA/ns slew rate
	B	105 mA/ns slew rate
BT3390PDT, BT3390PDT_PM		3.3V LVTTL Test 90 Ohm 3-State CIO w/Pull-Down
	A	75 mA/ns slew rate
	B	100 mA/ns slew rate

Table 38. Test Three-State Common I/Os (Continued)

I/O Name	Performance Level	Function
BT3320PUT, BT3320PUT_PM		3.3V LVTTL Test 20 Ohm 3-State CIO w/Pull-Up
	A	100 mA/ns slew rate
	B	135 mA/ns slew rate
BT3335PUT, BT3335PUT_PM		3.3V LVTTL Test 35 Ohm 3-State CIO w/Pull-Up
	A	90 mA/ns slew rate
	B	125 mA/ns slew rate
BT3350PUT, BT3350PUT_PM		3.3V LVTTL Test 50 Ohm 3-State CIO w/Pull-Up
	A	80 mA/ns slew rate
	B	130 mA/ns slew rate
BT3350LVPUT, BT3350LVPUT_PM		Low Voltage 3.3V LVTTL Test 50 Ohm 3-State CIO w/Pull-Up
	A	90 mA/ns slew rate
BT3365PUT, BT3365PUT_PM		3.3V LVTTL Test 65 Ohm 3-State CIO w/Pull-Up
	A	75 mA/ns slew rate
	B	105 mA/ns slew rate
BT3390PUT, BT3390PUT_PM		3.3V LVTTL Test 90 Ohm 3-State CIO w/Pull-Up
	A	75 mA/ns slew rate
	B	100 mA/ns slew rate

Table 39. Receivers, Standard Cell

Receiver Name	Performance Level	Function
IHSTL, IHSTL_PM	A	HSTL Nontest Differential Receiver
IHSTLTERM, IHSTLTERM_PM	A	1.5V HSTL Receiver with Termination
IHSTL18TERM, IHSTL18TERM_PM	A	1.8V HSTL Nontest Receiver with Termination
ILVDS, ILVDS_PM	A, B	1.8V Nontest LVDS Wide Common Mode Receiver
ILVDSO, ILVDSO_PM	A, B	1.8V Nontest LVDS Wide Common Mode Receiver w/ Terminator
ILVDSAO, ILVDSAO_PM	A	1.8V Nontest LVDS Wide Common Mode Receiver

Table 39. Receivers, Standard Cell (Continued)

Receiver Name	Performance Level	Function
ILVDSDAO, ILVDSDAO_PM	A	1.8V Nontest LVDS Wide Common Mode Receiver with Terminator
IPECL, IPECL_PM	A	1.8V/2.5V PECL Nontest Differential Receiver
ISTI18D, ISTI18D_PM	A	1.8V STI Nontest Terminated Differential Receiver
IC18T, IC18T_PM	A	1.8V CMOS Test Receiver
IC18D1PUT, IC18D1PUT_PM	A	1.8V CMOS Test DI1 Receiver w/Pull-Up
IC18D2PUT, IC18D2PUT_PM	A	1.8V CMOS Test DI2 Receiver w/Pull-Up
IC18DLTPUT, IC18DLTPUT_PM	A	1.8V Embedded DRAM Leakage Test Receiver w/Pull-Up
IC18LTPUT, IC18LTPUT_PM	A	1.8V CMOS Leakage Test Receiver w/Pull-Up
IC18MCT, IC18MCT_PM	A	1.8V CMOS Test Mode Control Receiver
IC18PDT, IC18PDT_PM	A	1.8V CMOS Test Receiver w/Pull-Down
IC18PUT, IC18PUT_PM	A	1.8V CMOS Test Receiver w/Pull-Up
IC18REPDT, IC18REPDT_PM	A	1.8V CMOS Test Reference Enable (RE) Receiver w/Pull-Down
IC18RIT, IC18RIT_PM	A	1.8V CMOS Test RI/TT Receiver
IC18TEPDT, IC18TEPDT_PM	A	1.8V CMOS Test Enable (TE) Receiver w/Pull-Down
IHSTLT, IHSTLT_PM	A	IHSTL Test Differential Receiver
ILVDST, ILVDST_PM	A	1.8V LVDS Wide Common Mode Test Receiver
ILVSDT, ILVSDT_PM	A	1.8V LVDS Wide Common Mode Test Receiver w/Terminator
IP25T, IP25T_PM	A	2.5V CMOS (3.3V Tolerant) Test Receiver
IP25D1T, IP25D1T_PM	A	2.5V CMOS (3.3V Tolerant) Test DI1 Receiver
IP25D2T, IP25D2T_PM	A	2.5V CMOS (3.3V Tolerant) Test DI2 Receiver
IP25LTT, IP25LTT_PM	A	2.5V CMOS (3.3V Tolerant) Leakage Test Receiver
IP25MCT, IP25MCT_PM	A	2.5V CMOS (3.3V Tolerant) Test Mode Control Receiver
IP25RET, IP25RET_PM	A	2.5V CMOS (3.3V Tolerant) Test Reference Enable Receiver

Table 39. Receivers, Standard Cell (Continued)

Receiver Name	Performance Level	Function
IP25RIT, IP25RIT_PM	A	2.5V CMOS (3.3V Tolerant) Test RI/TT Receiver
IP33T, IP33T_PM	A	5.0V Tolerant 3.3V LVTTL Test Receiver
IP33D1T, IP33D1T_PM	A	5.0V Tolerant 3.3V LVTTL Test D1 Receiver
IP33D2T, IP33D2T_PM	A	5.0V Tolerant 3.3V LVTTL Test D2 Receiver
IP33LTT, IP33LTT_PM	A	5.0V Tolerant 3.3V LVTTL Leakage Test Receiver
IP33MCT, IP33MCT_PM	A	5.0V Tolerant 3.3V LVTTL Test Mode Control Receiver
IP33RET, IP33RET_PM	A	5.0V Tolerant 3.3V LVTTL Test Reference Enable Receiver
IP33RIT, IP33RIT_PM	A	5.0V Tolerant 3.3V LVTTL Test RI/TT Receiver
IPECLT, IPECLT_PM	A	1.8V/2.5V PECL Test Differential Receiver
IPECLDT, IPECLDT_PM	A	1.8V/2.5V PECL Test Differential Receiver
IPECLDBDT, IPECLDBDT_PM	A	1.8V/2.5V PECL Test Differential Receiver w/Termination and PLL Delay Balance

Table 40. Drivers, Standard Cell

Driver Name	Performance Level	Function
OHSTL, OHSTL_PM	A	HSTL 1.5V Class 2 Differential Driver
OLVDS, OLVDS_PM	A, B	Low-Voltage Differential Swing Driver (Nontest)
OLVDS18, OLVDS18_PM	A	Low-Voltage Differential Swing Driver (Nontest)
OPLVDS, OPLVDS_PM	A	Pseudo Low-Voltage Differential Swing Driver (Nontest)
OPECL	A	1.8V/3.3V PECL Non-Test Differential Driver
OSTI18, OSTI18_PM	A	1.8V STI Nontest Differential Driver

Table 41. Programmable V_{dd} /GND, Standard Cell

Name	Performance Level	Function
GND_PM_A	A	Programmable Ground
VDD_PM_A	A	Programmable 1.8 Volt Vdd

Table 41. Programmable V_{dd}/GND , Standard Cell (Continued)

Name	Performance Level	Function
VDD150_PM_A	A	Programmable 1.5 Volt Vdd
VDD250_PM_A	A	Programmable 2.5 Volt Vdd
VDD330_PM_A	A	Programmable 3.3 Volt Vdd

Electrical Specifications

Table 42. Definition of Terms

Term	Definition
MAUL	Maximum allowable up level. The maximum voltage that can be applied without affecting the specified reliability. Cell functionality is not implied. Maximum allowable applies to overshoot only.
MPUL	Maximum positive up level. The most positive voltage that maintains cell functionality. The maximum positive logic level.
LPUL	Least positive up level. The least positive voltage that maintains cell functionality. The minimum positive logic level.
MPDL	Most positive down level. The most positive voltage that maintains cell functionality. The maximum negative logic level.
LPDL	Least positive down level. The least positive voltage that maintains cell functionality. The minimum negative logic level.
MADL	Minimum allowable down level. The minimum voltage that can be applied without affecting the specified reliability. Minimum allowable applies to undershoot only. Cell functionality is not implied.

Driver Specifications

Table 43. 1.8V CMOS Driver DC Voltage Specifications

Function	MAUL (V) ¹	MPUL (V)	LPUL (V)	MPDL (V)	LPDL (V)	MADL (V) ²
CMOS	$V_{dd}^3 + 0.45$	V_{dd}^3	$V_{dd}^3 - 0.45$	0.45	0.00	-0.60
- Maximum allowable applies to overshoot only. - Minimum allowable applies to undershoot only. $V_{dd} = 1.65$ to 1.95 volts. - Consult your IBM application engineer if overshoot/undershoot exceeds specifications.						

Table 44. 2.5V CMOS Driver DC Voltage Specifications

Function	MAUL (V) ¹	MPUL (V)	LPUL (V)	MPDL (V)	LPDL (V)	MADL (V) ²
CMOS	$V_{dd250}^3 + 0.6$	V_{dd250}^3	2.0	0.4	0.00	-0.60
1. Maximum allowable applies to overshoot only. 2. Minimum allowable applies to undershoot only. 3. $V_{dd250} = 2.3$ to 2.7 volts. 4. Consult your IBM application engineer if overshoot/undershoot exceeds specifications.						

Table 45. 3.3V Tolerant 2.5V CMOS Driver DC Voltage Specifications¹

Function	MAUL (V) ²	MPUL (V) ³	LPUL (V)	MPDL (V)	LPDL (V)	MADL (V) ⁴
CMOS	3.9	V_{dd250}^5	2.00	0.4	0.00	-0.60
1. All levels adhere to the JEDEC Standard JESD12-6, "Interface Standard for Semi-Custom Integrated Circuits", March 1991. 2. Maximum allowable applies to overshoot only. Output disabled. 3. Output active. 4. Minimum allowable applies to undershoot only. 5. $V_{dd250} = 2.3$ to 2.7 volts.						

Table 46. 3.3V LVTTTL Driver DC Voltage Specifications

Function	MAUL (V) ¹	MPUL (V)	LPUL (V)	MPDL (V)	LPDL (V)	MADL (V) ²
LVTTTL	$V_{dd330}^3 + 0.3$	V_{dd330}^3	2.4	0.4	0.00	-0.60
1. Maximum allowable applies to overshoot only. 2. Minimum allowable applies to undershoot only. 3. $V_{dd330} = 3.0$ to 3.6 volts. 4. Consult your IBM application engineer if overshoot/undershoot exceeds specifications.						

Table 47. 5.0V Tolerant 3.3V LVTTTL Driver DC Voltage Specifications

Function	MAUL (V) ¹	MPUL (V)	LPUL (V)	MPDL (V)	LPDL (V)	MADL (V) ²
LVTTTL	5.5V	V_{dd330} ³	2.4	0.4	0.00	-0.60

1. Maximum allowable applies to overshoot only
2. Minimum allowable applies to undershoot only.
3. $V_{dd330} = 3.0$ to 3.6 volts.
4. Consult your IBM application engineer if overshoot/undershoot exceeds specifications.

Table 48. 1.8V CMOS Driver Minimum DC Currents at Rated Voltage¹

Driver Type	V_{high} (V)	I_{high} (mA)	V_{low} (V)	I_{low} (mA)
CMOS 90 ohm driver outputs	1.2	4.4/23.0 ²	0.45	4.3
CMOS 65 ohm driver outputs	1.2	6.1/23.0 ²	0.45	6.0
CMOS 50 ohm driver outputs	1.2	8.0/23.0 ²	0.45	7.8
CMOS 35 ohm driver outputs	1.2	11.5/23.0 ²	0.45	11.3
CMOS 20 ohm driver outputs	1.2	19.6/23.0 ²	0.45	19.5

1. V_{dd} @ 1.65V, temperature @ 100°C.
2. 23 mA is the electromigration limit for 100k power on hour (POH) @ 100°C and 100% duty cycle. This limit can be adjusted for different temperature, duty cycle, and POH. Consult your IBM application engineer for additional details.

Table 49. 2.5V CMOS Driver Minimum DC Currents at Rated Voltage¹

Driver Type	V_{high} (V)	I_{high} (mA)	V_{low} (V)	I_{low} (mA)
CMOS 90 ohm driver outputs	2.0	2.9/23.0 ²	0.4	3.9
CMOS 65 ohm driver outputs	2.0	4.1/23.0 ²	0.4	5.4
CMOS 50 ohm driver outputs	2.0	5.2/23.0 ²	0.4	6.9
CMOS 35 ohm driver outputs	2.0	7.4/23.0 ²	0.4	9.7
CMOS 20 ohm driver outputs	2.0	13.6/23.0 ²	0.4	17.6

1. V_{dd250} @ 2.3V, temperature @ 100°C.
2. 23 mA is the electromigration limit for 100k power on hour (POH) @ 100°C and 100% duty cycle. This limit can be adjusted for different temperature, duty cycle, and POH. Consult your IBM application engineer for additional details.

Table 50. 3.3V LVTTL Driver Minimum DC Currents at Rated Voltage¹

Driver Type	V _{high} (V)	I _{high} (mA)	V _{low} (V)	I _{low} (mA)
LVTTL 90 ohm driver outputs	2.40	5.9/23.0 ²	0.4	3.9
LVTTL 65 ohm driver outputs	2.40	8.2/23.0 ²	0.4	5.4
LVTTL 50 ohm driver outputs	2.40	10.3/23.0 ²	0.4	7.1
LVTTL 35 ohm driver outputs	2.40	15.3/23.0 ²	0.4	10.2
LVTTL 20 ohm driver outputs	2.40	28.7/23.0 ²	0.4	19.3

1. V_{dd330} @ 3.0V, temperature @ 100°C.
2. 23 mA is the electromigration limit for 100k power on hour (POH) @ 100°C and 100% duty cycle. This limit can be adjusted for different temperature, duty cycle and POH. Consult your IBM AE for further details.

Receiver Specifications

Table 51. 1.8V CMOS Receiver DC Voltage Specifications

Function	MAUL (V) ¹	MPUL (V)	LPUL (V)	MPDL (V)	LPDL (V)	MADL (V) ²
CMOS	V _{dd} + 0.45	V _{dd} ³	0.65*V _{dd}	0.35*V _{dd}	0.00	-0.60

1. Maximum allowable applies to overshoot only.
2. Minimum allowable applies to undershoot only.
3. V_{dd} = 1.65 to 1.95 volts.

Table 52. 2.5V CMOS Receiver DC Voltage Specifications

Function	MAUL (V) ¹	MPUL (V)	LPUL (V)	MPDL (V)	LPDL (V)	MADL (V) ²
CMOS	V _{dd250} + 0.6	V _{dd250} ³	1.7	0.70	0.00	-0.60

1. Maximum allowable applies to overshoot only.
2. Minimum allowable applies to undershoot only.
3. V_{dd250} = 2.3 to 2.7 volts.

Table 53. 3.3V Tolerant 2.5V CMOS Receiver DC Voltage Specifications

Function	MAUL (V) ¹	MPUL (V)	LPUL (V)	MPDL (V)	LPDL (V)	MADL (V) ²
CMOS	3.9	3.6	1.7	0.7	0.00	-0.6
1. Maximum allowable applies to overshoot only. 2. Minimum allowable applies to undershoot only.						

Table 54. 3.3V LVTTTL Receiver DC Voltage Specifications

Function	MAUL (V) ¹	MPUL (V)	LPUL (V)	MPDL (V)	LPDL (V)	MADL (V) ²
LVTTTL	$V_{dd330}^3 + 0.3$	V_{dd330}^3	2.00	0.80	0.00	-0.60
1. Maximum allowable applies to overshoot only. 2. Minimum allowable applies to undershoot only. 3. V_{dd330} = 3.0 to 3.6 volts.						

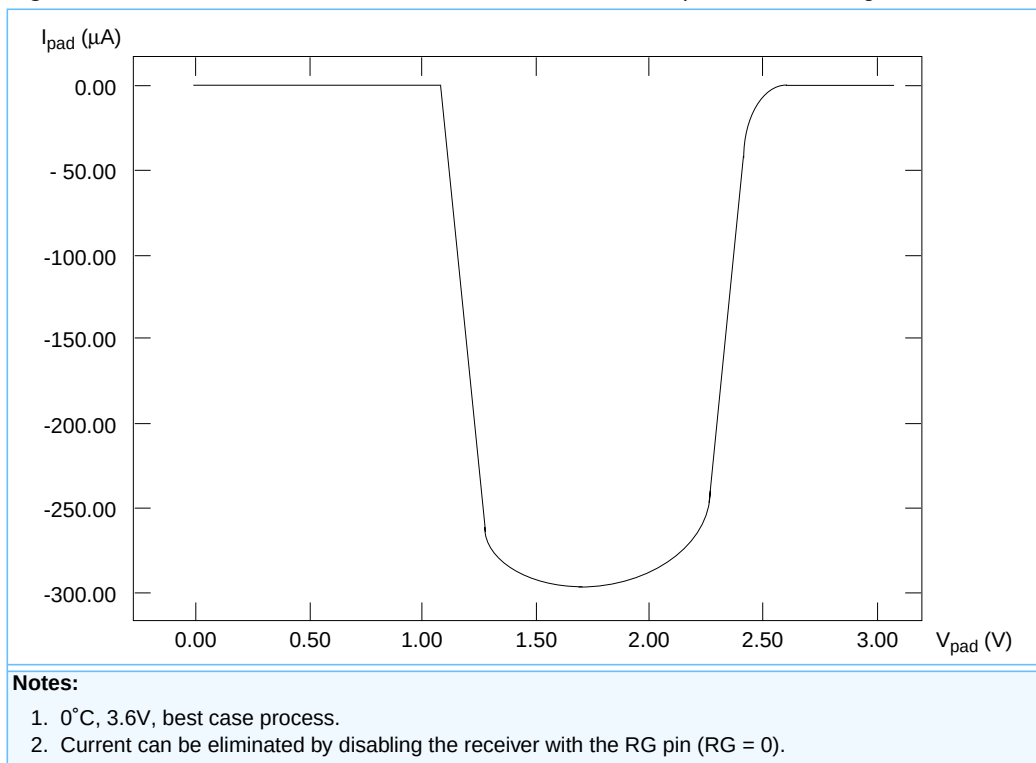
Table 55. 5.0V Tolerant 3.3V LVTTTL Receiver DC Voltage Specifications

Function	MAUL (V) ¹	MPUL (V)	LPUL (V)	MPDL (V)	LPDL (V)	MADL (V) ²
LVTTTL	5.5V	5.5V	2.00	0.80	0.00	-0.60
1. Maximum allowable applies to overshoot only 2. Minimum allowable applies to undershoot only. 3. Consult your IBM application engineer if overshoot/undershoot exceeds specifications.						

Table 56. Receiver Maximum Input Leakage DC Current Input Specifications

Function	I_{il} (μ A)	I_{ih} (μ A)
Without pull-up element or pull-down element	0 at V_{in} = LPDL	0 at V_{in} = MPUL
With pull-down element	0 at V_{in} = LPDL	200 at V_{in} = MPUL
With pull-up element	-150 at V_{in} = LPDL	0 at V_{in} = MPUL

Figure 10. 3.3V LVTTTL/5V Tolerant BP33 and IP33 Receiver Input Current/Voltage Curve



Power Supply Requirements

Table 57. I/O Voltage Requirements

Function	V_{dd}	V_{dd150}	V_{dd250}	V_{dd330}
1.8V CMOS CIO	1.8V	n/a	n/a	n/a
1.8V CMOS receiver	1.8V	n/a	n/a	n/a
2.5V CMOS CIO	1.8V	n/a	2.5V	n/a
2.5V (3.3V tolerant) receiver	1.8V	n/a	2.5V	n/a

Table 57. I/O Voltage Requirements (Continued)

Function	V _{dd}	V _{dd150}	V _{dd250}	V _{dd330}
2.5V CMOS CIO (3.3V protected)	1.8V	n/a	2.5V	n/a
3.3V LVTTTL CIO (5.0V protected)	1.8V	n/a	n/a	3.3V
3.3V LVTTTL (5.0V tolerant) receiver	1.8V	n/a	n/a	3.3V
1.8V HSTL CIO	1.8V	n/a	n/a	n/a
1.5V HSTL CIO	1.8V	1.5V	n/a	n/a
2.5V SSTL2 CIO	1.8V	n/a	2.5V	n/a
HSTL receivers	1.8V	n/a	n/a	n/a
1.5V HSTL drivers	1.8V	1.5V	n/a	n/a
LVDS receivers	1.8V	n/a	n/a	n/a
LVDS drivers	1.8V	n/a	2.5V	n/a
LVDS pseudo drivers	1.8V	n/a	n/a	n/a
PECL receivers	1.8V	n/a	2.5V	n/a
STI drivers, receivers	1.8V	n/a	n/a	n/a

Other Driver and Receiver Specifications

The following driver and receiver specification tables are provided as additional information to the data sheets for the AGP, GTL, HSTL, LVDS, PCI-X, PECL, SSTL, and STI series I/O cells.

AGP Specifications

Table 58. DC Specifications for AGP 2X Signaling

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{dd}	I/O supply voltage		1.65	1.95	V	
V_{ddq}	I/O supply voltage		3.0	3.6	V	1
V_{ih}	Input voltage high		$.5V_{ddq}$	$V_{ddq} + 0.5$	V	2
V_{il}	Input voltage low		-0.5	$.3V_{ddq}$	V	2
I_{il}	Input leakage current	$0 < V_{in} < V_{ddq}$		+/-10	μA	3
V_{oh}	Output high voltage	$I_{out} = -500 \mu A$	2.970		V	
V_{ol}	Output low voltage	$I_{out} = 1500 \mu A$		0.062	V	

Notes:

1. $V_{ddq} = V_{ddagp} = 3.3V$ (for AGP2X signaling).
2. Single-ended 3.3V LVTTTL receiver, not differential.
3. Input leakage currents include Hi-Z output leakage for all bidirectional buffers with three-state outputs.

Table 59. AC Specifications for AGP 2X Signaling

Symbol	Parameter	Condition	Min	Max	Units
$slew_r$	Output rise slew rate	$0.2V_{ddq} - 0.6V_{ddq}$	1.5	4	V/ns
$slew_f$	Output fall slew rate	$0.6V_{ddq} - 0.2V_{ddq}$	1.5	4	V/ns

Note: $V_{ddq} = V_{ddagp} = 3.3V$ (for AGP2X signaling).

Table 60. DC Specifications for AGP 4X Signaling

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{dd}	I/O supply voltage		1.65	1.95	V	
V_{ddq}	I/O supply voltage		1.4	1.6	V	1
V_{REF}	I/O reference voltage		$0.48V_{ddq}$	$0.52V_{ddq}$	V	
V_{ih}	Input voltage high		$.6V_{ddq}$	$V_{ddq} + 0.5$	V	
V_{il}	Input voltage low		-0.5	$.4V_{ddq}$	V	
I_{il}	Input leakage current	$0 < V_{in} < V_{ddq}$		+/- 10	μA	2
V_{oh}	Output high voltage	$I_{out} = -200 \mu A$	1.392		V	
V_{ol}	Output low voltage	$I_{out} = 1000 \mu A$		0.040	V	

Notes:

1. $V_{ddq} = V_{ddqpp} = 1.5V$ (for AGP4X signaling).
2. Input leakage currents include Hi-Z output leakage for all bidirectional buffers with three-state outputs.

Table 61. AC Specifications for AGP 4X Signaling

Symbol	Parameter	Condition	Min	Max	Units
I_{ol} (AC)	Switching current low	$0.15V_{ddq} < V_{out} \leq 1.0V_{ddq}$	4.37^1	44.35^1	mA
I_{oh} (AC)	Switching current high	$0.15V_{ddq} > V_{out} \geq 1.0V_{ddq}$	0^1	-39.02^1	mA
$slew_r$	Output rise slew rate	$0.2V_{ddq} - 0.6V_{ddq}$	1.4	5	V/ns
$slew_f$	Output fall slew rate	$0.6V_{ddq} - 0.2V_{ddq}$	1.4	5	V/ns

Note:

1. Only extreme values are shown for each range of V_{out} . Values are derived from the Accelerated Graphics Port Interface Specification Revision 2.0 (see specification for equations and more details).

GTL Specifications

Table 62. GTL DC Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{dd}	Device supply voltage	1.65	1.8	1.95	V	
V_{TT}	Termination voltage	1.14	1.2	1.26	V	JEDEC GTL
		1.35	1.5	1.65	V	GTL+
V_{REF}	Differential input reference voltage	$2/3 V_{TT} - 2\%$	0.8	$2/3 V_{TT} + 2\%$	V	JEDEC GTL
		$2/3 V_{TT} - 2\%$	1.0	$2/3 V_{TT} + 2\%$	V	GTL+
V_{oh}	Output high voltage	$V_{TT} - 0.5 \text{ mV}$			V	$I_{oh} < 10 \mu\text{A}$
V_{ol}	Output low voltage			0.45	V	$I_{ol}^1 = 48 \text{ mA}$ @0.4V
V_{ih}	Input high voltage	$V_{REF} + 0.05$		$V_{dd} + 0.45$	V	
V_{il}	Input low voltage	-0.6		$V_{REF} - 0.05$	V	
I_{oz}	3-state leakage current	0		10	μA	Driver Hi-Z

1. For double 50 ohm terminations only. $I_{ol} = 24 \text{ mA}$ for single 50 ohm termination.

Design Notes:

1. All GTL specifications are consistent with EIA/JEDEC Standard, JESD8-3 "Gunning Transceivers Logic (GTL): Low-Level, High-Speed Interface Standard for Digital Integrated Circuits," dated 11/93.
2. Di/dt and performance are chosen by performance level selection (A and B).
 - a. Performance level A targeted to run at 150 MHz (300 Mb/s) or faster depending on loading conditions. Di/dt is comparable to 65 mA/ns LVTTTL driver.
 - b. Performance level B targeted to run at 200 MHz (400 Mb/s) or faster depending on loading conditions. Di/dt is comparable to 105 mA/ns LVTTTL driver.
3. The differential input reference supply (V_{REF}) is brought on chip through VGTLR1 and VGTLR2 I/O cells.
4. Termination voltage (V_{TT}) is generated off-chip.
5. The 48 mA GTL driver is rated at 48 mA @ 100°C and 50% duty cycle for 100k power on hours (POH).

HSTL Specifications

Table 63. 1.8V HSTL DC Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{dd}	Device supply voltage	1.65	1.8	1.95	V	
V_{ddq}	Output supply voltage	1.65	1.8	1.95	V	
V_{TT}	Termination voltage	0.825	0.9	0.975	V	$V_{ddq}/2$
V_{REF}	Differential input reference voltage	0.825	0.9	0.975	V	$V_{ddq}/2$
V_{oh}	Output high voltage	$V_{ddq} - 0.4$			V	$I_{oh} = 8 \text{ mA @ } 1.25\text{V Class I}$ $I_{oh} = 16 \text{ mA @ } 1.25\text{V Class II}$
V_{ol}	Output low voltage			0.4	V	$I_{ol} = 8 \text{ mA @ } 0.4\text{V Class I}$ $I_{ol} = 16 \text{ mA @ } 0.4\text{V Class II}$
V_{ih}	Input high voltage	$V_{REF} + 0.1$		$V_{dd} + 0.3$	V	
V_{il}	Input low voltage	-0.3		$V_{REF} - 0.1$	V	
I_{oz}	3-state leakage current	0		10	μA	Driver Hi-Z

Design Notes:

- All HSTL specifications are consistent with the EIA/JEDEC specification except for the value of V_{ddq} , which is 1.8V instead of 1.5V.
- Two 1.8 V HSTL performance levels are offered:
 - Performance level A is targeted to run up to 350 MHz (700 Mb/second) depending on loading conditions. Maximum di/dt is comparable to 150 mA/ns 2.5V/3.3V LVTTTL drivers for Class II operation and 75 mA/ns for Class I operation.
 - Performance level B is targeted to run up to 450 MHz (900 Mb/second) depending on loading conditions. Di/dt is comparable to 150 mA/ns 2.5V/3.3V LVTTTL drivers for Class II operation and 125 mA/ns for Class I operation.
- The differential input reference supply (V_{REF}) is brought on chip through the VHSTL18R1 and VHSTL18R2 cells. The termination voltage (V_{TT}) is generated off chip.
- The 1.8V HSTL Class I driver is rated at 8 mA at 100°C and 100% duty cycle for 100k power on hours. The Class II driver is rated at 16 mA at 100°C and 100% duty cycle for 100k power on hours.

Table 64. 1.5V HSTL DC Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{dd}	Device supply voltage	1.65	1.8	1.95	V	
V_{ddq}	Output supply voltage	1.4	1.5	1.6	V	
V_{TT}	Termination voltage	0.68	0.75	0.9	V	$V_{ddq}/2$
V_{REF}	Differential input reference voltage	0.68	0.75	0.9	V	$V_{ddq}/2$
V_{oh}	Output high voltage	$V_{ddq} - 0.4$			V	$I_{oh} = 8 \text{ mA @ } 1.25\text{V Class I}$ $I_{oh} = 16 \text{ mA @ } 1.25\text{V Class II}$
V_{ol}	Output low voltage			0.4	V	$I_{ol} = 8 \text{ mA @ } 0.4\text{V Class I}$ $I_{ol} = 16 \text{ mA @ } 0.4\text{V Class II}$
V_{ih}	Input high voltage	$V_{REF} + 0.1$		$V_{dd} + 0.3$	V	
V_{il}	Input low voltage	-0.3		$V_{REF} - 0.1$	V	
I_{oz}	3-state leakage current	0		10	μA	Driver Hi-Z

Design Notes:

1. All HSTL specifications are consistent with the EIA/JEDEC specification.
2. The differential input reference supply (V_{REF}) is brought on chip through the VHSTLR1 and VHSTLR2 cells. The termination voltage (V_{TT}) is generated off chip.

LVDS Specifications

Table 65. LVDS Receiver DC Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{dd}	Device supply voltage	1.65	1.8	1.95	V	Receiver uses only V_{dd} supply
Temp	Temperature range	0	50	100	°C	
Rec Pwr	Input buffer power			9.3	mW	Including on-chip terminator $V_{PAD} - V_{PADN} = 0.4V$
V_{ih}	Receiver input voltage			$V_{dd} + 0.20$	V	Receiver ESD connected to V_{dd}
V_{il}	Receiver input voltage	-0.20			V	
$V_{ih} - V_{il}$	Receiver input voltage range	100			mV	@600 MHz
V_{icm}	Receiver common mode range	0	1.25	V_{dd}	V	

Design Notes:

1. All DC characteristics are based on power supply and temperature ranges as specified above.
2. LVDS design reference: IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), IEEE Standard 1596.3,1996.
3. Maximum frequency is load and package dependent. Operation at 600 MHz (1.2 Gb/second) is achievable with a minimum of 100 mV input swing over the wide common range as specified. The customer is responsible for determining optimal frequency and switching capabilities through thorough simulation and analysis.

Table 66. LVDS Driver DC Specifications: OLVD5_A

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{dd}	Device supply voltage	1.65	1.8	1.95	V	Receiver uses only V_{dd} supply
V_{dd250}	Device supply voltage	2.3	2.5	2.7	V	Buffer uses both V_{dd} and V_{dd250}
Temp	Temperature range	0	50	100	°C	Functional at 125°C with significant EM degradation
V_{oh}	Output voltage high	1.286	1.406	1.525	V	On-chip 100 Ω termination
V_{ol}	Output voltage low	0.908	0.984	1.06	V	On-chip 100 Ω termination
$ V_{od} $	Output differential voltage	363	421	480	mV	$V_{oh} - V_{ol}$
V_{os}	Output offset voltage	1.10	1.2	1.292	V	$(V_{oh} - V_{ol})/2$
R_o	Output impedance, single-ended	75		117	Ω	
ΔR_o	R_o mismatch between differential outputs PAD and PADN			10	%	
I_{load}	Terminator current	3.20	4.36	6.00	mA	On-chip termination
Drv Pwr	Output buffer power			25.8	mW	Excluding on-chip terminator
Drv Pwr (Hi-Z mode)	Output buffer power in Hi-Z mode			0.4	mW	

Design Notes:

1. All DC characteristics are based on power supply and temperature ranges as specified above and using on-chip 100 Ω terminator with approximately $\pm 20\%$ tolerance over supply and temperature.
2. LVDS design reference: IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), IEEE Standard 1596.3,1996.
3. Maximum frequency is load and package dependent. Operation at 622 MHz (1.25 Gb/s) and beyond is achievable over a reasonable length of PCB or cable. The customer is responsible for determining optimal frequency and switching capabilities through thorough simulation and analysis using appropriate package and transmission line models.

Table 67. LVDS Driver DC Specifications: OLVD5_B

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{dd}	Device supply voltage	1.65	1.8	1.95	V	Receiver uses only V_{dd} supply
V_{dd250}	Device supply voltage	2.3	2.5	2.7	V	Buffer uses both V_{dd} and V_{dd250}
Temp	Temperature range	0	50	100	°C	Functional at 125°C with significant EM degradation
V_{oh}	Output voltage high	1.29	1.4	1.51	V	On-chip 100 Ω termination at receiver
V_{ol}	Output voltage low	0.95	1.02	1.09	V	On-chip 100 Ω termination at receiver
$ V_{od} $	Output differential voltage	330	384	446	mV	$V_{oh} - V_{ol}$
V_{os}	Output offset voltage	1.12	1.21	1.3	V	$(V_{oh} - V_{ol})/2$
R_o	Output impedance, single-ended	31		54	Ω	
ΔR_o	R_o mismatch between differential outputs PAD and PADN			10	%	
I_{load}	Terminator current	3.20	4.36	5.60	mA	On-chip 100 Ω termination at receiver
Drv Pwr	Output buffer power			36.4	mW	Excluding on-chip terminator at receiver
Drv Pwr (Hi-Z mode)	Output buffer power in Hi-Z mode			0.4	mW	

Design Notes:

1. All DC characteristics are based on power supply and temperature ranges as specified above and using on-chip 100 Ω terminator with approximately $\pm 20\%$ tolerance over process, voltage, and temperature ranges.
2. LVDS design reference: IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), IEEE Standard 1596.3,1996.
3. Driver as built-in 100 Ω between PAD and PADN.
4. Maximum frequency is load and package dependent. Operation at 1.25 GHz (2.5 Gb/s) and beyond is achievable over a reasonable length of PCB or cable. The customer is responsible for determining optimal frequency and switching capabilities through thorough simulation and analysis using appropriate package and transmission line models.

Table 68. LVDS Driver DC Specifications: OPLVDS_A

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{dd}	Device supply voltage	1.65	1.8	1.95	V	Single power supply
Temp	Temperature range	0	50	100	°C	Functional at 125°C with significant EM degradation
V_{oh}	Output voltage high	1.478	1.611	1.745	V	On-chip 100 Ω termination at the receiver input
V_{ol}	Output voltage low	0.767	0.772	0.774	V	On-chip 100 Ω termination at the receiver input
$ V_{od} $	Output differential voltage	711	839	971	mV	$V_{oh} - V_{ol}$
V_{os}	Output offset voltage	1.12	1.29	1.26	V	$(V_{oh} - V_{ol})/2$
R_o	Output impedance, single-ended	15	20	26	Ω	
ΔR_o	R_o mismatch between differential outputs PAD and PADN			10	%	
I_{load}	Terminator current	6.37	8.69	11.19	mA	On-chip 100 Ω termination
Drv Pwr	Output buffer power			14.3	mW	Excluding on-chip termination at the receiver input
Drv Pwr (Hi-Z mode)	Output buffer power in Hi-Z mode			0.01	mW	

Design Notes:

1. All DC characteristics are based on power supply and temperature ranges as specified above and using on-chip 100 Ω terminator at the receiver input with approximately $\pm 20\%$ tolerance over power supply voltage and temperature.
2. The operation of the pseudo LVDS driver is similar to the standard IEEE LVDS driver with the following exception: the pseudo LVDS driver has a much larger output voltage swing.
3. Maximum frequency is load and package dependent. Operation at 1.5 GHz is achievable over a reasonable length of PCB or cable. The customer is responsible for determining optimal frequency and switching capabilities through thorough simulation and analysis using appropriate package and transmission line models.

PCI-X Specifications

DC Specifications

Table 69 shows the DC specifications for devices operating in PCI-X mode. Conventional 3.3V signaling DC specifications are included for reference.

Table 69. DC Specifications for PCI-X Devices

Symbol	Parameter	Condition	PCI-X		3.3V Conventional PCI (reference)		Units
			Min	Max	Min	Max	
V_{dd}	Supply voltage		3.0	3.6	3.0	3.6	V
V_{ih}	Input high voltage		$0.5 \cdot V_{dd}$	$V_{dd} + 0.5$	$0.5 \cdot V_{dd}$	$V_{dd} + 0.5$	V
V_{il}	Input low voltage		-0.5	$0.35 \cdot V_{dd}$	-0.5	$0.3 \cdot V_{dd}$	V
V_{ipu}^1	Input pull-up voltage		$0.7 \cdot V_{dd}$		$0.7 \cdot V_{dd}$		V
V_{oh}	Output high voltage	$I_{out} = -500 \mu A$	$0.9 \cdot V_{dd}$		$0.9 \cdot V_{dd}$		V
V_{ol}	Output low voltage	$I_{out} = 1500 \mu A$		$0.1 \cdot V_{dd}$		$0.1 \cdot V_{dd}$	V
C_{in}	Input pin capacitance			8		10	pF

1. This specification should be assured by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization must assure that the input buffer is conducting minimum current at this input voltage.

AC Specifications

The output drive characteristics for devices operating in PCI-X mode over the full range of output voltages are shown in Table 70 and Table 71 on page 131. Conventional PCI 66 MHz clock values are included for reference. For clarity, AC output characteristic equations define lines that pass through the origin. Actual device requirements when the output voltage is above V_{oh} or below V_{ol} are specified in the DC characteristics (Table 69 on page 128). As in conventional PCI devices, the DC characteristics are the only conditions under which steady-state operation is intended. The higher current por-

tions of the AC characteristics are intended to be reached only during switching transients.

Table 70. AC Specifications for PCI-X Devices

Symbol	Parameter	Condition	Min	Max	Units
Output Buffer Drive Currents					
I _{oh} (AC)	Switching current high	0 < V _{dd} - V _{out} ≤ 3.6 V		-74*(V _{dd} - V _{out})	mA
		0 < V _{dd} - V _{out} ≤ 1.2 V	-32*(V _{dd} - V _{out})		mA
		1.2 V < V _{dd} - V _{out} ≤ 1.9 V	-11*(V _{dd} - V _{out}) - 25.2		mA
		1.9 V < V _{dd} - V _{out} ≤ 3.6 V	-1.8*(V _{dd} - V _{out}) - 42.7		mA
I _{ol} (AC)	Switching current low	0 ≤ V _{out} ≤ 3.6 V		100*V _{out}	mA
		0 < V _{out} ≤ 1.3 V	48*V _{out}		mA
		1.3 V < V _{out} ≤ 3.6 V	5.7*V _{out} + 55		mA
Clamp Currents					
I _{cl}	Low clamp current	-3 V < V _{in} ≤ -0.8875 V	-40 + (V _{in} + 1)/0.005		mA
		-0.8875 V < V _{in} ≤ -0.625 V	-25 + (V _{in} + 1)/0.0015		mA
I _{ch}	High clamp current	0.8875 V ≤ V _{in} - V _{dd} < 4 V	40 + (V _{in} - V _{dd} - 1)/0.005		mA
		0.625 V ≤ V _{in} - V _{dd} < 0.8875 V	25 + (V _{in} - V _{dd} - 1)/0.015		mA

Output drive current limits from Table 70 are illustrated in Figure 11 and Figure 12 on page 130, with the axes the same as those shown in the PCI Local Bus specification, revision 2.2. Conventional PCI 33 MHz clock 3.3V limits are included for reference.

Figure 11. PCI-X Pull-Up Output Buffer V/I Curves

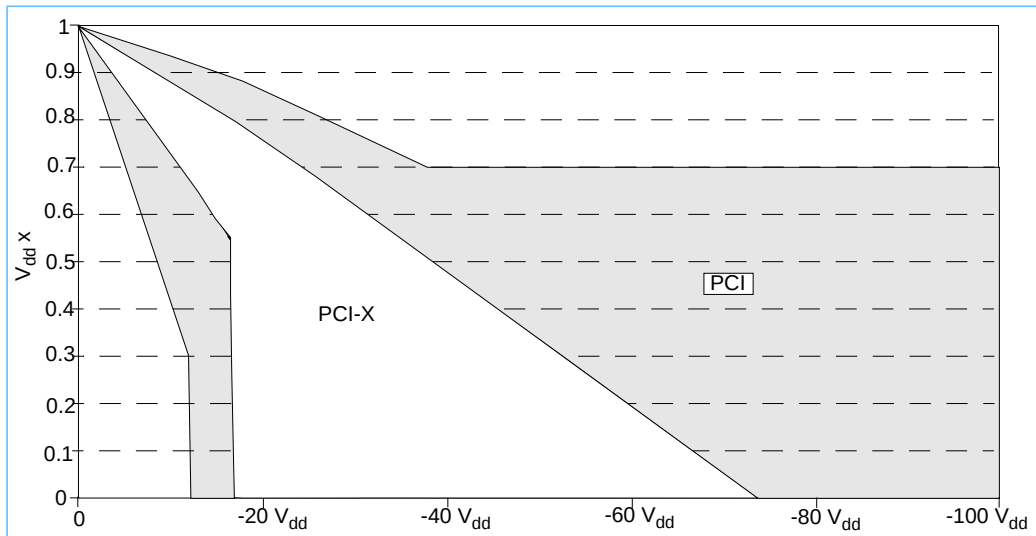
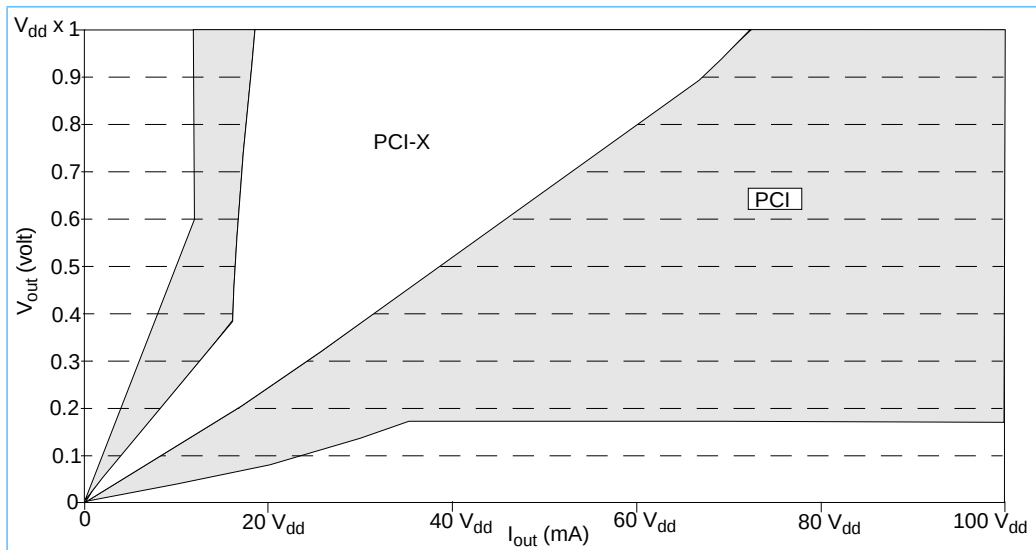


Figure 12. PCI-X Pull-Down Output Buffer V/I Curves



Electrical Specifications

Table 71. PCI-X Output Slew Rates

Symbol	Parameter	Condition	PCI-X		Conventional PCI 66 MHz (reference)		Units
			Min	Max	Min	Max	
t_r	Output rise slew rate	$0.3 \cdot V_{dd}$ to $0.6 \cdot V_{dd}$	1	6	1	4	V/ns
t_f	Output fall slew rate	$0.6 \cdot V_{dd}$ to $0.3 \cdot V_{dd}$	1	6	1	4	V/ns

Timing Specifications

Clock measurement conditions are the same for PCI-X devices as for conventional PCI devices in a 3.3V signaling environment except for voltage levels specified in Table 69 on page 128.

Figure 13. PCI-X 3.3V Clock Waveform

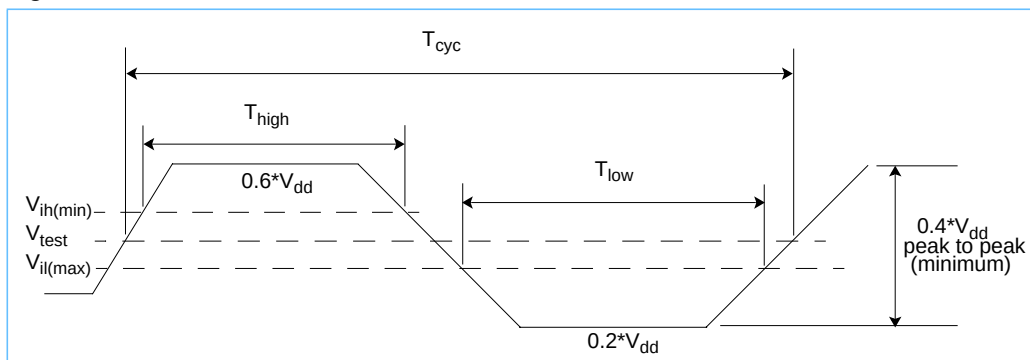


Table 72. PCI-X Clock Specifications

Symbol	Parameter	PCI-X 133 MHz 3V		PCI-X 66 MHz 3V		Conventional PCI 66 MHz (reference) 3V/5V		Conventional PCI 33 MHz (reference) 3V/5V		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
T _{cyc}	CLK cycle time	7.5	20	15	20	15	30	30	∞	ns
T _{high}	CLK high time	3		6		6		11		ns
T _{low}	CLK low time	3		6		6		11		ns
	CLK slew rate	1.5	4	1.5	4	1.5	4	1	4	V/ns

Table 73 shows the timing specifications for all signals other than the clock.

Table 73. PCI-X General Timing Parameters

Symbol	Parameter	PCI-X 133 MHz		PCI-X 66 MHz		Conventional PCI 66 MHz (reference)		Conventional PCI 33 MHz (reference)		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
T _{val}	CLK to signal valid delay (bused signals)	0.7	3.8	0.7	3.8	2	6	2	11	ns	1, 4, 5
T _{val(ptp)}	CLK to signal valid delay (point-to-point signals)	0.7	3.8	0.7	3.8	2	6	2	12	ns	1, 4, 5

Notes:

1. Minimum times are measured at the package pin, not the test point.
2. For purposes of active/float timing measurements, the Hi-Z of the "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
3. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
4. A PCI-X device is permitted to have the minimum values shown for T_{val}, T_{val(ptp)}, and T_{on} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in the PCI Local Bus Specification, revision 2.2, for the appropriate clock frequency.
5. The device must meet this specification independent of the number of outputs switching simultaneously.



Table 73. PCI-X General Timing Parameters (Continued)

Symbol	Parameter	PCI-X 133 MHz		PCI-X 66 MHz		Conventional PCI 66 MHz (reference)		Conventional PCI 33 MHz (reference)		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
T_{on}	Float to active delay	0		0		2		2		ns	2, 4, 5
T_{off}	Active to float delay		7		7		14		28	ns	3, 5
T_{su}	Input set up time to CLK (bused signals)	1.2		1.2		3		7		ns	3
$T_{su(ptp)}$	Input set up time to CLK (point-to-point signals)	1.2		1.2		5		10, 12		ns	
T_h	Input hold time from CLK	0.5		0.5		0		0		ns	
$T_{rst-off}$	Reset active to out- put float delay		40		40		40		40	ns	

Notes:

1. Minimum times are measured at the package pin, not the test point.
2. For purposes of active/float timing measurements, the Hi-Z of the "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
3. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
4. A PCI-X device is permitted to have the minimum values shown for T_{val} , $T_{val(ptp)}$, and T_{on} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in the PCI Local Bus Specification, revision 2.2, for the appropriate clock frequency.
5. The device must meet this specification independent of the number of outputs switching simultaneously.

PECL Specifications

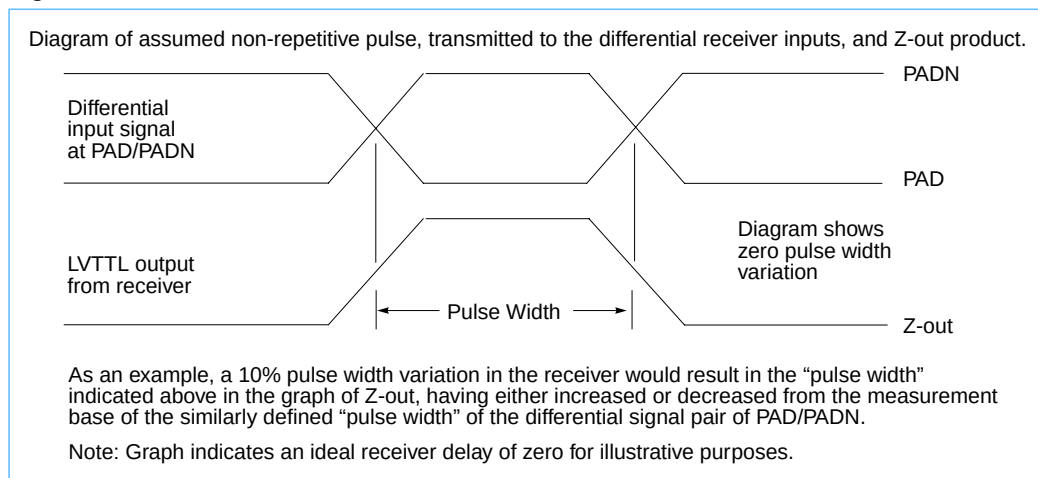
Table 74. PECL Receiver Specifications

Parameter	Value	Comments
200 MHz Operation		
Receiver common mode voltage level range, or V-crosspoint, at 200 MHz	0.55V to 2.35V	The average differential voltage with respect to receiver ground.
Receiver input differential voltage swing minimum	0.25V ¹	Absolute minimum input swing, allows for signal attenuation between the driver and receiver.
Absolute maximum pulse width shrinkage	10%	Pulse width variation from nominal with 0.25V swing at receiver input.
400 MHz Operation		
Receiver common mode voltage level range, or V-crosspoint, at 400 MHz	0.7V to 2.15V	The average differential voltage with respect to receiver ground.
Receiver input differential voltage swing minimum	0.25V ¹	Absolute minimum input swing, allows for signal attenuation between the driver and receiver.
Absolute maximum pulse width shrinkage	10%	Pulse width variation from nominal with 0.25V swing at receiver input.
600 MHz Operation³		
Receiver common mode voltage level range, or V-crosspoint, at 600 MHz ³	0.9V to 2.1V	The average differential voltage with respect to receiver ground.
Receiver input differential voltage swing minimum	0.25V ¹	Absolute minimum input swing, allows for signal attenuation between the driver and receiver.
Absolute maximum pulse width shrinkage	10%	Pulse width variation from nominal with 0.25V swing at receiver input.
1. Allows for pad transfer, package, and board drops. On-chip pad transfer resistances can reach 5.0 Ω. 2. Alternate termination schemes are suggested when using unterminated IPECL. 3. At operating frequencies greater than 500 MHz, skin effect and various other high frequency interconnect elements are crucial application considerations. 4. Specifications are based on analysis performed from 0°C to 100°C		

Table 74. PECL Receiver Specifications (Continued)

Parameter	Value	Comments
800 MHz Operation³		
Receiver common mode voltage level range, or V-crosspoint, at 800 MHz ³	1.2V to 2.0V	The average differential voltage with respect to receiver ground.
Receiver input differential voltage swing minimum	0.25V ¹	Absolute minimum input swing, allows for signal attenuation between the driver and receiver.
Absolute maximum pulse width shrinkage	10%	Pulse width variation from nominal with 0.5V swing at receiver input.
1000 MHz Operation³		
Receiver common mode voltage level range, or V-crosspoint, at 1000 MHz ³	1.5V to 1.95V	The average differential voltage with respect to receiver ground.
Receiver input differential voltage swing minimum	0.25V ¹	Absolute minimum input swing, allows for signal attenuation between the driver and receiver.
Absolute maximum pulse width shrinkage	10%	Pulse width variation from nominal with 0.5V swing at receiver input.
Receiver Impedance		
Receiver input impedance, IPECLD	100 $\Omega \pm 20 \Omega$	Line to line receiver termination. ²
Transmission line AC impedance	100 Ω line to line	Equivalent to 50 Ω to ground on each line.
Receiver Jitter Characteristics		
Cycle to cycle jitter	<10 ps	Absolute maximum cycle to cycle edge variation.
Power supply produced jitter	10 ps/100 mV	Absolute maximum jitter due to V _{dd} fluctuations.
1. Allows for pad transfer, package, and board drops. On-chip pad transfer resistances can reach 5.0 Ω. 2. Alternate termination schemes are suggested when using unterminated IPECL. 3. At operating frequencies greater than 500 MHz, skin effect and various other high frequency interconnect elements are crucial application considerations. 4. Specifications are based on analysis performed from 0°C to 100°C		

Figure 14. PECL Receiver Pulse Width Variation Definition



SSTL Specifications

Table 75. SSTL2 DC Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{dd}	Device supply voltage	1.65	1.8	1.95	V	
V_{ddq}	Output supply voltage	2.3	2.5	2.7	V	$V_{ddq} = V_{dd250}$
V_{TT}	Termination voltage	1.11 - 1.19	1.25	1.31 - 1.39	V	$0.5 \cdot V_{ddq}$

Design Notes:

- All SSTL2 specifications are consistent with JEDEC committee re-ballot (JC-16-97-58A), 10/14/97.
- Di/dt and performance are chosen by performance level selection (A and B).
 - Performance level A is targeted to run at 200 MHz or faster depending on loading conditions. Di/dt is comparable to 110 mA/ns 2.5V/3.3V LVTTL driver.
 - Performance level B is targeted to run at 250 MHz or faster depending on loading conditions. Di/dt is comparable to 150 mA/ns 2.5V/3.3V LVTTL driver.
- The differential input reference supply (V_{REF}) is brought on chip through VSSTL2R1 and VSSTL2R2 I/O cells.
- Termination voltage (V_{TT}) is generated off chip.
- SSTL2 driver is rated at 20 mA @100°C and 50% duty cycle for 100k power on hours (POH).



Table 75. SSTL2 DC Specifications (Continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{REF}	Differential input reference voltage	1.15	1.25	1.35	V	$0.5 \cdot V_{ddq}$
V_{oh} (Class II)	Output high voltage	1.95			V	$I_{oh} = 15.2 \text{ mA @ } 1.95\text{V}$
V_{ol} (Class II)	Output low voltage			0.55	V	$I_{ol} = 15.2 \text{ mA @ } 0.55\text{V}$
$R_{oh \text{ max}}$ (Class II)	Max pull-up impedance			36.2	ohm	
$R_{ol \text{ max}}$ (Class II)	Max pull-down impedance			36.2	ohm	
V_{ih}	Input high voltage	$V_{REF} + 0.18$		$V_{ddq} + 0.3$	V	
V_{il}	Input low voltage	-0.3		$V_{REF} - 0.18$	V	
I_{oz}	3-state leakage current	0		10	μA	Driver Hi-Z
Temp	Temperature	0	50	100	$^{\circ}\text{C}$	

Design Notes:

1. All SSTL2 specifications are consistent with JEDEC committee re-ballot (JC-16-97-58A), 10/14/97.
2. Di/dt and performance are chosen by performance level selection (A and B).
 - a. Performance level A is targeted to run at 200 MHz or faster depending on loading conditions. Di/dt is comparable to 110 mA/ns 2.5V/3.3V LVTTL driver.
 - b. Performance level B is targeted to run at 250 MHz or faster depending on loading conditions. Di/dt is comparable to 150 mA/ns 2.5V/3.3V LVTTL driver.
3. The differential input reference supply (V_{REF}) is brought on chip through VSSTL2R1 and VSSTL2R2 I/O cells.
4. Termination voltage (V_{TT}) is generated off chip.
5. SSTL2 driver is rated at 20 mA @100 $^{\circ}\text{C}$ and 50% duty cycle for 100k power on hours (POH).

STI Specifications

Table 76. STI Receiver Specifications¹

Parameter	Value	Comments
400 MHz Operation		
Receiver input differential voltage swing minimum	0.4V ²	Absolute minimum input swing, allows for signal attenuation between the driver and receiver.
Receiver common mode voltage level range, or V-crosspoint, at 400 MHz	-0.3V ^{3,4} to 2.7V	The average differential voltage with respect to receiver ground.
Absolute maximum pulse width variation.	10%	Pulse width variation from nominal, with 0.4V swing at receiver input.
600 MHz Operation⁵		
Receiver common mode voltage level range, or V-crosspoint, at 600 MHz	-0.2V ^{3,4} to 2.35V	The average differential voltage with respect to receiver ground.
Receiver input differential voltage swing minimum	0.4V ²	Absolute minimum input swing, allows for signal attenuation between the driver and receiver.
Absolute maximum pulse width variation.	10%	Pulse width variation from nominal, with 0.4V swing at receiver input.
800 MHz Operation⁵		
Receiver common mode voltage level range, or V-crosspoint, at 800 MHz	-0.1V ^{3,4} to 2.2V	The average differential voltage with respect to receiver ground.
Receiver input differential voltage swing minimum	0.4V ²	Absolute minimum input swing, allows for signal attenuation between the driver and receiver.
Absolute maximum pulse width variation.	10%	Pulse width variation from nominal, with 0.4V swing at receiver input.
- Specifications are based on analysis performed from 0°C to 100°C. - Allows for pad transfer, package, and board drops. On-chip pad transfer resistances can reach 10.0 Ω. - The receiver's optimal performance, with minimum skew, is obtained at a common mode level of 1.05V. - Common mode voltage range is clamped below these level, by the ESD devices at the PAD/PADN input connections, to a level of one diode drop beyond the V_{dd} and GND supplies. - At operating frequencies greater than 500 MHz, skin effect and various other high frequency interconnect elements are significant application considerations. - Alternate termination schemes are suggested when using unterminated STI.		

Table 76. STI Receiver Specifications¹ (Continued)

Parameter	Value	Comments
1000 MHz Operation⁵		
Receiver common mode voltage level range, or V-crosspoint, at 1000 MHz	1.05V ³ to 1.20V	The average differential voltage with respect to receiver ground.
Receiver input differential voltage swing minimum	0.4V ²	Absolute minimum input swing, allows for signal attenuation between the driver and receiver.
Absolute maximum pulse width variation.	10%	Pulse width variation from nominal, with 0.4V swing at receiver input.
Receiver Impedance		
Receiver input impedance, ISTI18D	100Ω ± 20Ω	Line to line receiver termination. ⁶
Transmission line AC impedance	100Ω line to line	Equivalent to 50Ω to ground on each line.
Receiver Jitter Characteristics		
Cycle to cycle jitter	<10 ps	Absolute maximum cycle to cycle edge variation.
Power supply produced jitter	10 ps/100 mV	Absolute maximum jitter due to V _{dd} fluctuations.
- Specifications are based on analysis performed from 0°C to 100°C. - Allows for pad transfer, package, and board drops. On-chip pad transfer resistances can reach 10.0 Ω. - The receiver's optimal performance, with minimum skew, is obtained at a common mode level of 1.05V. - Common mode voltage range is clamped below these level, by the ESD devices at the PAD/PADN input connections, to a level of one diode drop beyond the V_{dd} and GND supplies. - At operating frequencies greater than 500 MHz, skin effect and various other high frequency interconnect elements are significant application considerations. - Alternate termination schemes are suggested when using unterminated STI.		

Figure 15. STI Receiver Pulse Width Variation Definition

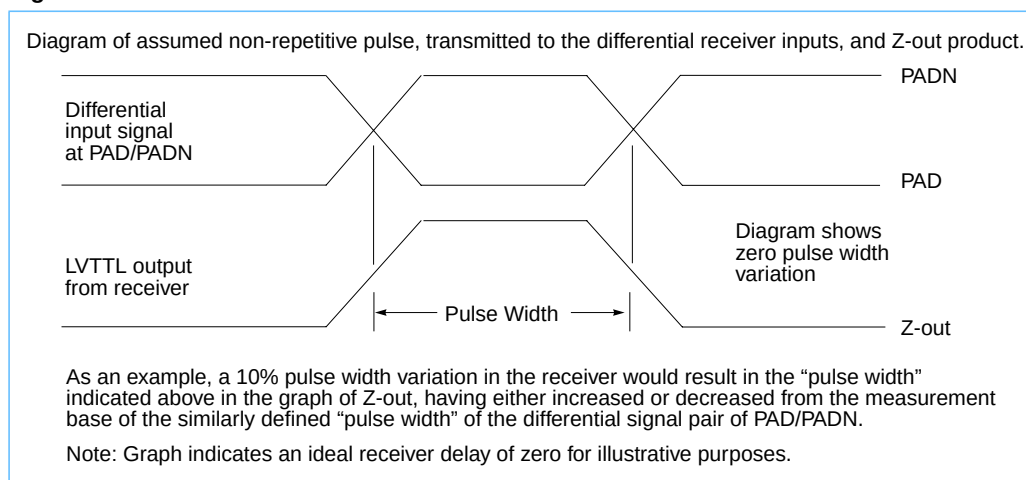


Table 77. STI Driver Specifications¹

Parameter	Value	Comments
Driver frequency range of operation	800 MHz ²	Maximum driver operation frequency.
Driver output common mode voltage	1.15V $\pm$ 0.1V	The average differential voltage.
Driver output differential voltage swing	1.0V $\pm$ 0.15V	Minimum and maximum differential voltage swing around the common mode voltage.
Maximum output slew rate dv/dt	7.5 V/ns	10% to 90% change in V/ns of either differential output.
Maximum output signal level variation	$\pm$ 15 mV	Level change of PAD or PADN versus the frequency of operation.

Notes:

1. Specifications are based on analysis performed from 0°C to 100°C.
2. At operating frequencies greater than 500 MHz, skin effect, and various other high frequency interconnect elements are significant application considerations.
3. Common mode voltage range and differential voltage swing are independent variables.

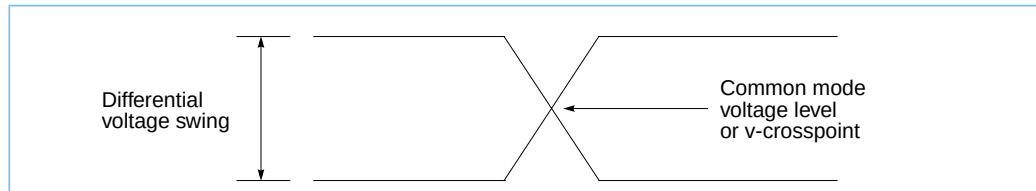
Table 77. STI Driver Specifications¹ (Continued)

Parameter	Value	Comments
Driver impedance	15 ohms $\pm$ 5 ohms	DC impedance of the driver.
Driver output differential skew	$\pm$ 25 ps	Maximum skew of the differential signal's crosspoints, or zero differential voltage, versus the input signal's transitional pass through the threshold measurement point.

Notes:

1. Specifications are based on analysis performed from 0°C to 100°C.
2. At operating frequencies greater than 500 MHz, skin effect, and various other high frequency interconnect elements are significant application considerations.
3. Common mode voltage range and differential voltage swing are independent variables.

Figure 16. STI Driver/Receiver Signal Level Definition



Notes:

1. Specifications are based on analysis performed from 0°C to 100°C.
2. At operating frequencies greater than 500 MHz, skin effect, and various other high frequency interconnect elements are significant application considerations.
3. Common mode voltage range and differential voltage swing are independent variables.

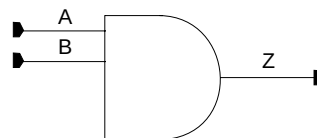


Gate Array Primitive Logic

Cell: AND2_G

Function: 2-Way AND

Boolean Expression: $Z = A \bullet B$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.125 + 0.011N _{std}	0.082 + 0.008N _{std}	0.059 + 0.006N _{std}
		t _{PHL}	0.118 + 0.008N _{std}	0.087 + 0.005N _{std}	0.066 + 0.004N _{std}
B-Z		t _{PLH}	0.124 + 0.011N _{std}	0.080 + 0.008N _{std}	0.056 + 0.006N _{std}
		t _{PHL}	0.130 + 0.008N _{std}	0.096 + 0.005N _{std}	0.074 + 0.004N _{std}
A-Z	H	t _{PLH}	0.114 + 0.006N _{std}	0.074 + 0.004N _{std}	0.053 + 0.003N _{std}
		t _{PHL}	0.107 + 0.004N _{std}	0.080 + 0.003N _{std}	0.061 + 0.002N _{std}
B-Z		t _{PLH}	0.116 + 0.006N _{std}	0.073 + 0.004N _{std}	0.050 + 0.003N _{std}
		t _{PHL}	0.125 + 0.004N _{std}	0.093 + 0.003N _{std}	0.072 + 0.002N _{std}
A-Z	J	t _{PLH}	0.135 + 0.003N _{std}	0.089 + 0.002N _{std}	0.063 + 0.001N _{std}
		t _{PHL}	0.128 + 0.002N _{std}	0.096 + 0.001N _{std}	0.072 + 0.001N _{std}
B-Z		t _{PLH}	0.133 + 0.003N _{std}	0.085 + 0.002N _{std}	0.059 + 0.001N _{std}
		t _{PHL}	0.141 + 0.002N _{std}	0.105 + 0.001N _{std}	0.080 + 0.001N _{std}
A-Z	L	t _{PLH}	0.158 + 0.002N _{std}	0.104 + 0.001N _{std}	0.074 + 0.001N _{std}
		t _{PHL}	0.149 + 0.001N _{std}	0.110 + 0.001N _{std}	0.083 + 0.001N _{std}
B-Z		t _{PLH}	0.155 + 0.002N _{std}	0.099 + 0.001N _{std}	0.069 + 0.001N _{std}
		t _{PHL}	0.161 + 0.001N _{std}	0.119 + 0.001N _{std}	0.090 + 0.001N _{std}

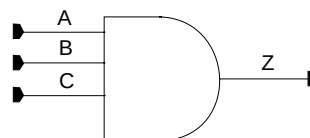
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level			
	E	H	J	L
A	0.974	1.916	1.931	1.930
B	0.980	1.946	2.065	2.061
Internal	5.165	9.124	12.111	15.373
Cell Units	9 cells	15 cells	15 cells	18 cells

Cell: AND3_G

Function: 3-Way AND

Boolean Expression: $Z = A \bullet B \bullet C$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.176 + 0.011N _{std}	0.113 + 0.008N _{std}	0.080 + 0.006N _{std}
		t _{PHL}	0.133 + 0.008N _{std}	0.097 + 0.005N _{std}	0.073 + 0.004N _{std}
C-Z		t _{PLH}	0.180 + 0.011N _{std}	0.110 + 0.008N _{std}	0.075 + 0.006N _{std}
		t _{PHL}	0.154 + 0.008N _{std}	0.113 + 0.005N _{std}	0.086 + 0.004N _{std}
A-Z	H	t _{PLH}	0.202 + 0.006N _{std}	0.130 + 0.004N _{std}	0.092 + 0.003N _{std}
		t _{PHL}	0.152 + 0.004N _{std}	0.110 + 0.003N _{std}	0.082 + 0.002N _{std}
C-Z		t _{PLH}	0.213 + 0.006N _{std}	0.130 + 0.004N _{std}	0.088 + 0.003N _{std}
		t _{PHL}	0.179 + 0.004N _{std}	0.131 + 0.003N _{std}	0.099 + 0.002N _{std}

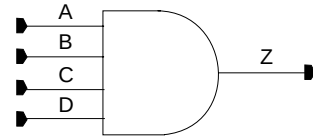
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A	0.974	0.968
B	0.982	0.980
C	0.980	0.977
Internal	5.686	7.082
Cell Units	9 cells	12 cells

Cell: AND4_G

Function: 4-Way AND

Boolean Expression: $Z = A \bullet B \bullet C \bullet D$



Propagation Delays

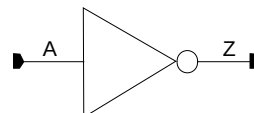
Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.205 + 0.011N _{std}	0.131 + 0.008N _{std}	0.093 + 0.006N _{std}
		t _{PHL}	0.133 + 0.008N _{std}	0.097 + 0.005N _{std}	0.072 + 0.004N _{std}
C-Z		t _{PLH}	0.234 + 0.011N _{std}	0.142 + 0.008N _{std}	0.097 + 0.006N _{std}
		t _{PHL}	0.160 + 0.008N _{std}	0.117 + 0.005N _{std}	0.088 + 0.004N _{std}
A-Z	H	t _{PLH}	0.238 + 0.006N _{std}	0.151 + 0.004N _{std}	0.107 + 0.003N _{std}
		t _{PHL}	0.152 + 0.004N _{std}	0.110 + 0.003N _{std}	0.080 + 0.002N _{std}
C-Z		t _{PLH}	0.264 + 0.006N _{std}	0.159 + 0.004N _{std}	0.108 + 0.003N _{std}
		t _{PHL}	0.179 + 0.004N _{std}	0.130 + 0.003N _{std}	0.096 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A	0.986	0.984
B	0.965	0.964
C	0.970	0.969
D	0.983	0.981
Internal	5.886	7.155
Cell Units	12 cells	15 cells

Cell: INVERT_G
Function: Inverter

Boolean Expression: $Z = \bar{A}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.080 + 0.011N _{std}	0.067 + 0.008N _{std}	0.056 + 0.006N _{std}
		t _{PHL}	0.064 + 0.008N _{std}	0.047 + 0.006N _{std}	0.033 + 0.004N _{std}
	H	t _{PLH}	0.069 + 0.006N _{std}	0.060 + 0.004N _{std}	0.052 + 0.003N _{std}
		t _{PHL}	0.055 + 0.004N _{std}	0.041 + 0.003N _{std}	0.029 + 0.002N _{std}
	J	t _{PLH}	0.069 + 0.003N _{std}	0.060 + 0.002N _{std}	0.051 + 0.001N _{std}
		t _{PHL}	0.054 + 0.002N _{std}	0.040 + 0.001N _{std}	0.029 + 0.001N _{std}
	L	t _{PLH}	0.068 + 0.002N _{std}	0.059 + 0.001N _{std}	0.051 + 0.001N _{std}
		t _{PHL}	0.054 + 0.001N _{std}	0.039 + 0.001N _{std}	0.029 + 0.001N _{std}
	N	t _{PLH}	0.067 + 0.001N _{std}	0.059 + 0.001N _{std}	0.051 + 0.001N _{std}
		t _{PHL}	0.053 + 0.001N _{std}	0.039 + 0.001N _{std}	0.028 + 0.001N _{std}
	P	t _{PLH}	0.067 + 0.001N _{std}	0.058 + 0.001N _{std}	0.050 + 0.001N _{std}
		t _{PHL}	0.052 + 0.001N _{std}	0.038 + 0.001N _{std}	0.028 + 0.000N _{std}

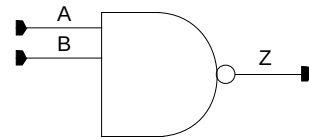
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level					
	E	H	J	L	N	P
A	1.024	1.950	3.894	5.838	7.780	9.723
Internal	2.536	4.140	8.265	12.384	16.503	20.633
Cell Units	6 cells	6 cells	9 cells	12 cells	15 cells	18 cells

Cell: NAND2_G

Function: 2-Way NAND

Boolean Expression: $Z = \overline{A \bullet B}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.080 + 0.011N _{std}	0.066 + 0.008N _{std}	0.053 + 0.006N _{std}
		t _{PHL}	0.078 + 0.013N _{std}	0.054 + 0.008N _{std}	0.039 + 0.006N _{std}
B-Z		t _{PLH}	0.090 + 0.011N _{std}	0.074 + 0.008N _{std}	0.060 + 0.006N _{std}
		t _{PHL}	0.074 + 0.013N _{std}	0.049 + 0.008N _{std}	0.034 + 0.006N _{std}
A-Z	H	t _{PLH}	0.074 + 0.006N _{std}	0.063 + 0.004N _{std}	0.052 + 0.003N _{std}
		t _{PHL}	0.073 + 0.007N _{std}	0.051 + 0.004N _{std}	0.038 + 0.003N _{std}
B-Z		t _{PLH}	0.084 + 0.006N _{std}	0.071 + 0.004N _{std}	0.058 + 0.003N _{std}
		t _{PHL}	0.068 + 0.007N _{std}	0.046 + 0.004N _{std}	0.033 + 0.003N _{std}
A-Z	J	t _{PLH}	0.074 + 0.003N _{std}	0.062 + 0.002N _{std}	0.051 + 0.001N _{std}
		t _{PHL}	0.073 + 0.003N _{std}	0.051 + 0.002N _{std}	0.038 + 0.002N _{std}
B-Z		t _{PLH}	0.084 + 0.003N _{std}	0.070 + 0.002N _{std}	0.058 + 0.001N _{std}
		t _{PHL}	0.068 + 0.003N _{std}	0.045 + 0.002N _{std}	0.032 + 0.002N _{std}
A-Z	L	t _{PLH}	0.074 + 0.002N _{std}	0.061 + 0.001N _{std}	0.051 + 0.001N _{std}
		t _{PHL}	0.072 + 0.002N _{std}	0.050 + 0.001N _{std}	0.037 + 0.001N _{std}
B-Z		t _{PLH}	0.084 + 0.002N _{std}	0.069 + 0.001N _{std}	0.058 + 0.001N _{std}
		t _{PHL}	0.068 + 0.002N _{std}	0.045 + 0.001N _{std}	0.032 + 0.001N _{std}



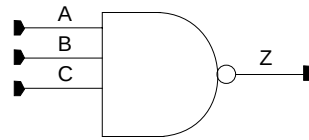
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level			
	E	H	J	L
A	0.973	1.933	4.040	5.833
B	0.991	2.051	3.987	6.019
Internal	2.659	4.828	9.637	14.447
Cell Units	6 cells	9 cells	15 cells	21 cells

Cell: NAND3_G

Function: 3-Way NAND

Boolean Expression: $Z = \overline{A \bullet B \bullet C}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.085 + 0.012N _{std}	0.067 + 0.008N _{std}	0.052 + 0.006N _{std}
		t _{PHL}	0.103 + 0.018N _{std}	0.067 + 0.011N _{std}	0.048 + 0.008N _{std}
C-Z		t _{PLH}	0.103 + 0.011N _{std}	0.081 + 0.008N _{std}	0.064 + 0.006N _{std}
		t _{PHL}	0.103 + 0.018N _{std}	0.061 + 0.011N _{std}	0.040 + 0.008N _{std}
A-Z	H	t _{PLH}	0.077 + 0.006N _{std}	0.063 + 0.004N _{std}	0.050 + 0.003N _{std}
		t _{PHL}	0.091 + 0.009N _{std}	0.061 + 0.006N _{std}	0.044 + 0.004N _{std}
C-Z		t _{PLH}	0.096 + 0.006N _{std}	0.077 + 0.004N _{std}	0.062 + 0.003N _{std}
		t _{PHL}	0.091 + 0.009N _{std}	0.054 + 0.006N _{std}	0.036 + 0.004N _{std}

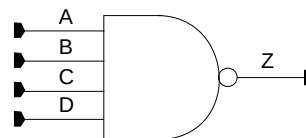
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A	0.996	1.918
B	0.968	2.015
C	0.989	2.137
Internal	3.225	5.715
Cell Units	6 cells	12 cells

Cell: NAND4_G

Function: 4-Way NAND

Boolean Expression: $Z = \overline{A \bullet B \bullet C \bullet D}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.083 + 0.012N _{std}	0.064 + 0.008N _{std}	0.048 + 0.007N _{std}
		t _{PHL}	0.116 + 0.023N _{std}	0.073 + 0.014N _{std}	0.052 + 0.010N _{std}
D-Z		t _{PLH}	0.107 + 0.012N _{std}	0.083 + 0.008N _{std}	0.065 + 0.006N _{std}
		t _{PHL}	0.129 + 0.023N _{std}	0.072 + 0.014N _{std}	0.045 + 0.010N _{std}
A-Z	H	t _{PLH}	0.080 + 0.006N _{std}	0.063 + 0.004N _{std}	0.049 + 0.003N _{std}
		t _{PHL}	0.111 + 0.012N _{std}	0.072 + 0.007N _{std}	0.052 + 0.005N _{std}
D-Z		t _{PLH}	0.105 + 0.006N _{std}	0.083 + 0.004N _{std}	0.065 + 0.003N _{std}
		t _{PHL}	0.126 + 0.012N _{std}	0.071 + 0.007N _{std}	0.045 + 0.005N _{std}

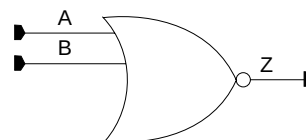
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A	0.986	1.921
B	0.965	2.014
C	0.969	2.094
D	0.990	2.184
Internal	3.393	6.559
Cell Units	9 cells	15 cells

Cell: NOR2_G

Function: 2-Way NOR

Boolean Expression: $Z = \overline{A + B}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.097 + 0.022N _{std}	0.076 + 0.015N _{std}	0.063 + 0.011N _{std}
		t _{PHL}	0.056 + 0.009N _{std}	0.036 + 0.006N _{std}	0.021 + 0.005N _{std}
B-Z		t _{PLH}	0.099 + 0.022N _{std}	0.072 + 0.015N _{std}	0.056 + 0.011N _{std}
		t _{PHL}	0.067 + 0.009N _{std}	0.045 + 0.006N _{std}	0.029 + 0.005N _{std}
A-Z	H	t _{PLH}	0.088 + 0.011N _{std}	0.071 + 0.008N _{std}	0.060 + 0.005N _{std}
		t _{PHL}	0.050 + 0.004N _{std}	0.033 + 0.003N _{std}	0.019 + 0.003N _{std}
B-Z		t _{PLH}	0.089 + 0.011N _{std}	0.067 + 0.008N _{std}	0.053 + 0.005N _{std}
		t _{PHL}	0.061 + 0.004N _{std}	0.042 + 0.003N _{std}	0.027 + 0.002N _{std}
A-Z	J	t _{PLH}	0.083 + 0.006N _{std}	0.065 + 0.004N _{std}	0.052 + 0.003N _{std}
		t _{PHL}	0.065 + 0.003N _{std}	0.046 + 0.002N _{std}	0.033 + 0.002N _{std}
B-Z		t _{PLH}	0.083 + 0.006N _{std}	0.065 + 0.004N _{std}	0.052 + 0.003N _{std}
		t _{PHL}	0.065 + 0.003N _{std}	0.046 + 0.002N _{std}	0.033 + 0.002N _{std}
A-Z	L	t _{PLH}	0.085 + 0.004N _{std}	0.066 + 0.003N _{std}	0.054 + 0.002N _{std}
		t _{PHL}	0.061 + 0.002N _{std}	0.042 + 0.001N _{std}	0.029 + 0.001N _{std}
B-Z		t _{PLH}	0.085 + 0.004N _{std}	0.067 + 0.003N _{std}	0.054 + 0.002N _{std}
		t _{PHL}	0.061 + 0.002N _{std}	0.042 + 0.001N _{std}	0.029 + 0.001N _{std}



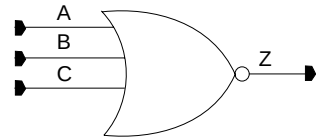
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level			
	E	H	J	L
A	0.978	2.009	3.673	5.718
B	0.969	2.088	3.613	5.680
Internal	2.672	4.759	8.629	13.413
Cell Units	6 cells	9 cells	15 cells	21 cells

Cell: NOR3_G

Function: 3-Way NOR

Boolean Expression: $Z = \overline{A + B + C}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.129 + 0.032N _{std}	0.097 + 0.022N _{std}	0.078 + 0.016N _{std}
		t _{PHL}	0.057 + 0.009N _{std}	0.035 + 0.007N _{std}	0.018 + 0.006N _{std}
C-Z		t _{PLH}	0.159 + 0.033N _{std}	0.107 + 0.022N _{std}	0.078 + 0.016N _{std}
		t _{PHL}	0.072 + 0.009N _{std}	0.047 + 0.007N _{std}	0.029 + 0.006N _{std}
A-Z	H	t _{PLH}	0.108 + 0.016N _{std}	0.084 + 0.011N _{std}	0.070 + 0.008N _{std}
		t _{PHL}	0.049 + 0.005N _{std}	0.030 + 0.004N _{std}	0.015 + 0.003N _{std}
C-Z		t _{PLH}	0.139 + 0.016N _{std}	0.094 + 0.011N _{std}	0.070 + 0.008N _{std}
		t _{PHL}	0.065 + 0.005N _{std}	0.043 + 0.003N _{std}	0.026 + 0.003N _{std}

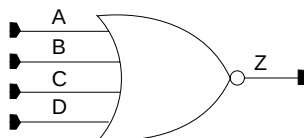
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A	1.003	2.003
B	0.976	2.067
C	0.970	2.188
Internal	3.123	5.487
Cell Units	6 cells	12 cells

Cell: NOR4_G

Function: 4-Way NOR

Boolean Expression: $Z = \overline{A + B + C + D}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.242 + 0.011N _{std}	0.165 + 0.008N _{std}	0.121 + 0.006N _{std}
		t _{PHL}	0.153 + 0.008N _{std}	0.097 + 0.005N _{std}	0.063 + 0.004N _{std}
D-Z		t _{PLH}	0.238 + 0.011N _{std}	0.158 + 0.008N _{std}	0.113 + 0.006N _{std}
		t _{PHL}	0.172 + 0.008N _{std}	0.111 + 0.005N _{std}	0.074 + 0.004N _{std}
A-Z	H	t _{PLH}	0.253 + 0.006N _{std}	0.173 + 0.004N _{std}	0.127 + 0.003N _{std}
		t _{PHL}	0.162 + 0.004N _{std}	0.104 + 0.003N _{std}	0.068 + 0.002N _{std}
D-Z		t _{PLH}	0.250 + 0.006N _{std}	0.165 + 0.004N _{std}	0.119 + 0.003N _{std}
		t _{PHL}	0.182 + 0.004N _{std}	0.118 + 0.003N _{std}	0.079 + 0.002N _{std}

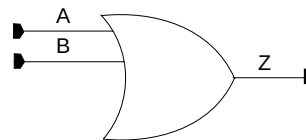
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A	1.012	1.012
B	1.013	1.013
C	1.031	1.031
D	1.027	1.027
Internal	7.363	8.413
Cell Units	18 cells	18 cells

Cell: OR2_G

Function: 2-Way OR

Boolean Expression: $Z = A + B$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.100 + 0.011N _{std}	0.064 + 0.008N _{std}	0.040 + 0.006N _{std}
		t _{PHL}	0.171 + 0.008N _{std}	0.123 + 0.006N _{std}	0.095 + 0.004N _{std}
B-Z		t _{PLH}	0.114 + 0.011N _{std}	0.074 + 0.008N _{std}	0.050 + 0.006N _{std}
		t _{PHL}	0.174 + 0.008N _{std}	0.121 + 0.006N _{std}	0.089 + 0.004N _{std}
A-Z	H	t _{PLH}	0.109 + 0.006N _{std}	0.071 + 0.004N _{std}	0.047 + 0.003N _{std}
		t _{PHL}	0.199 + 0.004N _{std}	0.144 + 0.003N _{std}	0.109 + 0.002N _{std}
B-Z		t _{PLH}	0.122 + 0.006N _{std}	0.081 + 0.004N _{std}	0.056 + 0.003N _{std}
		t _{PHL}	0.200 + 0.004N _{std}	0.140 + 0.003N _{std}	0.103 + 0.002N _{std}
A-Z	J	t _{PLH}	0.099 + 0.003N _{std}	0.064 + 0.002N _{std}	0.042 + 0.001N _{std}
		t _{PHL}	0.184 + 0.002N _{std}	0.134 + 0.001N _{std}	0.103 + 0.001N _{std}
B-Z		t _{PLH}	0.117 + 0.003N _{std}	0.078 + 0.002N _{std}	0.053 + 0.001N _{std}
		t _{PHL}	0.194 + 0.002N _{std}	0.135 + 0.001N _{std}	0.100 + 0.001N _{std}
A-Z	L	t _{PLH}	0.116 + 0.002N _{std}	0.077 + 0.001N _{std}	0.051 + 0.001N _{std}
		t _{PHL}	0.218 + 0.001N _{std}	0.157 + 0.001N _{std}	0.118 + 0.001N _{std}
B-Z		t _{PLH}	0.133 + 0.002N _{std}	0.089 + 0.001N _{std}	0.062 + 0.001N _{std}
		t _{PHL}	0.227 + 0.001N _{std}	0.157 + 0.001N _{std}	0.115 + 0.001N _{std}



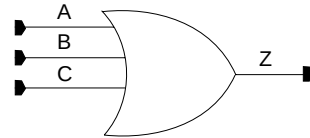
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level			
	E	H	J	L
A	1.012	0.964	1.929	1.916
B	1.007	0.963	1.953	1.947
Internal	5.051	6.343	12.106	15.684
Cell Units	9 cells	12 cells	18 cells	21 cells

Cell: OR3_G

Function: 3-Way OR

Boolean Expression: $Z = A + B + C$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.107 + 0.011N _{std}	0.068 + 0.008N _{std}	0.042 + 0.006N _{std}
		t _{PHL}	0.233 + 0.009N _{std}	0.163 + 0.006N _{std}	0.122 + 0.004N _{std}
C-Z		t _{PLH}	0.128 + 0.011N _{std}	0.083 + 0.008N _{std}	0.056 + 0.006N _{std}
		t _{PHL}	0.261 + 0.009N _{std}	0.173 + 0.006N _{std}	0.122 + 0.004N _{std}
A-Z	H	t _{PLH}	0.116 + 0.006N _{std}	0.075 + 0.004N _{std}	0.049 + 0.003N _{std}
		t _{PHL}	0.271 + 0.005N _{std}	0.190 + 0.003N _{std}	0.141 + 0.002N _{std}
C-Z		t _{PLH}	0.135 + 0.006N _{std}	0.090 + 0.004N _{std}	0.061 + 0.003N _{std}
		t _{PHL}	0.299 + 0.005N _{std}	0.199 + 0.003N _{std}	0.140 + 0.002N _{std}

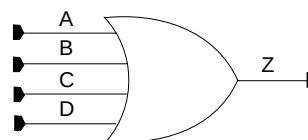
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A	1.028	1.017
B	0.980	0.975
C	0.994	0.991
Internal	5.420	6.835
Cell Units	12 cells	12 cells

Cell: OR4_G

Function: 4-Way OR

Boolean Expression: $Z = A + B + C + D$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _J = 125°C Process = Slow	V _{dd} = 1.8V T _J = 25°C Process = Nom.	V _{dd} = 1.95V T _J = 0°C Process = Fast
A-Z	E	t _{PLH}	0.103 + 0.011N _{std}	0.066 + 0.008N _{std}	0.042 + 0.006N _{std}
		t _{PHL}	0.185 + 0.013N _{std}	0.129 + 0.008N _{std}	0.098 + 0.006N _{std}
D-Z		t _{PLH}	0.120 + 0.011N _{std}	0.078 + 0.008N _{std}	0.052 + 0.006N _{std}
		t _{PHL}	0.180 + 0.013N _{std}	0.122 + 0.008N _{std}	0.090 + 0.006N _{std}
A-Z	H	t _{PLH}	0.118 + 0.006N _{std}	0.076 + 0.004N _{std}	0.050 + 0.003N _{std}
		t _{PHL}	0.218 + 0.007N _{std}	0.153 + 0.004N _{std}	0.114 + 0.003N _{std}
D-Z		t _{PLH}	0.137 + 0.006N _{std}	0.090 + 0.004N _{std}	0.062 + 0.003N _{std}
		t _{PHL}	0.216 + 0.007N _{std}	0.146 + 0.004N _{std}	0.106 + 0.003N _{std}

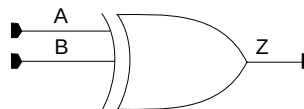
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A	0.989	0.979
B	1.007	1.003
C	1.024	1.014
D	1.023	1.018
Internal	5.203	7.343
Cell Units	15 cells	18 cells

Cell: XOR2_G

Function: 2-Way XOR

Boolean Expression: $Z = A \oplus B$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.147 + 0.022N _{std}	0.092 + 0.015N _{std}	0.059 + 0.011N _{std}
		t _{PHL}	0.187 + 0.008N _{std}	0.130 + 0.006N _{std}	0.098 + 0.004N _{std}
B-Z		t _{PLH}	0.175 + 0.022N _{std}	0.111 + 0.015N _{std}	0.073 + 0.011N _{std}
		t _{PHL}	0.190 + 0.008N _{std}	0.128 + 0.006N _{std}	0.093 + 0.004N _{std}
A-Z	H	t _{PLH}	0.207 + 0.006N _{std}	0.140 + 0.004N _{std}	0.101 + 0.003N _{std}
		t _{PHL}	0.209 + 0.004N _{std}	0.134 + 0.003N _{std}	0.093 + 0.002N _{std}
B-Z		t _{PLH}	0.235 + 0.006N _{std}	0.158 + 0.004N _{std}	0.115 + 0.003N _{std}
		t _{PHL}	0.207 + 0.004N _{std}	0.131 + 0.003N _{std}	0.089 + 0.002N _{std}
A-Z	J	t _{PLH}	0.291 + 0.003N _{std}	0.182 + 0.002N _{std}	0.118 + 0.001N _{std}
		t _{PHL}	0.302 + 0.002N _{std}	0.205 + 0.001N _{std}	0.150 + 0.001N _{std}
B-Z		t _{PLH}	0.323 + 0.003N _{std}	0.203 + 0.002N _{std}	0.137 + 0.001N _{std}
		t _{PHL}	0.305 + 0.002N _{std}	0.202 + 0.001N _{std}	0.144 + 0.001N _{std}
A-Z	L	t _{PLH}	0.310 + 0.002N _{std}	0.194 + 0.001N _{std}	0.126 + 0.001N _{std}
		t _{PHL}	0.323 + 0.001N _{std}	0.218 + 0.001N _{std}	0.159 + 0.001N _{std}
B-Z		t _{PLH}	0.343 + 0.002N _{std}	0.215 + 0.001N _{std}	0.144 + 0.001N _{std}
		t _{PHL}	0.326 + 0.001N _{std}	0.215 + 0.001N _{std}	0.153 + 0.001N _{std}



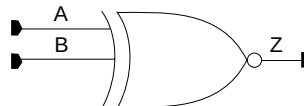
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level			
	E	H	J	L
A	1.923	1.929	1.922	1.922
B	1.975	1.969	1.969	1.969
Internal	4.574	7.796	14.637	18.609
Cell Units	12 cells	15 cells	24 cells	27 cells

Cell: XNOR2_G

Function: 2-Way XNOR

Boolean Expression: $Z = \overline{A \oplus B}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.101 + 0.022N _{std}	0.073 + 0.015N _{std}	0.055 + 0.011N _{std}
		t _{PHL}	0.137 + 0.013N _{std}	0.095 + 0.008N _{std}	0.071 + 0.006N _{std}
B-Z		t _{PLH}	0.098 + 0.022N _{std}	0.075 + 0.015N _{std}	0.061 + 0.011N _{std}
		t _{PHL}	0.161 + 0.013N _{std}	0.111 + 0.008N _{std}	0.083 + 0.006N _{std}
A-Z	H	t _{PLH}	0.244 + 0.006N _{std}	0.168 + 0.004N _{std}	0.125 + 0.003N _{std}
		t _{PHL}	0.246 + 0.004N _{std}	0.155 + 0.003N _{std}	0.101 + 0.002N _{std}
B-Z		t _{PLH}	0.247 + 0.006N _{std}	0.165 + 0.004N _{std}	0.119 + 0.003N _{std}
		t _{PHL}	0.277 + 0.004N _{std}	0.176 + 0.003N _{std}	0.117 + 0.002N _{std}
A-Z	J	t _{PLH}	0.252 + 0.003N _{std}	0.161 + 0.002N _{std}	0.111 + 0.001N _{std}
		t _{PHL}	0.266 + 0.002N _{std}	0.176 + 0.001N _{std}	0.125 + 0.001N _{std}
B-Z		t _{PLH}	0.252 + 0.003N _{std}	0.158 + 0.002N _{std}	0.108 + 0.001N _{std}
		t _{PHL}	0.294 + 0.002N _{std}	0.194 + 0.001N _{std}	0.139 + 0.001N _{std}
A-Z	L	t _{PLH}	0.266 + 0.002N _{std}	0.171 + 0.001N _{std}	0.118 + 0.001N _{std}
		t _{PHL}	0.286 + 0.001N _{std}	0.189 + 0.001N _{std}	0.134 + 0.001N _{std}
B-Z		t _{PLH}	0.266 + 0.002N _{std}	0.168 + 0.001N _{std}	0.114 + 0.001N _{std}
		t _{PHL}	0.314 + 0.001N _{std}	0.208 + 0.001N _{std}	0.148 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

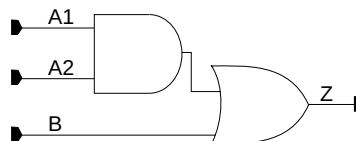
Input Pins	Performance Level			
	E	H	J	L
A	1.941	1.894	1.929	1.929
B	1.981	1.984	1.969	1.970
Internal	4.575	7.949	14.334	17.409
Cell Units	12 cells	15 cells	21 cells	24 cells

Gate Array Complex Logic

Cell: AO21_G

Function: 2x1 AND OR

Boolean Expression: $Z = (A1 \bullet A2) + B$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	E	t _{PLH}	0.124 + 0.011N _{std}	0.081 + 0.008N _{std}	0.055 + 0.006N _{std}
		t _{PHL}	0.165 + 0.008N _{std}	0.118 + 0.005N _{std}	0.090 + 0.004N _{std}
B-Z		t _{PLH}	0.117 + 0.011N _{std}	0.080 + 0.008N _{std}	0.061 + 0.006N _{std}
		t _{PHL}	0.188 + 0.008N _{std}	0.130 + 0.005N _{std}	0.090 + 0.004N _{std}
A1-Z	H	t _{PLH}	0.144 + 0.006N _{std}	0.092 + 0.004N _{std}	0.063 + 0.003N _{std}
		t _{PHL}	0.198 + 0.004N _{std}	0.142 + 0.003N _{std}	0.107 + 0.002N _{std}
B-Z		t _{PLH}	0.129 + 0.006N _{std}	0.086 + 0.004N _{std}	0.064 + 0.003N _{std}
		t _{PHL}	0.217 + 0.004N _{std}	0.151 + 0.003N _{std}	0.102 + 0.002N _{std}

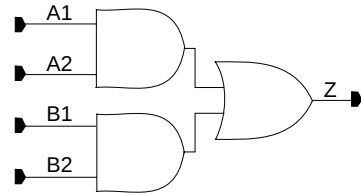
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A1	0.994	0.991
A2	1.025	1.019
B	1.009	1.007
Internal	5.210	6.436
Cell Units	9 cells	12 cells

Cell: AO22_G

Function: 2x2 AND OR

Boolean Expression: $Z = (A1 \bullet A2) + (B1 \bullet B2)$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	E	t _{PLH}	0.126 + 0.011N _{std}	0.082 + 0.008N _{std}	0.057 + 0.006N _{std}
		t _{PHL}	0.168 + 0.008N _{std}	0.120 + 0.005N _{std}	0.080 + 0.004N _{std}
B2-Z		t _{PLH}	0.157 + 0.011N _{std}	0.100 + 0.008N _{std}	0.074 + 0.006N _{std}
		t _{PHL}	0.214 + 0.008N _{std}	0.146 + 0.005N _{std}	0.098 + 0.004N _{std}
A1-Z	H	t _{PLH}	0.144 + 0.006N _{std}	0.093 + 0.004N _{std}	0.065 + 0.003N _{std}
		t _{PHL}	0.198 + 0.004N _{std}	0.143 + 0.003N _{std}	0.093 + 0.002N _{std}
B2-Z		t _{PLH}	0.173 + 0.006N _{std}	0.109 + 0.004N _{std}	0.080 + 0.003N _{std}
		t _{PHL}	0.242 + 0.004N _{std}	0.166 + 0.003N _{std}	0.109 + 0.002N _{std}

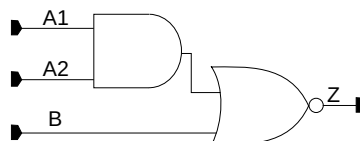
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A1	1.031	1.028
A2	1.072	1.067
B1	1.109	1.110
B2	1.022	1.028
Internal	5.525	6.717
Cell Units	12 cells	12 cells

Cell: AOI21_G

Function: 2x1 AND OR Invert

Boolean Expression: $Z = \overline{(A1 \bullet A2) + B}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	E	t _{PLH}	0.085 + 0.022N _{std}	0.067 + 0.015N _{std}	0.056 + 0.011N _{std}
		t _{PHL}	0.066 + 0.014N _{std}	0.045 + 0.009N _{std}	0.031 + 0.007N _{std}
B-Z		t _{PLH}	0.108 + 0.022N _{std}	0.079 + 0.015N _{std}	0.059 + 0.009N _{std}
		t _{PHL}	0.069 + 0.009N _{std}	0.050 + 0.006N _{std}	0.040 + 0.005N _{std}
A1-Z	H	t _{PLH}	0.108 + 0.011N _{std}	0.084 + 0.008N _{std}	0.068 + 0.005N _{std}
		t _{PHL}	0.082 + 0.007N _{std}	0.054 + 0.004N _{std}	0.036 + 0.003N _{std}
B-Z		t _{PLH}	0.117 + 0.011N _{std}	0.085 + 0.008N _{std}	0.064 + 0.004N _{std}
		t _{PHL}	0.077 + 0.004N _{std}	0.053 + 0.003N _{std}	0.040 + 0.002N _{std}

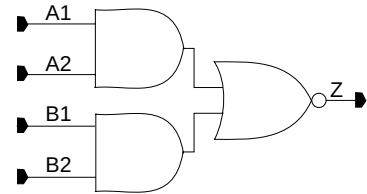
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A1	0.998	1.874
A2	1.031	2.038
B	1.010	1.956
Internal	2.791	5.987
Cell Units	6 cells	12 cells

Cell: AOI22_G

Function: 2x2 AND OR Invert

Boolean Expression: $Z = \overline{(A1 \bullet A2) + (B1 \bullet B2)}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	E	t _{PLH}	0.088 + 0.022N _{std}	0.069 + 0.015N _{std}	0.053 + 0.009N _{std}
		t _{PHL}	0.068 + 0.013N _{std}	0.046 + 0.009N _{std}	0.033 + 0.006N _{std}
B2-Z		t _{PLH}	0.130 + 0.023N _{std}	0.093 + 0.015N _{std}	0.067 + 0.009N _{std}
		t _{PHL}	0.090 + 0.013N _{std}	0.059 + 0.009N _{std}	0.046 + 0.006N _{std}
A1-Z	H	t _{PLH}	0.096 + 0.011N _{std}	0.076 + 0.008N _{std}	0.058 + 0.004N _{std}
		t _{PHL}	0.074 + 0.007N _{std}	0.050 + 0.004N _{std}	0.034 + 0.003N _{std}
B2-Z		t _{PLH}	0.139 + 0.011N _{std}	0.100 + 0.008N _{std}	0.072 + 0.004N _{std}
		t _{PHL}	0.098 + 0.007N _{std}	0.062 + 0.004N _{std}	0.047 + 0.003N _{std}

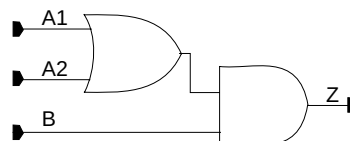
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A1	1.034	1.947
A2	1.077	2.046
B1	1.111	1.951
B2	1.023	2.049
Internal	3.149	6.361
Cell Units	9 cells	15 cells

Cell: OA21_G

Function: 2x1 OR AND

Boolean Expression: $Z = (A1 + A2) \bullet B$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	E	t _{PLH}	0.127 + 0.011N _{std}	0.080 + 0.008N _{std}	0.053 + 0.006N _{std}
		t _{PHL}	0.170 + 0.008N _{std}	0.121 + 0.006N _{std}	0.092 + 0.004N _{std}
B-Z		t _{PLH}	0.133 + 0.011N _{std}	0.084 + 0.008N _{std}	0.056 + 0.006N _{std}
		t _{PHL}	0.141 + 0.008N _{std}	0.104 + 0.005N _{std}	0.082 + 0.004N _{std}
A1-Z	H	t _{PLH}	0.140 + 0.006N _{std}	0.090 + 0.004N _{std}	0.061 + 0.003N _{std}
		t _{PHL}	0.196 + 0.004N _{std}	0.140 + 0.003N _{std}	0.105 + 0.002N _{std}
B-Z		t _{PLH}	0.145 + 0.006N _{std}	0.093 + 0.004N _{std}	0.062 + 0.003N _{std}
		t _{PHL}	0.154 + 0.004N _{std}	0.114 + 0.003N _{std}	0.089 + 0.002N _{std}

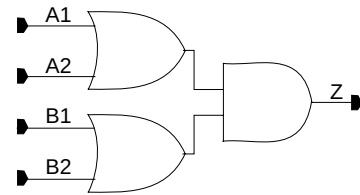
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A1	0.956	0.978
A2	1.005	0.968
B	0.985	1.012
Internal	5.194	6.415
Cell Units	9 cells	12 cells

Cell: OA22_G

Function: 2x2 OR AND

Boolean Expression: $Z = (A1 + A2) \bullet (B1 + B2)$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	E	t _{PLH}	0.162 + 0.011N _{std}	0.103 + 0.008N _{std}	0.062 + 0.006N _{std}
		t _{PHL}	0.217 + 0.008N _{std}	0.152 + 0.006N _{std}	0.113 + 0.004N _{std}
B2-Z		t _{PLH}	0.187 + 0.011N _{std}	0.116 + 0.008N _{std}	0.075 + 0.006N _{std}
		t _{PHL}	0.252 + 0.009N _{std}	0.171 + 0.006N _{std}	0.125 + 0.004N _{std}
A1-Z	H	t _{PLH}	0.176 + 0.006N _{std}	0.113 + 0.004N _{std}	0.069 + 0.003N _{std}
		t _{PHL}	0.240 + 0.004N _{std}	0.170 + 0.003N _{std}	0.126 + 0.002N _{std}
B2-Z		t _{PLH}	0.199 + 0.006N _{std}	0.125 + 0.004N _{std}	0.080 + 0.003N _{std}
		t _{PHL}	0.275 + 0.004N _{std}	0.187 + 0.003N _{std}	0.137 + 0.002N _{std}

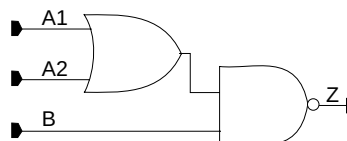
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A1	0.960	0.957
A2	1.094	1.092
B1	1.038	1.034
B2	1.004	1.003
Internal	6.277	7.671
Cell Units	12 cells	15 cells

Cell: OAI21_G

Function: 2x1 OR AND Invert

Boolean Expression: $Z = \overline{(A1 + A2)} \bullet B$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	E	t _{PLH}	0.096 + 0.022N _{std}	0.074 + 0.015N _{std}	0.060 + 0.011N _{std}
		t _{PHL}	0.070 + 0.014N _{std}	0.045 + 0.009N _{std}	0.029 + 0.007N _{std}
B-Z		t _{PLH}	0.090 + 0.012N _{std}	0.071 + 0.008N _{std}	0.060 + 0.006N _{std}
		t _{PHL}	0.074 + 0.014N _{std}	0.046 + 0.009N _{std}	0.031 + 0.006N _{std}
A1-Z	H	t _{PLH}	0.098 + 0.011N _{std}	0.077 + 0.008N _{std}	0.063 + 0.005N _{std}
		t _{PHL}	0.073 + 0.007N _{std}	0.048 + 0.004N _{std}	0.032 + 0.003N _{std}
B-Z		t _{PLH}	0.092 + 0.006N _{std}	0.074 + 0.004N _{std}	0.062 + 0.003N _{std}
		t _{PHL}	0.075 + 0.007N _{std}	0.048 + 0.004N _{std}	0.033 + 0.003N _{std}

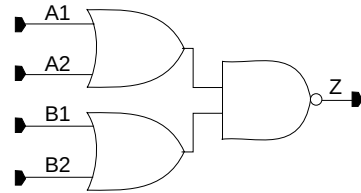
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A1	0.997	1.928
A2	0.991	2.018
B	1.001	1.927
Internal	2.798	5.628
Cell Units	6 cells	12 cells

Cell: OAI22_G

Function: 2x2 OR AND Invert

Boolean Expression: $Z = \overline{(A1 + A2) \cdot (B1 + B2)}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	E	t _{PLH}	0.131 + 0.022N _{std}	0.096 + 0.015N _{std}	0.076 + 0.011N _{std}
		t _{PHL}	0.095 + 0.013N _{std}	0.061 + 0.009N _{std}	0.036 + 0.006N _{std}
B2-Z		t _{PLH}	0.161 + 0.022N _{std}	0.114 + 0.015N _{std}	0.087 + 0.011N _{std}
		t _{PHL}	0.114 + 0.014N _{std}	0.070 + 0.009N _{std}	0.045 + 0.005N _{std}
A1-Z	H	t _{PLH}	0.099 + 0.011N _{std}	0.078 + 0.008N _{std}	0.064 + 0.005N _{std}
		t _{PHL}	0.073 + 0.007N _{std}	0.048 + 0.004N _{std}	0.028 + 0.003N _{std}
B2-Z		t _{PLH}	0.131 + 0.011N _{std}	0.095 + 0.007N _{std}	0.075 + 0.005N _{std}
		t _{PHL}	0.091 + 0.007N _{std}	0.057 + 0.004N _{std}	0.038 + 0.003N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

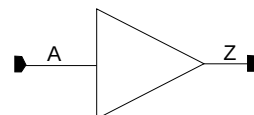
Input Pins	Performance Level	
	E	H
A1	0.966	1.883
A2	1.096	2.121
B1	1.040	2.059
B2	1.005	2.163
Internal	3.881	5.983
Cell Units	9 cells	15 cells

Gate Array Unique Logic

Cell: BUFFER_G

Function: Buffer

Boolean Expression: $Z = A$



Truth Table

Input	Output
A	Z
1	1
0	0

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-Z	E	t_{PLH}	$0.096 + 0.011N_{std}$	$0.064 + 0.008N_{std}$	$0.044 + 0.006N_{std}$
		t_{PHL}	$0.118 + 0.008N_{std}$	$0.088 + 0.005N_{std}$	$0.068 + 0.004N_{std}$
	H	t_{PLH}	$0.107 + 0.006N_{std}$	$0.072 + 0.004N_{std}$	$0.050 + 0.003N_{std}$
		t_{PHL}	$0.135 + 0.004N_{std}$	$0.101 + 0.003N_{std}$	$0.077 + 0.002N_{std}$
	J	t_{PLH}	$0.095 + 0.003N_{std}$	$0.063 + 0.002N_{std}$	$0.044 + 0.001N_{std}$
		t_{PHL}	$0.120 + 0.002N_{std}$	$0.091 + 0.001N_{std}$	$0.070 + 0.001N_{std}$
	L	t_{PLH}	$0.110 + 0.002N_{std}$	$0.075 + 0.001N_{std}$	$0.052 + 0.001N_{std}$
		t_{PHL}	$0.141 + 0.001N_{std}$	$0.106 + 0.001N_{std}$	$0.081 + 0.001N_{std}$
	N	t_{PLH}	$0.126 + 0.001N_{std}$	$0.086 + 0.001N_{std}$	$0.061 + 0.001N_{std}$
		t_{PHL}	$0.161 + 0.001N_{std}$	$0.119 + 0.001N_{std}$	$0.091 + 0.001N_{std}$
	P	t_{PLH}	$0.141 + 0.001N_{std}$	$0.096 + 0.001N_{std}$	$0.069 + 0.001N_{std}$
		t_{PHL}	$0.179 + 0.001N_{std}$	$0.132 + 0.001N_{std}$	$0.101 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level					
	E	H	J	L	N	P
A	0.984	0.980	1.931	1.940	1.937	1.933
Internal	5.084	6.273	11.648	14.910	18.335	21.913
Cell Units	6 cells	9 cells	12 cells	15 cells	18 cells	21 cells

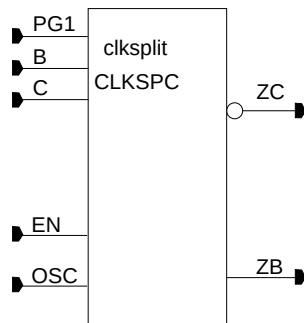
Cell: CLKSPC_G

Function: Clock Splitter

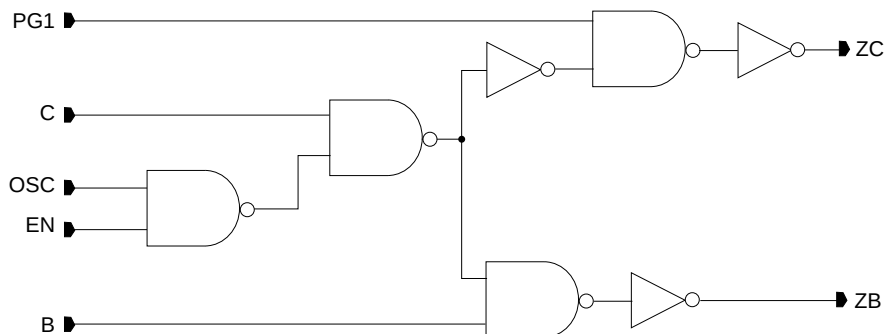
Description:

The clock splitter generates two nonoverlapping clock signals from a single oscillator input signal. The clock splitter allows independent control of clocks, and is fully testable.

EN	Disables the oscillator
PG1	Enable ZC
OSC	Oscillator input
B	LSSD B clock
C	LSSD C clock
ZB	Generated B clock (L2)
ZC	Generated C clock (L1)



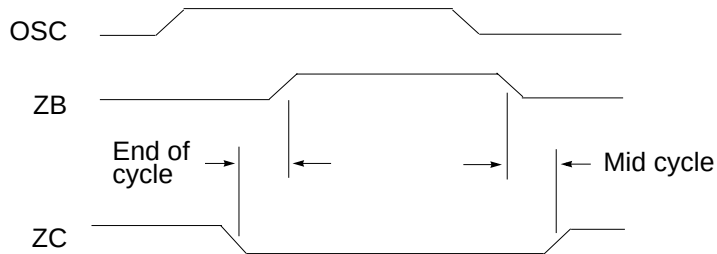
Logical Representation of Clock Splitter



Truth Table

Mode	Inputs					Outputs	
	OSC	EN	PG1	B	C	ZB	ZC
Functional	0	1	1	1	1	0	1
	1	1	1	1	1	1	0
OSC stopped	X	X	X	X	0	B	0
	X	0	X	X	1	0	PG1
Other	0	X	X	X	1	0	PG1
	1	1	X	X	X	B	0
ZC stopped	0	1	0	1	1	0	0
	1	1	0	1	1	1	0
ZB stopped	0	1	1	0	1	0	1
	1	1	1	0	1	0	0

Output Waveform



Waveform Calculation

Waveform ¹	Performance Level	Edge Separation in ns		
		V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
END OF CYCLE	H	-0.058 + 0.000N _{std}	-0.038 + 0.000N _{std}	-0.024 + 0.000N _{std}
MID CYCLE		0.147 + 0.000N _{std}	0.087 + 0.000N _{std}	0.058 - 0.001N _{std}

¹ See *Output Waveform diagram*.

Propagation Delays

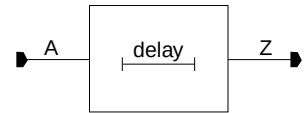
Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
OSC-ZB	H	t _{PLH}	0.319 + 0.003N _{std}	0.199 + 0.002N _{std}	0.136 + 0.001N _{std}
		t _{PHL}	0.381 + 0.003N _{std}	0.250 + 0.002N _{std}	0.178 + 0.002N _{std}
OSC-ZC		t _{PLH}	0.528 + 0.003N _{std}	0.337 + 0.002N _{std}	0.236 + 0.001N _{std}
		t _{PHL}	0.377 + 0.003N _{std}	0.237 + 0.002N _{std}	0.160 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	H
B	0.967
C	0.973
EN	0.964
OSC	0.957
PG1	1.022
Internal	15.511
Cell Units	54 cells

Cell: DELAY_G
Function: Delay Line

Boolean Expression: $Z = A$



Truth Table

Input	Output
A	Z
1	1
0	0

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-Z	U	t_{PLH}	$0.882 + 0.004N_{std}$	$0.543 + 0.003N_{std}$	$0.361 + 0.002N_{std}$
		t_{PHL}	$0.869 + 0.004N_{std}$	$0.543 + 0.003N_{std}$	$0.370 + 0.002N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

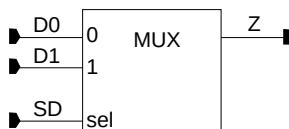
Input Pins	Performance Level
	U
A	0.999
Internal	22.110
Cell Units	36 cells

Cell: MUX21_G

Function: 2:1 Multiplexer

Description:

Selects data from D0 or D1 based on the value of the SD input pin.



Truth Table

Inputs			Output
SD	D0	D1	Z
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D0-Z	E	t _{PLH}	0.141 + 0.011N _{std}	0.090 + 0.008N _{std}	0.061 + 0.006N _{std}
		t _{PHL}	0.194 + 0.008N _{std}	0.137 + 0.006N _{std}	0.103 + 0.004N _{std}
SD-Z		t _{PLH}	0.216 + 0.011N _{std}	0.146 + 0.008N _{std}	0.106 + 0.006N _{std}
		t _{PHL}	0.237 + 0.008N _{std}	0.151 + 0.006N _{std}	0.101 + 0.004N _{std}
D0-Z	H	t _{PLH}	0.153 + 0.006N _{std}	0.099 + 0.004N _{std}	0.068 + 0.003N _{std}
		t _{PHL}	0.219 + 0.004N _{std}	0.155 + 0.003N _{std}	0.116 + 0.002N _{std}
SD-Z		t _{PLH}	0.226 + 0.006N _{std}	0.152 + 0.004N _{std}	0.111 + 0.003N _{std}
		t _{PHL}	0.260 + 0.004N _{std}	0.167 + 0.003N _{std}	0.112 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

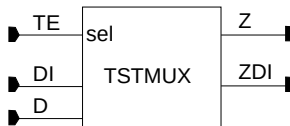
Input Pins	Performance Level	
	E	H
D0	0.967	0.981
D1	0.939	0.958
SD	2.121	2.120
Internal	7.077	8.311
Cell Units	15 cells	15 cells

Cell: PSHRDI1_G

Function: DI1 Test Function MUX

Description:

This multiplexer allows the driver inhibit (DI1) receiver to be used for both test and system function purposes (pin sharing). Input DI must be driven by the DI1 receiver and TE driven by a test enable receiver.



TE	Multiplexer control, driven by test enable receiver
DI	DI1 input, driven by DI1 receiver
D	Data input
ZDI	DI1 output
Z	Functional output

Truth Table

Inputs			Outputs	
TE	D	DI	Z	ZDI
0	X	X	DI	1
1	X	X	D	DI

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D-Z	E	t _{PLH}	0.158 + 0.011N _{std}	0.100 + 0.008N _{std}	0.068 + 0.006N _{std}
		t _{PHL}	0.197 + 0.009N _{std}	0.139 + 0.006N _{std}	0.104 + 0.004N _{std}
DI-ZDI		t _{PLH}	0.114 + 0.011N _{std}	0.074 + 0.008N _{std}	0.050 + 0.006N _{std}
		t _{PHL}	0.175 + 0.008N _{std}	0.121 + 0.006N _{std}	0.090 + 0.004N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	E
D	1.131
DI	2.071
TE	2.100
Internal	19.552
Cell Units	24 cells

Cell: PSHRDI2_G

Function: DI2 Test Function MUX

Description:

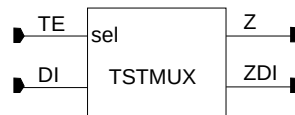
This cell allows the driver inhibit (DI2) receiver to be used for both test and system function purposes (pin sharing). Input DI must be driven by the DI2 receiver and input TE driven by a test enable receiver.

TE Multiplexer control, driven by test enable receiver

DI DI2 input, driven by DI2 receiver

ZDI DI2 output

Z Functional output



Truth Table

Inputs		Outputs	
TE	DI	Z	ZDI
0	X	DI	1
1	X	DI	DI

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
DI-Z	E	t _{PLH}	0.100 + 0.011N _{std}	0.065 + 0.008N _{std}	0.045 + 0.006N _{std}
		t _{PHL}	0.120 + 0.008N _{std}	0.089 + 0.005N _{std}	0.069 + 0.004N _{std}
DI-ZDI		t _{PLH}	0.117 + 0.011N _{std}	0.076 + 0.008N _{std}	0.051 + 0.006N _{std}
		t _{PHL}	0.178 + 0.008N _{std}	0.123 + 0.006N _{std}	0.091 + 0.004N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

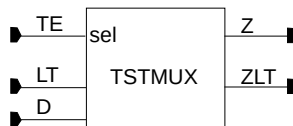
Input Pins	Performance Level
	E
DI	2.097
TE	1.006
Internal	19.165
Cell Units	18 cells

Cell: PSHRLT_G

Function: LT Test Function MUX

Description:

This multiplexer allows the leakage test (LT) receiver to be used for both test and system function purposes (pin sharing). Input LT must be driven by the leakage test receiver and input TE driven by a test enable receiver.



TE Multiplexer control, driven by test enable receiver

LT LT input, driven by leakage test receiver

D Data input

ZLT LT output

Z Functional output

Truth Table

Inputs			Outputs	
TE	D	LT	Z	ZLT
0	X	X	LT	0
1	X	X	D	LT

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D-Z	E	t _{PLH}	0.151 + 0.011N _{std}	0.096 + 0.008N _{std}	0.065 + 0.006N _{std}
		t _{PHL}	0.189 + 0.009N _{std}	0.134 + 0.006N _{std}	0.101 + 0.004N _{std}
LT-ZLT		t _{PLH}	0.125 + 0.011N _{std}	0.079 + 0.008N _{std}	0.054 + 0.006N _{std}
		t _{PHL}	0.132 + 0.008N _{std}	0.097 + 0.005N _{std}	0.074 + 0.004N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

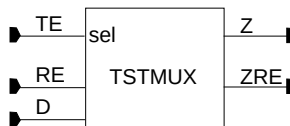
Input Pins	Performance Level
	E
D	1.033
LT	2.265
TE	3.070
Internal	19.525
Cell Units	21 cells

Cell: PSHRRE_G

Function: RE Test Function MUX

Description:

This multiplexer allows the receiver enable (RE) receiver to be used for both test and system function purposes (pin sharing). Input RE must be driven by the RE receiver and input TE driven by a test enable receiver.



TE	Multiplexer control, driven by test enable receiver
RE	RE input, driven by RE receiver
D	Data input
ZRE	RE output
Z	Functional output

Truth Table

Inputs			Outputs	
TE	D	RE	Z	ZRE
0	X	X	RE	0
1	X	X	D	RE

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D-Z	E	t _{PLH}	0.151 + 0.011N _{std}	0.096 + 0.008N _{std}	0.065 + 0.006N _{std}
		t _{PHL}	0.189 + 0.009N _{std}	0.134 + 0.006N _{std}	0.101 + 0.004N _{std}
RE-ZRE		t _{PLH}	0.125 + 0.011N _{std}	0.079 + 0.008N _{std}	0.054 + 0.006N _{std}
		t _{PHL}	0.132 + 0.008N _{std}	0.097 + 0.005N _{std}	0.074 + 0.004N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	E
D	1.033
RE	2.268
TE	3.097
Internal	19.533
Cell Units	21 cells

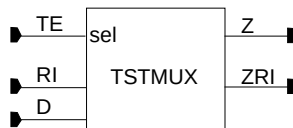
Cell: PSHRRI_G

Function: RI Test Function MUX

Description:

This multiplexer allows the receiver inhibit (RI) receiver to be used for both test and system function purposes (pin sharing). Input RI must be driven by the RI receiver and input TE driven by a test enable receiver.

TE	Multiplexer control, driven by test enable receiver
RI	RI input, driven by RI receiver
D	Data input
ZRI	RI output
Z	Functional output



Truth Table

Inputs			Outputs	
TE	D	RI	Z	ZRI
0	X	X	RI	1
1	X	X	D	RI

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D-Z	E	t _{PLH}	0.158 + 0.011N _{std}	0.100 + 0.008N _{std}	0.068 + 0.006N _{std}
		t _{PHL}	0.197 + 0.009N _{std}	0.139 + 0.006N _{std}	0.104 + 0.004N _{std}
RI-ZRI		t _{PLH}	0.114 + 0.011N _{std}	0.074 + 0.008N _{std}	0.050 + 0.006N _{std}
		t _{PHL}	0.175 + 0.008N _{std}	0.121 + 0.006N _{std}	0.090 + 0.004N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	E
D	1.131
RI	2.071
TE	2.100
Internal	19.552
Cell Units	24 cells

Cell: PSHRMC_G

Function: MC Test Function MUX

Description:

This multiplexer allows the mode control (MC) receiver to be used for both test and system function purposes (pin sharing). Input MC must be driven by the MC receiver and input TE driven by a test enable receiver.

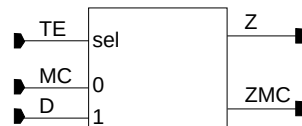
TE Multiplexer control, driven by test enable receiver

MC Mode control input, driven by MC receiver

D Data input

ZMC Mode control output

Z Functional output



Truth Table

Inputs			Outputs	
TE	D	MC	Z	ZMC
0	X	X	MC	1
1	X	X	D	MC

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
MC-ZMC	E	t _{PLH}	0.114 + 0.011N _{std}	0.074 + 0.008N _{std}	0.050 + 0.006N _{std}
		t _{PHL}	0.175 + 0.008N _{std}	0.121 + 0.006N _{std}	0.090 + 0.004N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	E
D	1.131
MC	2.070
TE	2.099
Internal	19.618
Cell Units	24 cells

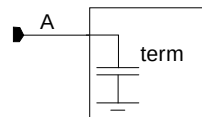
Cell: TERM_G

Function: Net Terminator

Description:

The net terminator is used to add additional capacitive load to a net. Additional load will vary the rise and fall time of the net.

Capacitive loads vary by performance level, as show in the table below.



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level					
	E	H	J	L	N	P
A	0.991	1.874	3.726	5.577	7.428	9.280
Internal	0.000	0.000	0.000	0.000	0.000	0.000
Cell Units	3 cells	3 cells	6 cells	9 cells	12 cells	15 cells

Gate Array LSSD Latches

Cell: LPH0001_G

Function: D Latch, LSSD, +L2 Output

Description:

This is a standard L1/L2 LSSD latch that is fully testable through scan rings using A and B clocks. This latch is also known as “master-slave” and is level-sensitive.

A A clock

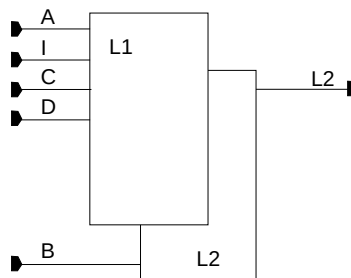
B B clock

C C clock

D Data

I Scan-in

L2 +L2 output (in phase with respect to data input)



LSSD Latch L1 Truth Table

Inputs				L1 State
A	I	C	D	
0	X	0	X	NC
1	X	0	X	I
0	X	1	X	D

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	L2
X	0	NC
X	1	L1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
B-L2	E	t _{PLH}	0.315 + 0.011N _{std}	0.200 + 0.008N _{std}	0.134 + 0.006N _{std}
		t _{PHL}	0.240 + 0.008N _{std}	0.152 + 0.005N _{std}	0.103 + 0.004N _{std}
	H	t _{PLH}	0.261 + 0.006N _{std}	0.167 + 0.004N _{std}	0.113 + 0.003N _{std}
		t _{PHL}	0.276 + 0.004N _{std}	0.175 + 0.003N _{std}	0.121 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A	1.950	1.950
B	2.057	1.982
C	2.068	2.357
D	1.027	2.044
I	1.733	1.734
Internal	11.108	13.437
Cell Units	39 cells	51 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level	
	E	H
Setup	0.317424	0.268527
Hold	-0.188696	-0.156213

¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

Cell: LPH0101_G

Function: D Latch, LSSD, +L1, +L2 Outputs

Description:

This is a standard L1/L2 LSSD latch that is fully testable through scan rings using A and B clocks. This latch is also known as “master-slave” and is level-sensitive.

A A clock

B B clock

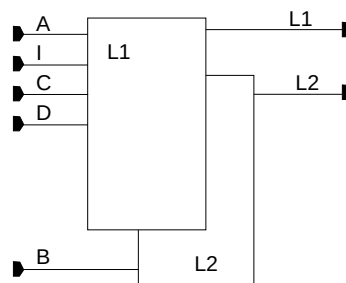
C C clock

D Data

I Scan-in

L1 +L1 output (in phase with respect to data input)

L2 +L2 output (in phase with respect to data input)



LSSD Latch L1 Truth Table

Inputs				Output
A	I	C	D	L1
0	X	0	X	NC
1	X	0	X	I
0	X	1	X	D

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	L2
X	0	NC
X	1	L1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D-L1	E	t _{PLH}	0.225 + 0.011N _{std}	0.141 + 0.008N _{std}	0.097 + 0.006N _{std}
		t _{PHL}	0.306 + 0.009N _{std}	0.205 + 0.006N _{std}	0.145 + 0.004N _{std}
B-L2		t _{PLH}	0.315 + 0.011N _{std}	0.200 + 0.008N _{std}	0.134 + 0.006N _{std}
		t _{PHL}	0.239 + 0.008N _{std}	0.151 + 0.005N _{std}	0.103 + 0.004N _{std}
D-L1	H	t _{PLH}	0.182 + 0.006N _{std}	0.114 + 0.004N _{std}	0.078 + 0.003N _{std}
		t _{PHL}	0.252 + 0.004N _{std}	0.171 + 0.003N _{std}	0.122 + 0.002N _{std}
B-L2		t _{PLH}	0.260 + 0.006N _{std}	0.167 + 0.004N _{std}	0.113 + 0.003N _{std}
		t _{PHL}	0.274 + 0.004N _{std}	0.174 + 0.003N _{std}	0.120 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A	1.962	1.950
B	2.064	1.984
C	2.067	2.392
D	1.027	2.034
I	1.723	1.724
Internal	11.164	14.252
Cell Units	42 cells	54 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level	
	E	H
Setup	0.346232	0.298717
Hold	-0.212696	-0.178463

¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

Gate Array Pseudocells

Cell: D_F_LPH0001_G

Function: D Latch Pseudocell, +L2 Output

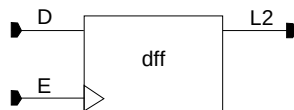
Description:

This is a standard positive edge-triggered D-FF. It is inferred by the synthesis tools and replaced by the F_LPH0001_G cell.

D Data

E E clock (positive edge clock)

L2 +L2 output (in phase with respect to input)



Truth Table

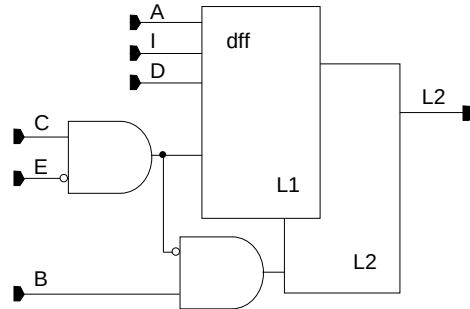
Inputs		Output
D	E	L2
X	R	D
X	F	NC

Cell: F_LPH0001_G

Function: D Latch Pseudocell, +L2 Output

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the proper C and B clocks for L1 and L2, respectively. The B and C inputs must be held high during normal system operation. This cell is replaced by real technology cell LPH0001_G and shared clock splitters.



- A A clock
- B B clock
- C C clock
- D Data
- E E clock
- I Scan-in
- L2 +L2 output (in phase with respect to input)

D-FF Operation

Inputs						Output
A	I	C	E	D	B	L2
0	X	1	R	X	1	D
0	X	1	F	X	1	NC

LSSD Latch L1 Truth Table

Inputs					L1 State
A	I	C	E	D	
0	X	0	X	X	NC
1	X	0	X	X	I
0	X	1	0	X	D
0	X	1	1	X	NC

LSSD Latch L2 Truth Table

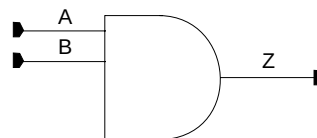
Inputs			Output
E	B	C	L2
X	0	X	NC
0	1	1	NC
X	1	0	L1
1	1	X	L1

Standard Cell Primitive Logic

Cell: AND2

Function: 2-Way AND

Boolean Expression: $Z = A \bullet B$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	B	t _{PLH}	0.128 + 0.078N _{std}	0.080 + 0.050N _{std}	0.052 + 0.034N _{std}
		t _{PHL}	0.132 + 0.035N _{std}	0.095 + 0.023N _{std}	0.072 + 0.017N _{std}
B-Z		t _{PLH}	0.125 + 0.078N _{std}	0.076 + 0.050N _{std}	0.049 + 0.034N _{std}
		t _{PHL}	0.143 + 0.036N _{std}	0.103 + 0.023N _{std}	0.078 + 0.017N _{std}
A-Z	C	t _{PLH}	0.116 + 0.036N _{std}	0.074 + 0.024N _{std}	0.050 + 0.017N _{std}
		t _{PHL}	0.132 + 0.023N _{std}	0.096 + 0.015N _{std}	0.073 + 0.011N _{std}
B-Z		t _{PLH}	0.113 + 0.035N _{std}	0.071 + 0.024N _{std}	0.047 + 0.017N _{std}
		t _{PHL}	0.143 + 0.023N _{std}	0.104 + 0.015N _{std}	0.080 + 0.011N _{std}
A-Z	D	t _{PLH}	0.114 + 0.022N _{std}	0.074 + 0.015N _{std}	0.052 + 0.011N _{std}
		t _{PHL}	0.117 + 0.018N _{std}	0.087 + 0.012N _{std}	0.066 + 0.009N _{std}
B-Z		t _{PLH}	0.111 + 0.022N _{std}	0.071 + 0.015N _{std}	0.048 + 0.011N _{std}
		t _{PHL}	0.128 + 0.018N _{std}	0.094 + 0.012N _{std}	0.073 + 0.009N _{std}
A-Z	E	t _{PLH}	0.115 + 0.016N _{std}	0.075 + 0.011N _{std}	0.053 + 0.008N _{std}
		t _{PHL}	0.119 + 0.013N _{std}	0.088 + 0.009N _{std}	0.068 + 0.007N _{std}
B-Z		t _{PLH}	0.112 + 0.016N _{std}	0.071 + 0.011N _{std}	0.049 + 0.008N _{std}
		t _{PHL}	0.130 + 0.013N _{std}	0.096 + 0.009N _{std}	0.075 + 0.007N _{std}
A-Z	F	t _{PLH}	0.111 + 0.011N _{std}	0.073 + 0.007N _{std}	0.051 + 0.006N _{std}
		t _{PHL}	0.119 + 0.009N _{std}	0.088 + 0.006N _{std}	0.069 + 0.004N _{std}
B-Z		t _{PLH}	0.109 + 0.011N _{std}	0.070 + 0.007N _{std}	0.048 + 0.006N _{std}
		t _{PHL}	0.131 + 0.009N _{std}	0.097 + 0.006N _{std}	0.076 + 0.004N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	H	t _{PLH}	0.112 + 0.009N _{std}	0.073 + 0.006N _{std}	0.050 + 0.004N _{std}
		t _{PHL}	0.140 + 0.005N _{std}	0.104 + 0.003N _{std}	0.081 + 0.002N _{std}
B-Z		t _{PLH}	0.110 + 0.009N _{std}	0.070 + 0.006N _{std}	0.048 + 0.004N _{std}
		t _{PHL}	0.155 + 0.005N _{std}	0.115 + 0.003N _{std}	0.090 + 0.002N _{std}
A-Z	I	t _{PLH}	0.123 + 0.006N _{std}	0.082 + 0.004N _{std}	0.058 + 0.003N _{std}
		t _{PHL}	0.136 + 0.004N _{std}	0.101 + 0.003N _{std}	0.078 + 0.002N _{std}
B-Z		t _{PLH}	0.120 + 0.006N _{std}	0.078 + 0.004N _{std}	0.055 + 0.003N _{std}
		t _{PHL}	0.147 + 0.004N _{std}	0.109 + 0.003N _{std}	0.085 + 0.002N _{std}
A-Z	J	t _{PLH}	0.131 + 0.004N _{std}	0.087 + 0.003N _{std}	0.061 + 0.002N _{std}
		t _{PHL}	0.157 + 0.003N _{std}	0.117 + 0.002N _{std}	0.090 + 0.001N _{std}
B-Z		t _{PLH}	0.128 + 0.004N _{std}	0.083 + 0.003N _{std}	0.058 + 0.002N _{std}
		t _{PHL}	0.171 + 0.003N _{std}	0.126 + 0.002N _{std}	0.098 + 0.001N _{std}
A-Z	K	t _{PLH}	0.145 + 0.003N _{std}	0.096 + 0.002N _{std}	0.069 + 0.002N _{std}
		t _{PHL}	0.158 + 0.002N _{std}	0.117 + 0.002N _{std}	0.090 + 0.001N _{std}
B-Z		t _{PLH}	0.141 + 0.003N _{std}	0.092 + 0.002N _{std}	0.065 + 0.002N _{std}
		t _{PHL}	0.170 + 0.002N _{std}	0.126 + 0.002N _{std}	0.097 + 0.001N _{std}



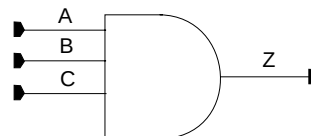
Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins			
	A	B	Internal	Cell Units
B	0.281	0.304	1.178	6 cells
C	0.357	0.362	1.594	6 cells
D	0.499	0.492	2.244	6 cells
E	0.558	0.552	2.725	6 cells
F	0.729	0.730	3.782	6 cells
H	0.735	0.736	4.499	6 cells
I	0.876	0.881	5.635	6 cells
J	0.973	0.969	7.615	8 cells
K	1.041	1.039	8.872	8 cells

Cell: AND3

Function: 3-Way AND

Boolean Expression: $Z = A \bullet B \bullet C$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	B	t _{PLH}	0.143 + 0.075N _{std}	0.087 + 0.048N _{std}	0.056 + 0.032N _{std}
		t _{PHL}	0.162 + 0.036N _{std}	0.113 + 0.024N _{std}	0.084 + 0.017N _{std}
C-Z		t _{PLH}	0.143 + 0.075N _{std}	0.084 + 0.048N _{std}	0.052 + 0.033N _{std}
		t _{PHL}	0.193 + 0.037N _{std}	0.134 + 0.024N _{std}	0.099 + 0.017N _{std}
A-Z	C	t _{PLH}	0.155 + 0.035N _{std}	0.097 + 0.024N _{std}	0.066 + 0.017N _{std}
t _{PHL}		0.149 + 0.029N _{std}	0.106 + 0.019N _{std}	0.080 + 0.014N _{std}	
C-Z		t _{PLH}	0.153 + 0.035N _{std}	0.092 + 0.024N _{std}	0.060 + 0.017N _{std}
		t _{PHL}	0.169 + 0.029N _{std}	0.121 + 0.019N _{std}	0.092 + 0.014N _{std}
A-Z	D	t _{PLH}	0.141 + 0.023N _{std}	0.090 + 0.016N _{std}	0.062 + 0.011N _{std}
t _{PHL}		0.134 + 0.020N _{std}	0.098 + 0.013N _{std}	0.074 + 0.010N _{std}	
C-Z		t _{PLH}	0.140 + 0.023N _{std}	0.086 + 0.016N _{std}	0.057 + 0.011N _{std}
		t _{PHL}	0.156 + 0.020N _{std}	0.114 + 0.013N _{std}	0.087 + 0.010N _{std}
A-Z	E	t _{PLH}	0.150 + 0.016N _{std}	0.096 + 0.011N _{std}	0.067 + 0.008N _{std}
t _{PHL}		0.137 + 0.014N _{std}	0.100 + 0.009N _{std}	0.076 + 0.007N _{std}	
C-Z		t _{PLH}	0.149 + 0.016N _{std}	0.091 + 0.011N _{std}	0.061 + 0.008N _{std}
		t _{PHL}	0.157 + 0.014N _{std}	0.115 + 0.009N _{std}	0.088 + 0.007N _{std}
A-Z	F	t _{PLH}	0.147 + 0.011N _{std}	0.094 + 0.008N _{std}	0.066 + 0.006N _{std}
t _{PHL}		0.137 + 0.009N _{std}	0.100 + 0.006N _{std}	0.076 + 0.004N _{std}	
C-Z		t _{PLH}	0.146 + 0.011N _{std}	0.090 + 0.008N _{std}	0.060 + 0.006N _{std}
		t _{PHL}	0.158 + 0.009N _{std}	0.116 + 0.006N _{std}	0.089 + 0.004N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	H	t _{PLH}	0.145 + 0.008N _{std}	0.093 + 0.005N _{std}	0.065 + 0.004N _{std}
		t _{PHL}	0.152 + 0.004N _{std}	0.112 + 0.003N _{std}	0.086 + 0.002N _{std}
C-Z		t _{PLH}	0.145 + 0.008N _{std}	0.090 + 0.005N _{std}	0.060 + 0.004N _{std}
		t _{PHL}	0.180 + 0.005N _{std}	0.132 + 0.003N _{std}	0.101 + 0.002N _{std}
A-Z	I	t _{PLH}	0.153 + 0.006N _{std}	0.099 + 0.004N _{std}	0.070 + 0.003N _{std}
		t _{PHL}	0.155 + 0.004N _{std}	0.114 + 0.003N _{std}	0.088 + 0.002N _{std}
C-Z		t _{PLH}	0.154 + 0.006N _{std}	0.095 + 0.004N _{std}	0.064 + 0.003N _{std}
		t _{PHL}	0.180 + 0.004N _{std}	0.132 + 0.003N _{std}	0.101 + 0.002N _{std}
A-Z	J	t _{PLH}	0.157 + 0.004N _{std}	0.101 + 0.003N _{std}	0.070 + 0.002N _{std}
		t _{PHL}	0.163 + 0.002N _{std}	0.121 + 0.002N _{std}	0.093 + 0.001N _{std}
C-Z		t _{PLH}	0.158 + 0.004N _{std}	0.098 + 0.003N _{std}	0.065 + 0.002N _{std}
		t _{PHL}	0.191 + 0.002N _{std}	0.140 + 0.002N _{std}	0.108 + 0.001N _{std}
A-Z	K	t _{PLH}	0.157 + 0.003N _{std}	0.102 + 0.002N _{std}	0.071 + 0.002N _{std}
		t _{PHL}	0.168 + 0.002N _{std}	0.124 + 0.002N _{std}	0.095 + 0.001N _{std}
C-Z		t _{PLH}	0.158 + 0.003N _{std}	0.098 + 0.002N _{std}	0.066 + 0.002N _{std}
		t _{PHL}	0.195 + 0.002N _{std}	0.143 + 0.002N _{std}	0.110 + 0.001N _{std}

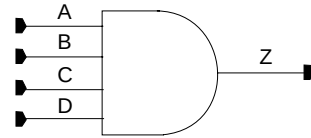
Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins				
	A	B	C	Internal	Cell Units
B	0.286	0.281	0.293	1.225	7 cells
C	0.341	0.317	0.330	1.581	7 cells
D	0.490	0.455	0.465	2.291	7 cells
E	0.525	0.491	0.500	2.731	7 cells
F	0.659	0.636	0.641	3.757	7 cells
H	0.777	0.751	0.754	5.053	7 cells
I	0.883	0.863	0.864	6.159	7 cells
J	1.102	1.174	1.184	8.872	10 cells
K	1.219	1.300	1.304	10.134	10 cells

Cell: AND4

Function: 4-Way AND

Boolean Expression: $Z = A \bullet B \bullet C \bullet D$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	B	t _{PLH}	0.171 + 0.065N _{std}	0.105 + 0.042N _{std}	0.070 + 0.029N _{std}
		t _{PHL}	0.143 + 0.035N _{std}	0.102 + 0.023N _{std}	0.075 + 0.017N _{std}
C-Z		t _{PLH}	0.180 + 0.065N _{std}	0.107 + 0.042N _{std}	0.069 + 0.029N _{std}
		t _{PHL}	0.168 + 0.036N _{std}	0.119 + 0.023N _{std}	0.089 + 0.017N _{std}
A-Z	C	t _{PLH}	0.163 + 0.034N _{std}	0.102 + 0.023N _{std}	0.069 + 0.016N _{std}
		t _{PHL}	0.151 + 0.027N _{std}	0.108 + 0.017N _{std}	0.081 + 0.013N _{std}
C-Z		t _{PLH}	0.173 + 0.034N _{std}	0.103 + 0.023N _{std}	0.068 + 0.016N _{std}
		t _{PHL}	0.177 + 0.027N _{std}	0.126 + 0.018N _{std}	0.095 + 0.013N _{std}
A-Z	D	t _{PLH}	0.163 + 0.022N _{std}	0.103 + 0.015N _{std}	0.071 + 0.011N _{std}
		t _{PHL}	0.153 + 0.018N _{std}	0.110 + 0.012N _{std}	0.083 + 0.009N _{std}
C-Z		t _{PLH}	0.173 + 0.022N _{std}	0.104 + 0.015N _{std}	0.069 + 0.011N _{std}
		t _{PHL}	0.179 + 0.019N _{std}	0.129 + 0.012N _{std}	0.098 + 0.009N _{std}
A-Z	E	t _{PLH}	0.164 + 0.016N _{std}	0.104 + 0.011N _{std}	0.072 + 0.008N _{std}
		t _{PHL}	0.152 + 0.014N _{std}	0.110 + 0.009N _{std}	0.083 + 0.007N _{std}
C-Z		t _{PLH}	0.174 + 0.016N _{std}	0.105 + 0.011N _{std}	0.070 + 0.008N _{std}
		t _{PHL}	0.178 + 0.014N _{std}	0.128 + 0.009N _{std}	0.098 + 0.007N _{std}
A-Z	F	t _{PLH}	0.166 + 0.010N _{std}	0.107 + 0.007N _{std}	0.075 + 0.005N _{std}
		t _{PHL}	0.153 + 0.009N _{std}	0.112 + 0.006N _{std}	0.086 + 0.004N _{std}
C-Z		t _{PLH}	0.177 + 0.010N _{std}	0.109 + 0.007N _{std}	0.073 + 0.005N _{std}
		t _{PHL}	0.179 + 0.009N _{std}	0.131 + 0.006N _{std}	0.100 + 0.004N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	H	t _{PLH}	0.165 + 0.008N _{std}	0.106 + 0.005N _{std}	0.075 + 0.004N _{std}
		t _{PHL}	0.151 + 0.006N _{std}	0.111 + 0.004N _{std}	0.085 + 0.003N _{std}
C-Z		t _{PLH}	0.177 + 0.008N _{std}	0.109 + 0.005N _{std}	0.073 + 0.004N _{std}
		t _{PHL}	0.178 + 0.006N _{std}	0.130 + 0.004N _{std}	0.099 + 0.003N _{std}
A-Z	I	t _{PLH}	0.204 + 0.005N _{std}	0.129 + 0.004N _{std}	0.089 + 0.003N _{std}
		t _{PHL}	0.179 + 0.004N _{std}	0.131 + 0.003N _{std}	0.099 + 0.002N _{std}
C-Z		t _{PLH}	0.213 + 0.005N _{std}	0.130 + 0.004N _{std}	0.087 + 0.003N _{std}
		t _{PHL}	0.203 + 0.004N _{std}	0.148 + 0.003N _{std}	0.113 + 0.002N _{std}
A-Z	J	t _{PLH}	0.196 + 0.004N _{std}	0.125 + 0.003N _{std}	0.086 + 0.002N _{std}
		t _{PHL}	0.186 + 0.003N _{std}	0.136 + 0.002N _{std}	0.103 + 0.002N _{std}
C-Z		t _{PLH}	0.206 + 0.004N _{std}	0.126 + 0.003N _{std}	0.085 + 0.002N _{std}
		t _{PHL}	0.213 + 0.003N _{std}	0.155 + 0.002N _{std}	0.118 + 0.002N _{std}
A-Z	K	t _{PLH}	0.202 + 0.003N _{std}	0.129 + 0.002N _{std}	0.090 + 0.002N _{std}
		t _{PHL}	0.180 + 0.002N _{std}	0.132 + 0.002N _{std}	0.100 + 0.001N _{std}
C-Z		t _{PLH}	0.213 + 0.003N _{std}	0.131 + 0.002N _{std}	0.088 + 0.002N _{std}
		t _{PHL}	0.205 + 0.002N _{std}	0.150 + 0.002N _{std}	0.114 + 0.001N _{std}



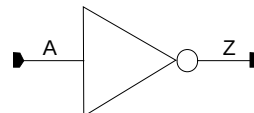
Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins					
	A	B	C	D	Internal	Cell Units
B	0.359	0.361	0.374	0.328	1.511	8 cells
C	0.397	0.395	0.409	0.367	1.849	8 cells
D	0.449	0.444	0.458	0.420	2.299	8 cells
E	0.518	0.510	0.525	0.493	2.836	8 cells
F	0.645	0.631	0.647	0.625	3.956	9 cells
H	0.804	0.779	0.795	0.790	5.071	9 cells
I	0.902	0.902	0.857	0.904	6.692	16 cells
J	1.057	1.051	1.009	1.060	8.403	16 cells
K	1.264	1.239	1.213	1.256	10.580	16 cells

Cell: INVERT

Function: Inverter

Boolean Expression: $Z = \bar{A}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-Z	A	t_{PLH}	$0.092 + 0.085N_{std}$	$0.072 + 0.054N_{std}$	$0.061 + 0.036N_{std}$
		t_{PHL}	$0.043 + 0.036N_{std}$	$0.029 + 0.024N_{std}$	$0.016 + 0.019N_{std}$
	B	t_{PLH}	$0.084 + 0.069N_{std}$	$0.067 + 0.045N_{std}$	$0.057 + 0.031N_{std}$
		t_{PHL}	$0.046 + 0.036N_{std}$	$0.032 + 0.024N_{std}$	$0.019 + 0.018N_{std}$
	C	t_{PLH}	$0.066 + 0.033N_{std}$	$0.055 + 0.023N_{std}$	$0.047 + 0.017N_{std}$
		t_{PHL}	$0.050 + 0.024N_{std}$	$0.036 + 0.016N_{std}$	$0.026 + 0.012N_{std}$
	D	t_{PLH}	$0.063 + 0.022N_{std}$	$0.053 + 0.015N_{std}$	$0.046 + 0.011N_{std}$
		t_{PHL}	$0.050 + 0.016N_{std}$	$0.037 + 0.011N_{std}$	$0.027 + 0.009N_{std}$
	E	t_{PLH}	$0.063 + 0.016N_{std}$	$0.053 + 0.011N_{std}$	$0.046 + 0.008N_{std}$
		t_{PHL}	$0.050 + 0.012N_{std}$	$0.037 + 0.008N_{std}$	$0.028 + 0.006N_{std}$
	F	t_{PLH}	$0.069 + 0.010N_{std}$	$0.058 + 0.007N_{std}$	$0.051 + 0.005N_{std}$
		t_{PHL}	$0.038 + 0.005N_{std}$	$0.028 + 0.003N_{std}$	$0.018 + 0.003N_{std}$
	H	t_{PLH}	$0.064 + 0.007N_{std}$	$0.055 + 0.005N_{std}$	$0.048 + 0.004N_{std}$
		t_{PHL}	$0.045 + 0.004N_{std}$	$0.033 + 0.003N_{std}$	$0.024 + 0.002N_{std}$
	I	t_{PLH}	$0.062 + 0.005N_{std}$	$0.053 + 0.004N_{std}$	$0.046 + 0.003N_{std}$
		t_{PHL}	$0.049 + 0.004N_{std}$	$0.038 + 0.003N_{std}$	$0.029 + 0.002N_{std}$
	J	t_{PLH}	$0.063 + 0.004N_{std}$	$0.054 + 0.003N_{std}$	$0.047 + 0.002N_{std}$
		t_{PHL}	$0.051 + 0.003N_{std}$	$0.039 + 0.002N_{std}$	$0.031 + 0.001N_{std}$
	K	t_{PLH}	$0.063 + 0.003N_{std}$	$0.054 + 0.002N_{std}$	$0.047 + 0.002N_{std}$
		t_{PHL}	$0.050 + 0.002N_{std}$	$0.038 + 0.002N_{std}$	$0.029 + 0.001N_{std}$
	L	t_{PLH}	$0.063 + 0.003N_{std}$	$0.054 + 0.002N_{std}$	$0.047 + 0.001N_{std}$
		t_{PHL}	$0.050 + 0.002N_{std}$	$0.038 + 0.001N_{std}$	$0.028 + 0.001N_{std}$

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-Z	M	t_{PLH}	$0.061 + 0.002N_{std}$	$0.053 + 0.001N_{std}$	$0.046 + 0.001N_{std}$
		t_{PHL}	$0.052 + 0.001N_{std}$	$0.040 + 0.001N_{std}$	$0.031 + 0.001N_{std}$
	N	t_{PLH}	$0.060 + 0.001N_{std}$	$0.052 + 0.001N_{std}$	$0.045 + 0.001N_{std}$
		t_{PHL}	$0.053 + 0.001N_{std}$	$0.041 + 0.001N_{std}$	$0.032 + 0.001N_{std}$
	O	t_{PLH}	$0.060 + 0.001N_{std}$	$0.052 + 0.001N_{std}$	$0.045 + 0.001N_{std}$
		t_{PHL}	$0.052 + 0.001N_{std}$	$0.040 + 0.001N_{std}$	$0.031 + 0.001N_{std}$
	U	t_{PLH}	$0.042 + 0.000N_{std}$	$0.038 + 0.000N_{std}$	$0.033 + 0.000N_{std}$
		t_{PHL}	$0.059 + 0.000N_{std}$	$0.046 + 0.000N_{std}$	$0.037 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins		
	A	Internal	Cell Units
A	0.253	0.531	3 cells
B	0.265	0.569	3 cells
C	0.396	0.862	3 cells
D	0.554	1.198	3 cells
E	0.720	1.575	3 cells
F	1.528	3.042	3 cells
H	1.716	3.542	3 cells
I	2.005	4.286	3 cells
J	2.894	6.235	5 cells
K	3.572	7.662	5 cells
L	4.018	8.701	5 cells
M	5.758	12.389	8 cells
N	7.277	15.820	10 cells
O	8.768	18.941	13 cells
U	19.369	47.105	26 cells

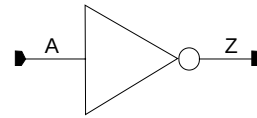
Cell: INVERTBAL

Function: Balanced Inverter

Description:

Balanced rising and falling delay.

Boolean Expression: $Z = \bar{A}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-Z	E	t_{PLH}	$0.058 + 0.009N_{std}$	$0.050 + 0.006N_{std}$	$0.043 + 0.005N_{std}$
		t_{PHL}	$0.056 + 0.009N_{std}$	$0.042 + 0.006N_{std}$	$0.033 + 0.005N_{std}$
	H	t_{PLH}	$0.058 + 0.006N_{std}$	$0.050 + 0.004N_{std}$	$0.043 + 0.003N_{std}$
		t_{PHL}	$0.056 + 0.005N_{std}$	$0.043 + 0.004N_{std}$	$0.034 + 0.003N_{std}$
	J	t_{PLH}	$0.059 + 0.003N_{std}$	$0.051 + 0.002N_{std}$	$0.044 + 0.001N_{std}$
		t_{PHL}	$0.057 + 0.003N_{std}$	$0.044 + 0.002N_{std}$	$0.035 + 0.001N_{std}$
	L	t_{PLH}	$0.059 + 0.002N_{std}$	$0.051 + 0.001N_{std}$	$0.044 + 0.001N_{std}$
		t_{PHL}	$0.057 + 0.002N_{std}$	$0.044 + 0.001N_{std}$	$0.035 + 0.001N_{std}$

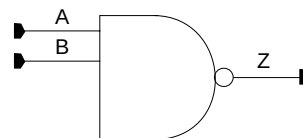
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level			
	E	H	J	L
A	1.107	1.701	3.401	5.104
Internal	2.406	3.693	7.394	11.033
Cell Units	3 cells	3 cells	6 cells	9 cells

Cell: NAND2

Function: 2-Way NAND

Boolean Expression: $Z = \overline{A \bullet B}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	A	t _{PLH}	0.087 + 0.066N _{std}	0.068 + 0.044N _{std}	0.056 + 0.030N _{std}
		t _{PHL}	0.065 + 0.055N _{std}	0.044 + 0.034N _{std}	0.029 + 0.024N _{std}
B-Z		t _{PLH}	0.095 + 0.066N _{std}	0.075 + 0.043N _{std}	0.062 + 0.030N _{std}
		t _{PHL}	0.059 + 0.055N _{std}	0.038 + 0.034N _{std}	0.024 + 0.024N _{std}
A-Z	B	t _{PLH}	0.085 + 0.059N _{std}	0.067 + 0.039N _{std}	0.055 + 0.027N _{std}
		t _{PHL}	0.059 + 0.045N _{std}	0.039 + 0.028N _{std}	0.026 + 0.020N _{std}
B-Z		t _{PLH}	0.095 + 0.058N _{std}	0.075 + 0.039N _{std}	0.062 + 0.027N _{std}
		t _{PHL}	0.054 + 0.044N _{std}	0.035 + 0.028N _{std}	0.022 + 0.020N _{std}
A-Z	C	t _{PLH}	0.073 + 0.027N _{std}	0.060 + 0.019N _{std}	0.051 + 0.014N _{std}
		t _{PHL}	0.054 + 0.022N _{std}	0.037 + 0.014N _{std}	0.026 + 0.011N _{std}
B-Z		t _{PLH}	0.085 + 0.027N _{std}	0.069 + 0.019N _{std}	0.058 + 0.014N _{std}
		t _{PHL}	0.051 + 0.022N _{std}	0.034 + 0.014N _{std}	0.022 + 0.011N _{std}
A-Z	D	t _{PLH}	0.071 + 0.018N _{std}	0.059 + 0.012N _{std}	0.050 + 0.009N _{std}
		t _{PHL}	0.055 + 0.015N _{std}	0.038 + 0.010N _{std}	0.027 + 0.007N _{std}
B-Z		t _{PLH}	0.083 + 0.017N _{std}	0.068 + 0.012N _{std}	0.057 + 0.009N _{std}
		t _{PHL}	0.052 + 0.015N _{std}	0.035 + 0.009N _{std}	0.024 + 0.007N _{std}
A-Z	E	t _{PLH}	0.071 + 0.013N _{std}	0.059 + 0.009N _{std}	0.051 + 0.007N _{std}
		t _{PHL}	0.056 + 0.011N _{std}	0.039 + 0.007N _{std}	0.028 + 0.005N _{std}
B-Z		t _{PLH}	0.083 + 0.013N _{std}	0.068 + 0.009N _{std}	0.058 + 0.007N _{std}
		t _{PHL}	0.053 + 0.011N _{std}	0.036 + 0.007N _{std}	0.025 + 0.005N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	F	t _{PLH}	0.073 + 0.010N _{std}	0.061 + 0.007N _{std}	0.052 + 0.005N _{std}
		t _{PHL}	0.050 + 0.007N _{std}	0.035 + 0.004N _{std}	0.024 + 0.003N _{std}
B-Z		t _{PLH}	0.088 + 0.010N _{std}	0.071 + 0.007N _{std}	0.061 + 0.005N _{std}
		t _{PHL}	0.048 + 0.007N _{std}	0.032 + 0.004N _{std}	0.021 + 0.003N _{std}
A-Z	H	t _{PLH}	0.075 + 0.005N _{std}	0.062 + 0.004N _{std}	0.054 + 0.003N _{std}
t _{PHL}		0.051 + 0.004N _{std}	0.036 + 0.002N _{std}	0.025 + 0.002N _{std}	
B-Z		t _{PLH}	0.090 + 0.005N _{std}	0.073 + 0.004N _{std}	0.062 + 0.003N _{std}
		t _{PHL}	0.048 + 0.003N _{std}	0.032 + 0.002N _{std}	0.022 + 0.002N _{std}
A-Z	I	t _{PLH}	0.076 + 0.005N _{std}	0.063 + 0.003N _{std}	0.055 + 0.003N _{std}
t _{PHL}		0.049 + 0.003N _{std}	0.035 + 0.002N _{std}	0.024 + 0.002N _{std}	
B-Z		t _{PLH}	0.093 + 0.005N _{std}	0.075 + 0.003N _{std}	0.063 + 0.003N _{std}
		t _{PHL}	0.046 + 0.003N _{std}	0.031 + 0.002N _{std}	0.020 + 0.002N _{std}
A-Z	J	t _{PLH}	0.077 + 0.004N _{std}	0.064 + 0.002N _{std}	0.055 + 0.002N _{std}
t _{PHL}		0.055 + 0.003N _{std}	0.038 + 0.002N _{std}	0.028 + 0.001N _{std}	
B-Z		t _{PLH}	0.077 + 0.004N _{std}	0.064 + 0.002N _{std}	0.055 + 0.002N _{std}
		t _{PHL}	0.055 + 0.003N _{std}	0.038 + 0.002N _{std}	0.028 + 0.001N _{std}
A-Z	K	t _{PLH}	0.076 + 0.003N _{std}	0.063 + 0.002N _{std}	0.054 + 0.001N _{std}
t _{PHL}		0.057 + 0.002N _{std}	0.040 + 0.002N _{std}	0.029 + 0.001N _{std}	
B-Z		t _{PLH}	0.077 + 0.003N _{std}	0.064 + 0.002N _{std}	0.055 + 0.001N _{std}
		t _{PHL}	0.057 + 0.002N _{std}	0.039 + 0.002N _{std}	0.028 + 0.001N _{std}
A-Z	L	t _{PLH}	0.075 + 0.002N _{std}	0.063 + 0.002N _{std}	0.054 + 0.001N _{std}
t _{PHL}		0.057 + 0.002N _{std}	0.040 + 0.001N _{std}	0.029 + 0.001N _{std}	
B-Z		t _{PLH}	0.075 + 0.002N _{std}	0.062 + 0.002N _{std}	0.054 + 0.001N _{std}
		t _{PHL}	0.057 + 0.002N _{std}	0.040 + 0.001N _{std}	0.029 + 0.001N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	M	t _{PLH}	0.077 + 0.002N _{std}	0.064 + 0.001N _{std}	0.055 + 0.001N _{std}
		t _{PHL}	0.055 + 0.002N _{std}	0.038 + 0.001N _{std}	0.027 + 0.001N _{std}
B-Z		t _{PLH}	0.077 + 0.002N _{std}	0.064 + 0.001N _{std}	0.055 + 0.001N _{std}
		t _{PHL}	0.055 + 0.002N _{std}	0.038 + 0.001N _{std}	0.027 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

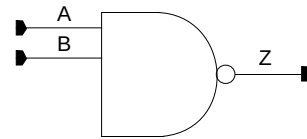
Performance Level	Input Pins			
	A	B	Internal	Cell Units
A	0.276	0.304	0.618	4 cells
B	0.306	0.334	0.689	4 cells
C	0.555	0.545	1.235	4 cells
D	0.773	0.772	1.807	4 cells
E	0.992	0.989	2.371	4 cells
F	1.528	1.606	3.415	4 cells
H	2.931	3.024	6.631	8 cells
I	3.115	3.194	7.011	8 cells
J	3.578	3.543	8.408	8 cells
K	4.552	4.632	10.956	11 cells
L	5.630	5.618	13.310	12 cells
M	7.175	7.136	16.806	16 cells

Cell: NAND2BAL

Function: Balanced 2-Way NAND

Description:

Balanced rising and falling delays. A to Z delay equals B to Z delay.



Boolean Expression: $Z = \overline{A \bullet B}$

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.070 + 0.009N _{std}	0.058 + 0.006N _{std}	0.049 + 0.005N _{std}
		t _{PHL}	0.065 + 0.011N _{std}	0.045 + 0.007N _{std}	0.033 + 0.005N _{std}
B-Z		t _{PLH}	0.070 + 0.009N _{std}	0.058 + 0.006N _{std}	0.049 + 0.005N _{std}
		t _{PHL}	0.065 + 0.011N _{std}	0.045 + 0.007N _{std}	0.033 + 0.005N _{std}
A-Z	H	t _{PLH}	0.070 + 0.006N _{std}	0.058 + 0.004N _{std}	0.049 + 0.003N _{std}
		t _{PHL}	0.064 + 0.007N _{std}	0.045 + 0.004N _{std}	0.034 + 0.003N _{std}
B-Z		t _{PLH}	0.069 + 0.006N _{std}	0.058 + 0.004N _{std}	0.049 + 0.003N _{std}
		t _{PHL}	0.064 + 0.007N _{std}	0.045 + 0.004N _{std}	0.034 + 0.003N _{std}
A-Z	J	t _{PLH}	0.070 + 0.003N _{std}	0.059 + 0.002N _{std}	0.050 + 0.001N _{std}
		t _{PHL}	0.065 + 0.004N _{std}	0.046 + 0.002N _{std}	0.035 + 0.002N _{std}
B-Z		t _{PLH}	0.070 + 0.003N _{std}	0.059 + 0.002N _{std}	0.049 + 0.001N _{std}
		t _{PHL}	0.065 + 0.004N _{std}	0.046 + 0.002N _{std}	0.035 + 0.002N _{std}
A-Z	L	t _{PLH}	0.071 + 0.002N _{std}	0.059 + 0.001N _{std}	0.050 + 0.001N _{std}
		t _{PHL}	0.065 + 0.002N _{std}	0.046 + 0.001N _{std}	0.035 + 0.001N _{std}
B-Z		t _{PLH}	0.070 + 0.002N _{std}	0.059 + 0.001N _{std}	0.050 + 0.001N _{std}
		t _{PHL}	0.065 + 0.002N _{std}	0.046 + 0.001N _{std}	0.035 + 0.001N _{std}



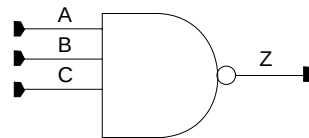
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level			
	E	H	J	L
A	1.228	1.866	3.732	5.548
B	1.223	1.871	3.765	5.603
Internal	2.968	4.612	9.216	13.651
Cell Units	5 cells	5 cells	10 cells	15 cells

Cell: NAND3

Function: 3-Way NAND

Boolean Expression: $Z = \overline{A \bullet B \bullet C}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	A	t _{PLH}	0.104 + 0.085N _{std}	0.080 + 0.054N _{std}	0.064 + 0.037N _{std}
		t _{PHL}	0.080 + 0.075N _{std}	0.051 + 0.044N _{std}	0.034 + 0.030N _{std}
C-Z		t _{PLH}	0.126 + 0.085N _{std}	0.096 + 0.054N _{std}	0.076 + 0.036N _{std}
		t _{PHL}	0.076 + 0.075N _{std}	0.046 + 0.044N _{std}	0.027 + 0.030N _{std}
A-Z	B	t _{PLH}	0.093 + 0.053N _{std}	0.073 + 0.035N _{std}	0.060 + 0.025N _{std}
		t _{PHL}	0.067 + 0.044N _{std}	0.043 + 0.027N _{std}	0.029 + 0.019N _{std}
C-Z		t _{PLH}	0.120 + 0.052N _{std}	0.092 + 0.035N _{std}	0.074 + 0.024N _{std}
		t _{PHL}	0.067 + 0.044N _{std}	0.040 + 0.027N _{std}	0.024 + 0.019N _{std}
A-Z	C	t _{PLH}	0.078 + 0.022N _{std}	0.064 + 0.015N _{std}	0.053 + 0.012N _{std}
		t _{PHL}	0.070 + 0.024N _{std}	0.047 + 0.015N _{std}	0.033 + 0.011N _{std}
C-Z		t _{PLH}	0.099 + 0.022N _{std}	0.079 + 0.015N _{std}	0.065 + 0.011N _{std}
		t _{PHL}	0.070 + 0.024N _{std}	0.043 + 0.015N _{std}	0.027 + 0.011N _{std}
A-Z	D	t _{PLH}	0.081 + 0.017N _{std}	0.066 + 0.012N _{std}	0.056 + 0.009N _{std}
		t _{PHL}	0.062 + 0.015N _{std}	0.041 + 0.009N _{std}	0.028 + 0.007N _{std}
C-Z		t _{PLH}	0.108 + 0.017N _{std}	0.086 + 0.012N _{std}	0.071 + 0.009N _{std}
		t _{PHL}	0.064 + 0.015N _{std}	0.038 + 0.009N _{std}	0.023 + 0.007N _{std}
A-Z	E	t _{PLH}	0.080 + 0.012N _{std}	0.066 + 0.008N _{std}	0.056 + 0.006N _{std}
		t _{PHL}	0.062 + 0.011N _{std}	0.042 + 0.007N _{std}	0.029 + 0.005N _{std}
C-Z		t _{PLH}	0.107 + 0.012N _{std}	0.085 + 0.008N _{std}	0.071 + 0.006N _{std}
		t _{PHL}	0.063 + 0.011N _{std}	0.039 + 0.007N _{std}	0.024 + 0.005N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	F	t _{PLH}	0.081 + 0.008N _{std}	0.066 + 0.006N _{std}	0.056 + 0.004N _{std}
		t _{PHL}	0.065 + 0.008N _{std}	0.044 + 0.005N _{std}	0.031 + 0.003N _{std}
C-Z		t _{PLH}	0.106 + 0.008N _{std}	0.084 + 0.005N _{std}	0.070 + 0.004N _{std}
		t _{PHL}	0.066 + 0.008N _{std}	0.041 + 0.005N _{std}	0.026 + 0.003N _{std}
A-Z	H	t _{PLH}	0.081 + 0.006N _{std}	0.066 + 0.004N _{std}	0.056 + 0.003N _{std}
		t _{PHL}	0.065 + 0.006N _{std}	0.045 + 0.004N _{std}	0.032 + 0.003N _{std}
C-Z		t _{PLH}	0.106 + 0.006N _{std}	0.084 + 0.004N _{std}	0.070 + 0.003N _{std}
		t _{PHL}	0.066 + 0.006N _{std}	0.041 + 0.004N _{std}	0.026 + 0.003N _{std}
A-Z	I	t _{PLH}	0.084 + 0.004N _{std}	0.068 + 0.003N _{std}	0.058 + 0.002N _{std}
		t _{PHL}	0.061 + 0.003N _{std}	0.041 + 0.002N _{std}	0.029 + 0.002N _{std}
C-Z		t _{PLH}	0.113 + 0.004N _{std}	0.089 + 0.003N _{std}	0.074 + 0.002N _{std}
		t _{PHL}	0.062 + 0.003N _{std}	0.038 + 0.002N _{std}	0.023 + 0.002N _{std}
A-Z	J	t _{PLH}	0.081 + 0.003N _{std}	0.066 + 0.002N _{std}	0.056 + 0.002N _{std}
		t _{PHL}	0.062 + 0.003N _{std}	0.042 + 0.002N _{std}	0.030 + 0.001N _{std}
C-Z		t _{PLH}	0.110 + 0.003N _{std}	0.087 + 0.002N _{std}	0.072 + 0.002N _{std}
		t _{PHL}	0.064 + 0.003N _{std}	0.039 + 0.002N _{std}	0.025 + 0.001N _{std}
A-Z	K	t _{PLH}	0.082 + 0.002N _{std}	0.067 + 0.002N _{std}	0.056 + 0.001N _{std}
		t _{PHL}	0.065 + 0.002N _{std}	0.045 + 0.001N _{std}	0.032 + 0.001N _{std}
C-Z		t _{PLH}	0.108 + 0.002N _{std}	0.085 + 0.002N _{std}	0.071 + 0.001N _{std}
		t _{PHL}	0.066 + 0.002N _{std}	0.041 + 0.001N _{std}	0.026 + 0.001N _{std}

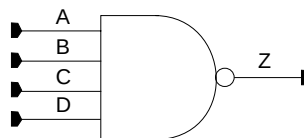
Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins				
	A	B	C	Internal	Cell Units
A	0.252	0.273	0.287	0.653	6 cells
B	0.389	0.375	0.385	0.938	6 cells
C	0.632	0.636	0.642	1.732	6 cells
D	0.890	0.948	0.979	2.472	6 cells
E	1.198	1.263	1.278	3.339	6 cells
F	1.829	1.875	1.886	4.949	10 cells
H	2.252	2.338	2.320	6.294	10 cells
I	3.845	3.845	3.917	10.034	15 cells
J	4.828	4.874	4.902	12.731	17 cells
K	5.777	5.821	5.951	15.482	21 cells

Cell: NAND4

Function: 4-Way NAND

Boolean Expression: $Z = \overline{A \bullet B \bullet C \bullet D}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	A	t _{PLH}	0.102 + 0.053N _{std}	0.079 + 0.035N _{std}	0.063 + 0.025N _{std}
D-Z		t _{PHL}	0.075 + 0.048N _{std}	0.048 + 0.029N _{std}	0.032 + 0.020N _{std}
		t _{PLH}	0.146 + 0.053N _{std}	0.109 + 0.035N _{std}	0.086 + 0.025N _{std}
		t _{PHL}	0.085 + 0.048N _{std}	0.049 + 0.029N _{std}	0.029 + 0.020N _{std}
A-Z	B	t _{PLH}	0.092 + 0.031N _{std}	0.073 + 0.021N _{std}	0.060 + 0.016N _{std}
D-Z		t _{PHL}	0.069 + 0.029N _{std}	0.045 + 0.018N _{std}	0.030 + 0.013N _{std}
		t _{PLH}	0.136 + 0.031N _{std}	0.104 + 0.021N _{std}	0.084 + 0.015N _{std}
		t _{PHL}	0.082 + 0.029N _{std}	0.047 + 0.018N _{std}	0.028 + 0.013N _{std}
A-Z	C	t _{PLH}	0.093 + 0.017N _{std}	0.075 + 0.012N _{std}	0.062 + 0.009N _{std}
D-Z		t _{PHL}	0.066 + 0.015N _{std}	0.043 + 0.009N _{std}	0.029 + 0.006N _{std}
		t _{PLH}	0.141 + 0.017N _{std}	0.109 + 0.012N _{std}	0.089 + 0.009N _{std}
		t _{PHL}	0.080 + 0.015N _{std}	0.046 + 0.009N _{std}	0.027 + 0.006N _{std}
A-Z	D	t _{PLH}	0.092 + 0.013N _{std}	0.074 + 0.009N _{std}	0.062 + 0.007N _{std}
D-Z		t _{PHL}	0.065 + 0.012N _{std}	0.043 + 0.007N _{std}	0.029 + 0.005N _{std}
		t _{PLH}	0.141 + 0.013N _{std}	0.109 + 0.009N _{std}	0.089 + 0.007N _{std}
		t _{PHL}	0.079 + 0.012N _{std}	0.046 + 0.007N _{std}	0.027 + 0.005N _{std}
A-Z	E	t _{PLH}	0.088 + 0.010N _{std}	0.071 + 0.007N _{std}	0.059 + 0.005N _{std}
D-Z		t _{PHL}	0.070 + 0.010N _{std}	0.046 + 0.006N _{std}	0.032 + 0.004N _{std}
		t _{PLH}	0.130 + 0.010N _{std}	0.102 + 0.007N _{std}	0.083 + 0.005N _{std}
		t _{PHL}	0.086 + 0.010N _{std}	0.050 + 0.006N _{std}	0.030 + 0.004N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	F	t _{PLH}	0.086 + 0.007N _{std}	0.070 + 0.005N _{std}	0.058 + 0.003N _{std}
		t _{PHL}	0.070 + 0.007N _{std}	0.047 + 0.004N _{std}	0.033 + 0.003N _{std}
D-Z		t _{PLH}	0.128 + 0.007N _{std}	0.100 + 0.005N _{std}	0.082 + 0.003N _{std}
		t _{PHL}	0.086 + 0.007N _{std}	0.050 + 0.004N _{std}	0.031 + 0.003N _{std}

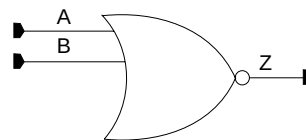
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level					
	A	B	C	D	E	F
A	0.426	0.589	1.161	1.385	1.622	2.275
B	0.419	0.575	1.119	1.351	1.610	2.264
C	0.400	0.583	1.071	1.307	1.629	2.300
D	0.405	0.582	1.152	1.384	1.655	2.341
Internal	1.127	1.711	3.228	3.951	4.926	7.078
Cell Units	6 cells	6 cells	10 cells	10 cells	14 cells	14 cells

Cell: NOR2

Function: 2-Way NOR

Boolean Expression: $Z = \overline{A + B}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	A	t _{PLH}	0.112 + 0.127N _{std}	0.083 + 0.081N _{std}	0.067 + 0.055N _{std}
		t _{PHL}	0.045 + 0.038N _{std}	0.029 + 0.026N _{std}	0.015 + 0.021N _{std}
B-Z		t _{PLH}	0.110 + 0.127N _{std}	0.078 + 0.082N _{std}	0.060 + 0.056N _{std}
		t _{PHL}	0.051 + 0.037N _{std}	0.034 + 0.026N _{std}	0.020 + 0.020N _{std}
A-Z	B	t _{PLH}	0.081 + 0.061N _{std}	0.064 + 0.041N _{std}	0.052 + 0.029N _{std}
		t _{PHL}	0.060 + 0.035N _{std}	0.043 + 0.023N _{std}	0.029 + 0.017N _{std}
B-Z		t _{PLH}	0.082 + 0.061N _{std}	0.061 + 0.041N _{std}	0.046 + 0.029N _{std}
		t _{PHL}	0.073 + 0.035N _{std}	0.051 + 0.023N _{std}	0.037 + 0.017N _{std}
A-Z	C	t _{PLH}	0.069 + 0.029N _{std}	0.055 + 0.020N _{std}	0.046 + 0.015N _{std}
		t _{PHL}	0.061 + 0.020N _{std}	0.044 + 0.014N _{std}	0.033 + 0.010N _{std}
B-Z		t _{PLH}	0.072 + 0.029N _{std}	0.054 + 0.020N _{std}	0.041 + 0.015N _{std}
		t _{PHL}	0.077 + 0.020N _{std}	0.056 + 0.013N _{std}	0.042 + 0.010N _{std}
A-Z	D	t _{PLH}	0.067 + 0.019N _{std}	0.054 + 0.013N _{std}	0.045 + 0.010N _{std}
		t _{PHL}	0.061 + 0.013N _{std}	0.045 + 0.009N _{std}	0.034 + 0.007N _{std}
B-Z		t _{PLH}	0.071 + 0.019N _{std}	0.053 + 0.013N _{std}	0.040 + 0.010N _{std}
		t _{PHL}	0.078 + 0.013N _{std}	0.057 + 0.009N _{std}	0.044 + 0.007N _{std}
A-Z	E	t _{PLH}	0.066 + 0.014N _{std}	0.053 + 0.010N _{std}	0.044 + 0.007N _{std}
		t _{PHL}	0.062 + 0.010N _{std}	0.046 + 0.007N _{std}	0.036 + 0.005N _{std}
B-Z		t _{PLH}	0.070 + 0.014N _{std}	0.052 + 0.010N _{std}	0.040 + 0.007N _{std}
		t _{PHL}	0.079 + 0.010N _{std}	0.058 + 0.007N _{std}	0.046 + 0.005N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	F	t _{PLH}	0.070 + 0.010N _{std}	0.056 + 0.007N _{std}	0.046 + 0.005N _{std}
		t _{PHL}	0.062 + 0.007N _{std}	0.046 + 0.004N _{std}	0.035 + 0.003N _{std}
B-Z		t _{PLH}	0.073 + 0.010N _{std}	0.055 + 0.007N _{std}	0.042 + 0.005N _{std}
		t _{PHL}	0.079 + 0.006N _{std}	0.058 + 0.004N _{std}	0.045 + 0.003N _{std}
A-Z	H	t _{PLH}	0.068 + 0.007N _{std}	0.055 + 0.005N _{std}	0.046 + 0.004N _{std}
		t _{PHL}	0.063 + 0.005N _{std}	0.047 + 0.004N _{std}	0.036 + 0.003N _{std}
B-Z		t _{PLH}	0.072 + 0.007N _{std}	0.054 + 0.005N _{std}	0.041 + 0.004N _{std}
		t _{PHL}	0.079 + 0.005N _{std}	0.058 + 0.003N _{std}	0.046 + 0.003N _{std}
A-Z	I	t _{PLH}	0.067 + 0.005N _{std}	0.054 + 0.004N _{std}	0.045 + 0.003N _{std}
		t _{PHL}	0.063 + 0.004N _{std}	0.048 + 0.003N _{std}	0.037 + 0.002N _{std}
B-Z		t _{PLH}	0.071 + 0.005N _{std}	0.053 + 0.004N _{std}	0.040 + 0.003N _{std}
		t _{PHL}	0.080 + 0.004N _{std}	0.060 + 0.003N _{std}	0.047 + 0.002N _{std}
A-Z	J	t _{PLH}	0.068 + 0.003N _{std}	0.054 + 0.002N _{std}	0.044 + 0.002N _{std}
		t _{PHL}	0.069 + 0.002N _{std}	0.052 + 0.002N _{std}	0.041 + 0.001N _{std}
B-Z		t _{PLH}	0.070 + 0.003N _{std}	0.054 + 0.002N _{std}	0.042 + 0.002N _{std}
		t _{PHL}	0.075 + 0.003N _{std}	0.056 + 0.002N _{std}	0.045 + 0.001N _{std}



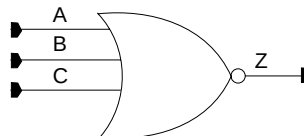
Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins			
	A	B	Internal	Cell Units
A	0.307	0.326	0.608	4 cells
B	0.404	0.416	0.860	4 cells
C	0.648	0.675	1.510	4 cells
D	0.944	1.036	2.211	4 cells
E	1.214	1.308	2.903	4 cells
F	1.878	1.977	4.427	7 cells
H	2.331	2.440	5.602	7 cells
I	3.155	3.326	7.589	8 cells
J	4.864	4.973	11.432	12 cells

Cell: NOR3

Function: 3-Way NOR

Boolean Expression: $Z = \overline{A + B + C}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	A	t _{PLH}	0.099 + 0.074N _{std}	0.075 + 0.049N _{std}	0.060 + 0.035N _{std}
		t _{PHL}	0.071 + 0.035N _{std}	0.049 + 0.023N _{std}	0.033 + 0.018N _{std}
C-Z		t _{PLH}	0.123 + 0.074N _{std}	0.084 + 0.050N _{std}	0.060 + 0.035N _{std}
		t _{PHL}	0.093 + 0.035N _{std}	0.064 + 0.023N _{std}	0.046 + 0.017N _{std}
A-Z	B	t _{PLH}	0.089 + 0.050N _{std}	0.068 + 0.033N _{std}	0.055 + 0.024N _{std}
		t _{PHL}	0.068 + 0.024N _{std}	0.047 + 0.017N _{std}	0.033 + 0.013N _{std}
C-Z		t _{PLH}	0.115 + 0.050N _{std}	0.079 + 0.033N _{std}	0.056 + 0.024N _{std}
		t _{PHL}	0.092 + 0.025N _{std}	0.065 + 0.017N _{std}	0.047 + 0.013N _{std}
A-Z	C	t _{PLH}	0.078 + 0.024N _{std}	0.060 + 0.017N _{std}	0.048 + 0.012N _{std}
		t _{PHL}	0.079 + 0.016N _{std}	0.057 + 0.011N _{std}	0.043 + 0.008N _{std}
C-Z		t _{PLH}	0.109 + 0.024N _{std}	0.075 + 0.016N _{std}	0.051 + 0.012N _{std}
		t _{PHL}	0.116 + 0.016N _{std}	0.082 + 0.011N _{std}	0.063 + 0.008N _{std}
A-Z	D	t _{PLH}	0.076 + 0.017N _{std}	0.059 + 0.011N _{std}	0.048 + 0.008N _{std}
		t _{PHL}	0.075 + 0.011N _{std}	0.055 + 0.007N _{std}	0.042 + 0.006N _{std}
C-Z		t _{PLH}	0.107 + 0.017N _{std}	0.073 + 0.011N _{std}	0.051 + 0.008N _{std}
		t _{PHL}	0.111 + 0.011N _{std}	0.079 + 0.007N _{std}	0.062 + 0.005N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.076 + 0.013N _{std}	0.060 + 0.009N _{std}	0.049 + 0.006N _{std}
		t _{PHL}	0.071 + 0.008N _{std}	0.052 + 0.005N _{std}	0.039 + 0.004N _{std}
C-Z		t _{PLH}	0.105 + 0.013N _{std}	0.073 + 0.009N _{std}	0.051 + 0.006N _{std}
		t _{PHL}	0.103 + 0.008N _{std}	0.074 + 0.005N _{std}	0.057 + 0.004N _{std}
A-Z	F	t _{PLH}	0.073 + 0.008N _{std}	0.058 + 0.005N _{std}	0.048 + 0.004N _{std}
		t _{PHL}	0.070 + 0.005N _{std}	0.051 + 0.003N _{std}	0.040 + 0.002N _{std}
C-Z		t _{PLH}	0.103 + 0.008N _{std}	0.071 + 0.005N _{std}	0.050 + 0.004N _{std}
		t _{PHL}	0.103 + 0.005N _{std}	0.074 + 0.003N _{std}	0.058 + 0.002N _{std}

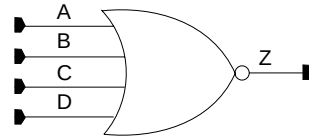
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level					
	A	B	C	D	E	F
A	0.449	0.603	1.123	1.521	2.007	3.042
B	0.442	0.592	1.062	1.471	2.032	3.149
C	0.440	0.593	1.117	1.538	2.068	3.275
Internal	1.128	1.555	2.865	4.069	5.308	8.359
Cell Units	5 cells	5 cells	8 cells	8 cells	10 cells	11 cells

Cell: NOR4

Function: 4-Way NOR

Boolean Expression: $Z = \overline{A + B + C + D}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	A	t _{PLH}	0.095 + 0.075N _{std}	0.073 + 0.049N _{std}	0.059 + 0.035N _{std}
		t _{PHL}	0.078 + 0.035N _{std}	0.054 + 0.023N _{std}	0.037 + 0.018N _{std}
D-Z		t _{PLH}	0.160 + 0.075N _{std}	0.107 + 0.050N _{std}	0.074 + 0.036N _{std}
		t _{PHL}	0.115 + 0.037N _{std}	0.079 + 0.024N _{std}	0.057 + 0.018N _{std}
A-Z	B	t _{PLH}	0.084 + 0.043N _{std}	0.065 + 0.029N _{std}	0.053 + 0.021N _{std}
		t _{PHL}	0.076 + 0.022N _{std}	0.053 + 0.015N _{std}	0.039 + 0.012N _{std}
D-Z		t _{PLH}	0.151 + 0.044N _{std}	0.101 + 0.030N _{std}	0.069 + 0.021N _{std}
		t _{PHL}	0.119 + 0.023N _{std}	0.082 + 0.016N _{std}	0.061 + 0.012N _{std}
A-Z	C	t _{PLH}	0.081 + 0.021N _{std}	0.063 + 0.014N _{std}	0.051 + 0.010N _{std}
		t _{PHL}	0.078 + 0.011N _{std}	0.056 + 0.007N _{std}	0.042 + 0.006N _{std}
D-Z		t _{PLH}	0.154 + 0.021N _{std}	0.102 + 0.014N _{std}	0.070 + 0.010N _{std}
		t _{PHL}	0.124 + 0.011N _{std}	0.088 + 0.007N _{std}	0.067 + 0.006N _{std}
A-Z	D	t _{PLH}	0.080 + 0.010N _{std}	0.062 + 0.007N _{std}	0.050 + 0.005N _{std}
		t _{PHL}	0.080 + 0.005N _{std}	0.058 + 0.004N _{std}	0.044 + 0.003N _{std}
D-Z		t _{PLH}	0.151 + 0.010N _{std}	0.100 + 0.007N _{std}	0.069 + 0.005N _{std}
		t _{PHL}	0.126 + 0.006N _{std}	0.090 + 0.004N _{std}	0.069 + 0.003N _{std}



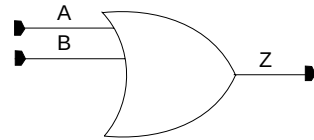
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level			
	A	B	C	D
A	0.485	0.732	1.611	3.167
B	0.559	0.792	1.590	3.158
C	0.531	0.768	1.556	3.161
D	0.506	0.766	1.581	3.118
Internal	1.454	2.290	4.801	9.398
Cell Units	5 cells	5 cells	10 cells	17 cells

Cell: OR2

Function: 2-Way OR

Boolean Expression: $Z = A + B$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	B	t _{PLH}	0.100 + 0.078N _{std}	0.063 + 0.050N _{std}	0.038 + 0.034N _{std}
		t _{PHL}	0.174 + 0.037N _{std}	0.120 + 0.024N _{std}	0.090 + 0.018N _{std}
B-Z		t _{PLH}	0.109 + 0.077N _{std}	0.069 + 0.050N _{std}	0.044 + 0.034N _{std}
		t _{PHL}	0.172 + 0.037N _{std}	0.116 + 0.024N _{std}	0.084 + 0.018N _{std}
A-Z	C	t _{PLH}	0.103 + 0.036N _{std}	0.067 + 0.024N _{std}	0.045 + 0.018N _{std}
		t _{PHL}	0.163 + 0.026N _{std}	0.115 + 0.017N _{std}	0.088 + 0.013N _{std}
B-Z		t _{PLH}	0.115 + 0.036N _{std}	0.076 + 0.024N _{std}	0.053 + 0.017N _{std}
		t _{PHL}	0.163 + 0.026N _{std}	0.112 + 0.017N _{std}	0.082 + 0.013N _{std}
A-Z	D	t _{PLH}	0.114 + 0.023N _{std}	0.075 + 0.016N _{std}	0.052 + 0.011N _{std}
		t _{PHL}	0.172 + 0.017N _{std}	0.121 + 0.011N _{std}	0.092 + 0.008N _{std}
B-Z		t _{PLH}	0.126 + 0.023N _{std}	0.085 + 0.016N _{std}	0.060 + 0.011N _{std}
		t _{PHL}	0.171 + 0.017N _{std}	0.118 + 0.011N _{std}	0.086 + 0.008N _{std}
A-Z	E	t _{PLH}	0.110 + 0.016N _{std}	0.073 + 0.011N _{std}	0.051 + 0.008N _{std}
		t _{PHL}	0.166 + 0.013N _{std}	0.118 + 0.008N _{std}	0.090 + 0.006N _{std}
B-Z		t _{PLH}	0.123 + 0.016N _{std}	0.083 + 0.011N _{std}	0.060 + 0.008N _{std}
		t _{PHL}	0.167 + 0.013N _{std}	0.115 + 0.008N _{std}	0.084 + 0.006N _{std}
A-Z	F	t _{PLH}	0.109 + 0.011N _{std}	0.074 + 0.007N _{std}	0.052 + 0.006N _{std}
		t _{PHL}	0.169 + 0.008N _{std}	0.121 + 0.005N _{std}	0.092 + 0.004N _{std}
B-Z		t _{PLH}	0.123 + 0.011N _{std}	0.084 + 0.007N _{std}	0.060 + 0.006N _{std}
		t _{PHL}	0.169 + 0.008N _{std}	0.118 + 0.005N _{std}	0.086 + 0.004N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	H	t _{PLH}	0.109 + 0.008N _{std}	0.074 + 0.006N _{std}	0.052 + 0.004N _{std}
		t _{PHL}	0.184 + 0.005N _{std}	0.132 + 0.003N _{std}	0.100 + 0.002N _{std}
B-Z		t _{PLH}	0.121 + 0.008N _{std}	0.083 + 0.006N _{std}	0.059 + 0.004N _{std}
		t _{PHL}	0.184 + 0.005N _{std}	0.128 + 0.003N _{std}	0.094 + 0.002N _{std}
A-Z	I	t _{PLH}	0.109 + 0.005N _{std}	0.075 + 0.004N _{std}	0.054 + 0.003N _{std}
		t _{PHL}	0.169 + 0.004N _{std}	0.122 + 0.003N _{std}	0.093 + 0.002N _{std}
B-Z		t _{PLH}	0.124 + 0.005N _{std}	0.085 + 0.004N _{std}	0.063 + 0.003N _{std}
		t _{PHL}	0.171 + 0.004N _{std}	0.119 + 0.003N _{std}	0.087 + 0.002N _{std}
A-Z	J	t _{PLH}	0.113 + 0.004N _{std}	0.077 + 0.003N _{std}	0.055 + 0.002N _{std}
		t _{PHL}	0.182 + 0.002N _{std}	0.130 + 0.002N _{std}	0.099 + 0.001N _{std}
B-Z		t _{PLH}	0.125 + 0.004N _{std}	0.086 + 0.003N _{std}	0.063 + 0.002N _{std}
		t _{PHL}	0.183 + 0.002N _{std}	0.128 + 0.002N _{std}	0.093 + 0.001N _{std}
A-Z	K	t _{PLH}	0.127 + 0.003N _{std}	0.088 + 0.002N _{std}	0.064 + 0.001N _{std}
		t _{PHL}	0.187 + 0.002N _{std}	0.134 + 0.001N _{std}	0.100 + 0.001N _{std}
B-Z		t _{PLH}	0.142 + 0.003N _{std}	0.099 + 0.002N _{std}	0.073 + 0.001N _{std}
		t _{PHL}	0.189 + 0.002N _{std}	0.131 + 0.001N _{std}	0.095 + 0.001N _{std}

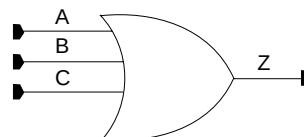
Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins			
	A	B	Internal	Cell Units
B	0.310	0.325	1.149	6 cells
C	0.372	0.372	1.508	6 cells
D	0.386	0.389	1.848	6 cells
E	0.464	0.471	2.380	6 cells
F	0.578	0.588	3.324	6 cells
H	0.679	0.682	4.375	6 cells
I	0.917	0.933	5.867	6 cells
J	1.218	1.275	8.481	8 cells
K	1.346	1.416	10.454	8 cells

Cell: OR3

Function: 3-Way OR

Boolean Expression: $Z = A + B + C$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	B	t _{PLH}	0.114 + 0.070N _{std}	0.073 + 0.046N _{std}	0.047 + 0.031N _{std}
		t _{PHL}	0.187 + 0.038N _{std}	0.128 + 0.025N _{std}	0.095 + 0.018N _{std}
C-Z		t _{PLH}	0.136 + 0.070N _{std}	0.089 + 0.045N _{std}	0.060 + 0.031N _{std}
		t _{PHL}	0.210 + 0.038N _{std}	0.137 + 0.025N _{std}	0.094 + 0.018N _{std}
A-Z	C	t _{PLH}	0.116 + 0.035N _{std}	0.076 + 0.024N _{std}	0.051 + 0.017N _{std}
		t _{PHL}	0.194 + 0.026N _{std}	0.134 + 0.017N _{std}	0.101 + 0.012N _{std}
C-Z		t _{PLH}	0.142 + 0.035N _{std}	0.094 + 0.024N _{std}	0.066 + 0.017N _{std}
		t _{PHL}	0.217 + 0.026N _{std}	0.144 + 0.017N _{std}	0.100 + 0.012N _{std}
A-Z	D	t _{PLH}	0.129 + 0.023N _{std}	0.086 + 0.016N _{std}	0.059 + 0.012N _{std}
		t _{PHL}	0.191 + 0.017N _{std}	0.134 + 0.011N _{std}	0.100 + 0.008N _{std}
C-Z		t _{PLH}	0.161 + 0.023N _{std}	0.107 + 0.016N _{std}	0.076 + 0.011N _{std}
		t _{PHL}	0.216 + 0.017N _{std}	0.144 + 0.011N _{std}	0.100 + 0.008N _{std}
A-Z	E	t _{PLH}	0.129 + 0.017N _{std}	0.086 + 0.012N _{std}	0.060 + 0.009N _{std}
		t _{PHL}	0.194 + 0.013N _{std}	0.136 + 0.008N _{std}	0.102 + 0.006N _{std}
C-Z		t _{PLH}	0.161 + 0.017N _{std}	0.108 + 0.012N _{std}	0.078 + 0.009N _{std}
		t _{PHL}	0.219 + 0.013N _{std}	0.146 + 0.008N _{std}	0.102 + 0.006N _{std}
A-Z	F	t _{PLH}	0.130 + 0.011N _{std}	0.089 + 0.007N _{std}	0.064 + 0.005N _{std}
		t _{PHL}	0.191 + 0.008N _{std}	0.136 + 0.005N _{std}	0.102 + 0.004N _{std}
C-Z		t _{PLH}	0.165 + 0.011N _{std}	0.112 + 0.007N _{std}	0.083 + 0.005N _{std}
		t _{PHL}	0.217 + 0.008N _{std}	0.146 + 0.005N _{std}	0.103 + 0.004N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	H	t _{PLH}	0.126 + 0.008N _{std}	0.086 + 0.006N _{std}	0.062 + 0.004N _{std}
		t _{PHL}	0.190 + 0.006N _{std}	0.134 + 0.004N _{std}	0.101 + 0.003N _{std}
C-Z		t _{PLH}	0.159 + 0.008N _{std}	0.109 + 0.006N _{std}	0.081 + 0.004N _{std}
		t _{PHL}	0.216 + 0.006N _{std}	0.146 + 0.004N _{std}	0.102 + 0.003N _{std}
A-Z	I	t _{PLH}	0.148 + 0.006N _{std}	0.103 + 0.004N _{std}	0.075 + 0.003N _{std}
		t _{PHL}	0.213 + 0.004N _{std}	0.149 + 0.003N _{std}	0.110 + 0.002N _{std}
C-Z		t _{PLH}	0.185 + 0.006N _{std}	0.127 + 0.004N _{std}	0.094 + 0.003N _{std}
		t _{PHL}	0.240 + 0.004N _{std}	0.161 + 0.003N _{std}	0.111 + 0.002N _{std}
A-Z	J	t _{PLH}	0.144 + 0.004N _{std}	0.099 + 0.003N _{std}	0.073 + 0.002N _{std}
		t _{PHL}	0.209 + 0.003N _{std}	0.147 + 0.002N _{std}	0.109 + 0.001N _{std}
C-Z		t _{PLH}	0.178 + 0.004N _{std}	0.123 + 0.003N _{std}	0.092 + 0.002N _{std}
		t _{PHL}	0.237 + 0.003N _{std}	0.159 + 0.002N _{std}	0.110 + 0.001N _{std}
A-Z	K	t _{PLH}	0.151 + 0.003N _{std}	0.104 + 0.002N _{std}	0.077 + 0.001N _{std}
		t _{PHL}	0.217 + 0.002N _{std}	0.152 + 0.001N _{std}	0.113 + 0.001N _{std}
C-Z		t _{PLH}	0.186 + 0.003N _{std}	0.128 + 0.002N _{std}	0.096 + 0.001N _{std}
		t _{PHL}	0.245 + 0.002N _{std}	0.164 + 0.001N _{std}	0.114 + 0.001N _{std}



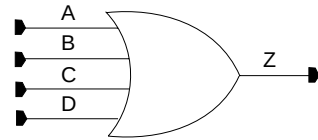
Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins				
	A	B	C	Internal	Cell Units
B	0.378	0.381	0.383	1.436	8 cells
C	0.401	0.406	0.411	1.761	8 cells
D	0.436	0.444	0.453	2.188	8 cells
E	0.490	0.498	0.510	2.661	8 cells
F	0.665	0.650	0.656	3.796	8 cells
H	0.828	0.816	0.825	4.866	8 cells
I	1.041	0.966	1.006	6.750	13 cells
J	1.309	1.240	1.285	8.751	13 cells
K	1.600	1.539	1.593	11.878	13 cells

Cell: OR4

Function: 4-Way OR

Boolean Expression: $Z = A + B + C + D$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	B	t _{PLH}	0.116 + 0.070N _{std}	0.075 + 0.045N _{std}	0.049 + 0.031N _{std}
		t _{PHL}	0.176 + 0.040N _{std}	0.121 + 0.026N _{std}	0.091 + 0.019N _{std}
D-Z		t _{PLH}	0.151 + 0.070N _{std}	0.099 + 0.046N _{std}	0.069 + 0.031N _{std}
		t _{PHL}	0.241 + 0.039N _{std}	0.156 + 0.025N _{std}	0.105 + 0.019N _{std}
A-Z	C	t _{PLH}	0.120 + 0.033N _{std}	0.080 + 0.022N _{std}	0.056 + 0.016N _{std}
		t _{PHL}	0.171 + 0.026N _{std}	0.120 + 0.017N _{std}	0.091 + 0.012N _{std}
D-Z		t _{PLH}	0.171 + 0.033N _{std}	0.114 + 0.023N _{std}	0.082 + 0.016N _{std}
		t _{PHL}	0.238 + 0.026N _{std}	0.155 + 0.017N _{std}	0.106 + 0.012N _{std}
A-Z	D	t _{PLH}	0.122 + 0.022N _{std}	0.082 + 0.015N _{std}	0.058 + 0.011N _{std}
		t _{PHL}	0.174 + 0.017N _{std}	0.123 + 0.012N _{std}	0.094 + 0.009N _{std}
D-Z		t _{PLH}	0.175 + 0.022N _{std}	0.118 + 0.015N _{std}	0.086 + 0.011N _{std}
		t _{PHL}	0.241 + 0.017N _{std}	0.158 + 0.012N _{std}	0.109 + 0.009N _{std}
A-Z	E	t _{PLH}	0.125 + 0.016N _{std}	0.085 + 0.011N _{std}	0.060 + 0.008N _{std}
		t _{PHL}	0.179 + 0.013N _{std}	0.126 + 0.008N _{std}	0.096 + 0.006N _{std}
D-Z		t _{PLH}	0.179 + 0.016N _{std}	0.121 + 0.011N _{std}	0.089 + 0.008N _{std}
		t _{PHL}	0.245 + 0.013N _{std}	0.161 + 0.008N _{std}	0.111 + 0.006N _{std}
A-Z	F	t _{PLH}	0.101 + 0.010N _{std}	0.068 + 0.007N _{std}	0.047 + 0.005N _{std}
		t _{PHL}	0.155 + 0.007N _{std}	0.111 + 0.004N _{std}	0.085 + 0.003N _{std}
D-Z		t _{PLH}	0.128 + 0.010N _{std}	0.087 + 0.007N _{std}	0.061 + 0.005N _{std}
		t _{PHL}	0.163 + 0.007N _{std}	0.112 + 0.004N _{std}	0.082 + 0.003N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	H	t _{PLH}	0.106 + 0.007N _{std}	0.072 + 0.005N _{std}	0.050 + 0.004N _{std}
		t _{PHL}	0.172 + 0.006N _{std}	0.121 + 0.004N _{std}	0.092 + 0.003N _{std}
D-Z		t _{PLH}	0.130 + 0.007N _{std}	0.088 + 0.005N _{std}	0.063 + 0.004N _{std}
		t _{PHL}	0.179 + 0.006N _{std}	0.122 + 0.004N _{std}	0.089 + 0.003N _{std}
A-Z	I	t _{PLH}	0.134 + 0.005N _{std}	0.091 + 0.003N _{std}	0.065 + 0.002N _{std}
		t _{PHL}	0.197 + 0.003N _{std}	0.139 + 0.002N _{std}	0.104 + 0.001N _{std}
D-Z		t _{PLH}	0.160 + 0.005N _{std}	0.108 + 0.003N _{std}	0.078 + 0.002N _{std}
		t _{PHL}	0.205 + 0.003N _{std}	0.140 + 0.002N _{std}	0.101 + 0.001N _{std}
A-Z	J	t _{PLH}	0.139 + 0.003N _{std}	0.095 + 0.002N _{std}	0.069 + 0.002N _{std}
		t _{PHL}	0.209 + 0.002N _{std}	0.147 + 0.002N _{std}	0.109 + 0.001N _{std}
D-Z		t _{PLH}	0.165 + 0.003N _{std}	0.112 + 0.002N _{std}	0.082 + 0.002N _{std}
		t _{PHL}	0.217 + 0.002N _{std}	0.148 + 0.002N _{std}	0.106 + 0.001N _{std}
A-Z	K	t _{PLH}	0.151 + 0.003N _{std}	0.104 + 0.002N _{std}	0.076 + 0.001N _{std}
		t _{PHL}	0.218 + 0.002N _{std}	0.153 + 0.001N _{std}	0.113 + 0.001N _{std}
D-Z		t _{PLH}	0.177 + 0.003N _{std}	0.120 + 0.002N _{std}	0.088 + 0.001N _{std}
		t _{PHL}	0.226 + 0.002N _{std}	0.154 + 0.001N _{std}	0.110 + 0.001N _{std}

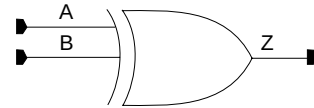
Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins					
	A	B	C	D	Internal	Cell Units
B	0.511	0.526	0.519	0.481	1.871	8 cells
C	0.600	0.623	0.620	0.585	2.449	8 cells
D	0.689	0.680	0.678	0.679	3.026	8 cells
E	0.762	0.759	0.758	0.757	3.622	8 cells
F	0.942	0.939	0.939	0.941	5.369	10 cells
H	0.940	0.937	0.938	0.940	6.083	10 cells
I	0.983	0.982	0.979	0.979	8.971	14 cells
J	1.204	1.268	1.204	1.278	12.252	20 cells
K	1.260	1.331	1.260	1.341	14.250	20 cells

Cell: XOR2

Function: 2-Way XOR

Boolean Expression: $Z = A \oplus B$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	A	t _{PLH}	0.131 + 0.060N _{std}	0.086 + 0.040N _{std}	0.058 + 0.029N _{std}
		t _{PHL}	0.140 + 0.040N _{std}	0.098 + 0.024N _{std}	0.073 + 0.017N _{std}
B-Z		t _{PLH}	0.146 + 0.060N _{std}	0.107 + 0.040N _{std}	0.082 + 0.029N _{std}
		t _{PHL}	0.138 + 0.039N _{std}	0.096 + 0.024N _{std}	0.072 + 0.017N _{std}
A-Z	B	t _{PLH}	0.129 + 0.049N _{std}	0.085 + 0.033N _{std}	0.058 + 0.023N _{std}
		t _{PHL}	0.136 + 0.036N _{std}	0.095 + 0.022N _{std}	0.071 + 0.016N _{std}
B-Z		t _{PLH}	0.137 + 0.048N _{std}	0.101 + 0.033N _{std}	0.078 + 0.024N _{std}
		t _{PHL}	0.134 + 0.036N _{std}	0.094 + 0.022N _{std}	0.070 + 0.016N _{std}
A-Z	C	t _{PLH}	0.119 + 0.024N _{std}	0.079 + 0.016N _{std}	0.056 + 0.012N _{std}
		t _{PHL}	0.125 + 0.019N _{std}	0.089 + 0.012N _{std}	0.067 + 0.009N _{std}
B-Z		t _{PLH}	0.124 + 0.024N _{std}	0.092 + 0.017N _{std}	0.073 + 0.012N _{std}
		t _{PHL}	0.123 + 0.019N _{std}	0.087 + 0.012N _{std}	0.065 + 0.009N _{std}
A-Z	D	t _{PLH}	0.190 + 0.024N _{std}	0.130 + 0.016N _{std}	0.096 + 0.011N _{std}
		t _{PHL}	0.203 + 0.018N _{std}	0.132 + 0.011N _{std}	0.089 + 0.008N _{std}
B-Z		t _{PLH}	0.175 + 0.024N _{std}	0.122 + 0.016N _{std}	0.092 + 0.011N _{std}
		t _{PHL}	0.212 + 0.018N _{std}	0.137 + 0.011N _{std}	0.092 + 0.008N _{std}
A-Z	E	t _{PLH}	0.187 + 0.017N _{std}	0.129 + 0.012N _{std}	0.095 + 0.008N _{std}
		t _{PHL}	0.202 + 0.013N _{std}	0.132 + 0.009N _{std}	0.090 + 0.006N _{std}
B-Z		t _{PLH}	0.172 + 0.017N _{std}	0.121 + 0.012N _{std}	0.091 + 0.008N _{std}
		t _{PHL}	0.211 + 0.013N _{std}	0.137 + 0.009N _{std}	0.093 + 0.006N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	F	t _{PLH}	0.182 + 0.011N _{std}	0.126 + 0.007N _{std}	0.093 + 0.005N _{std}
		t _{PHL}	0.199 + 0.008N _{std}	0.131 + 0.006N _{std}	0.090 + 0.004N _{std}
B-Z		t _{PLH}	0.167 + 0.011N _{std}	0.118 + 0.007N _{std}	0.089 + 0.005N _{std}
		t _{PHL}	0.208 + 0.008N _{std}	0.136 + 0.006N _{std}	0.092 + 0.004N _{std}
A-Z	H	t _{PLH}	0.189 + 0.009N _{std}	0.130 + 0.006N _{std}	0.095 + 0.004N _{std}
		t _{PHL}	0.205 + 0.007N _{std}	0.135 + 0.004N _{std}	0.094 + 0.003N _{std}
B-Z		t _{PLH}	0.175 + 0.009N _{std}	0.116 + 0.006N _{std}	0.086 + 0.004N _{std}
		t _{PHL}	0.213 + 0.007N _{std}	0.140 + 0.004N _{std}	0.096 + 0.003N _{std}
A-Z	I	t _{PLH}	0.210 + 0.005N _{std}	0.143 + 0.004N _{std}	0.104 + 0.003N _{std}
		t _{PHL}	0.233 + 0.004N _{std}	0.154 + 0.003N _{std}	0.106 + 0.002N _{std}
B-Z		t _{PLH}	0.195 + 0.005N _{std}	0.129 + 0.004N _{std}	0.095 + 0.003N _{std}
		t _{PHL}	0.241 + 0.004N _{std}	0.158 + 0.003N _{std}	0.108 + 0.002N _{std}
A-Z	J	t _{PLH}	0.235 + 0.004N _{std}	0.159 + 0.003N _{std}	0.116 + 0.002N _{std}
		t _{PHL}	0.270 + 0.003N _{std}	0.178 + 0.002N _{std}	0.123 + 0.001N _{std}
B-Z		t _{PLH}	0.221 + 0.004N _{std}	0.146 + 0.003N _{std}	0.107 + 0.002N _{std}
		t _{PHL}	0.278 + 0.003N _{std}	0.183 + 0.002N _{std}	0.125 + 0.001N _{std}



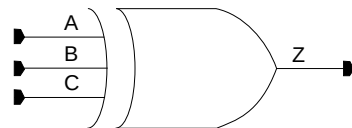
Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins			
	A	B	Internal	Cell Units
A	0.460	0.628	2.070	7 cells
B	0.511	0.690	2.356	7 cells
C	0.855	1.144	4.149	7 cells
D	0.516	0.788	3.367	10 cells
E	0.583	0.896	4.009	10 cells
F	0.758	1.169	5.508	10 cells
H	0.807	1.257	6.150	10 cells
I	0.819	1.277	7.372	10 cells
J	0.819	1.276	9.091	13 cells

Cell: XOR3

Function: 3-Way XOR

Boolean Expression: $Z = A \oplus B \oplus C$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	B	t _{PLH}	0.223 + 0.061N _{std}	0.142 + 0.040N _{std}	0.075 + 0.028N _{std}
		t _{PHL}	0.235 + 0.040N _{std}	0.147 + 0.026N _{std}	0.080 + 0.017N _{std}
C-Z		t _{PLH}	0.133 + 0.061N _{std}	0.092 + 0.040N _{std}	0.068 + 0.028N _{std}
		t _{PHL}	0.158 + 0.038N _{std}	0.103 + 0.025N _{std}	0.070 + 0.018N _{std}
A-Z	C	t _{PLH}	0.230 + 0.031N _{std}	0.152 + 0.021N _{std}	0.100 + 0.016N _{std}
		t _{PHL}	0.261 + 0.023N _{std}	0.168 + 0.015N _{std}	0.113 + 0.010N _{std}
C-Z		t _{PLH}	0.134 + 0.032N _{std}	0.093 + 0.022N _{std}	0.069 + 0.015N _{std}
		t _{PHL}	0.173 + 0.022N _{std}	0.114 + 0.015N _{std}	0.081 + 0.011N _{std}
A-Z	D	t _{PLH}	0.226 + 0.022N _{std}	0.145 + 0.015N _{std}	0.100 + 0.011N _{std}
		t _{PHL}	0.253 + 0.016N _{std}	0.162 + 0.011N _{std}	0.109 + 0.008N _{std}
C-Z		t _{PLH}	0.136 + 0.022N _{std}	0.096 + 0.015N _{std}	0.071 + 0.011N _{std}
		t _{PHL}	0.180 + 0.016N _{std}	0.120 + 0.010N _{std}	0.085 + 0.008N _{std}
A-Z	E	t _{PLH}	0.235 + 0.016N _{std}	0.155 + 0.011N _{std}	0.111 + 0.008N _{std}
		t _{PHL}	0.274 + 0.011N _{std}	0.177 + 0.007N _{std}	0.122 + 0.005N _{std}
C-Z		t _{PLH}	0.146 + 0.016N _{std}	0.102 + 0.011N _{std}	0.075 + 0.008N _{std}
		t _{PHL}	0.193 + 0.010N _{std}	0.128 + 0.007N _{std}	0.090 + 0.005N _{std}
A-Z	F	t _{PLH}	0.244 + 0.010N _{std}	0.161 + 0.007N _{std}	0.116 + 0.005N _{std}
		t _{PHL}	0.285 + 0.005N _{std}	0.189 + 0.003N _{std}	0.133 + 0.003N _{std}
C-Z		t _{PLH}	0.151 + 0.010N _{std}	0.105 + 0.007N _{std}	0.078 + 0.005N _{std}
		t _{PHL}	0.190 + 0.006N _{std}	0.128 + 0.004N _{std}	0.091 + 0.003N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	H	t _{PLH}	0.251 + 0.008N _{std}	0.162 + 0.005N _{std}	0.112 + 0.004N _{std}
		t _{PHL}	0.300 + 0.004N _{std}	0.199 + 0.003N _{std}	0.140 + 0.002N _{std}
C-Z		t _{PLH}	0.158 + 0.008N _{std}	0.110 + 0.005N _{std}	0.081 + 0.004N _{std}
		t _{PHL}	0.212 + 0.005N _{std}	0.142 + 0.003N _{std}	0.101 + 0.002N _{std}
A-Z	I	t _{PLH}	0.279 + 0.005N _{std}	0.179 + 0.004N _{std}	0.125 + 0.003N _{std}
		t _{PHL}	0.335 + 0.003N _{std}	0.222 + 0.002N _{std}	0.154 + 0.001N _{std}
C-Z		t _{PLH}	0.183 + 0.005N _{std}	0.119 + 0.004N _{std}	0.083 + 0.003N _{std}
		t _{PHL}	0.245 + 0.003N _{std}	0.162 + 0.002N _{std}	0.113 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

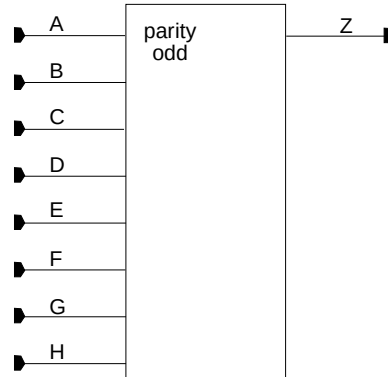
Performance Level	Input Pins				
	A	B	C	Internal	Cell Units
B	1.263	0.886	0.983	5.443	17 cells
C	1.278	0.892	0.982	5.404	17 cells
D	1.276	0.890	1.035	6.014	17 cells
E	1.371	0.985	1.035	6.623	17 cells
F	1.419	0.983	1.360	8.586	17 cells
H	1.420	0.982	1.361	9.226	17 cells
I	1.434	0.987	1.507	12.741	19 cells

Cell: XOR8

Function: 8-Way XOR (8-Bit Parity Odd)

Boolean Expression:

$$Z = A \oplus B \oplus C \oplus D \oplus E \oplus F \oplus G \oplus H$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.542 + 0.018N _{std}	0.335 + 0.012N _{std}	0.215 + 0.009N _{std}
		t _{PHL}	0.587 + 0.013N _{std}	0.365 + 0.009N _{std}	0.234 + 0.006N _{std}
H-Z		t _{PLH}	0.578 + 0.018N _{std}	0.358 + 0.012N _{std}	0.249 + 0.008N _{std}
		t _{PHL}	0.638 + 0.013N _{std}	0.399 + 0.009N _{std}	0.197 + 0.006N _{std}
A-Z	H	t _{PLH}	0.575 + 0.009N _{std}	0.356 + 0.006N _{std}	0.233 + 0.004N _{std}
		t _{PHL}	0.613 + 0.007N _{std}	0.382 + 0.004N _{std}	0.250 + 0.003N _{std}
H-Z		t _{PLH}	0.608 + 0.009N _{std}	0.376 + 0.006N _{std}	0.261 + 0.004N _{std}
		t _{PHL}	0.684 + 0.007N _{std}	0.427 + 0.004N _{std}	0.211 + 0.003N _{std}
A-Z	J	t _{PLH}	0.664 + 0.004N _{std}	0.410 + 0.003N _{std}	0.269 + 0.002N _{std}
		t _{PHL}	0.727 + 0.002N _{std}	0.454 + 0.002N _{std}	0.298 + 0.001N _{std}
H-Z		t _{PLH}	0.707 + 0.004N _{std}	0.437 + 0.003N _{std}	0.302 + 0.002N _{std}
		t _{PHL}	0.811 + 0.002N _{std}	0.508 + 0.002N _{std}	0.263 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

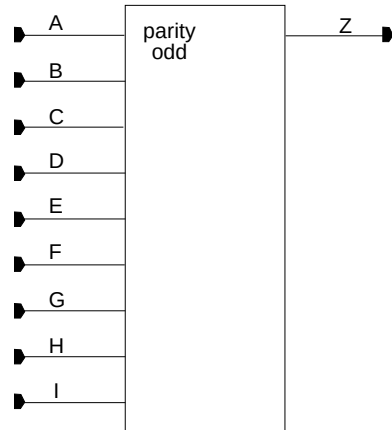
Input Pins	Performance Level		
	E	H	J
A	0.392	0.392	0.392
B	0.488	0.488	0.488
C	0.493	0.493	0.493
D	0.358	0.358	0.358
E	0.355	0.355	0.355
F	0.526	0.526	0.526
G	0.360	0.360	0.360
H	0.534	0.534	0.534
Internal	6.770	8.936	15.423
Cell Units	52 cells	52 cells	59 cells

Cell: XOR9

Function: 9-Way XOR (9-Bit Parity Odd)

Boolean Expression:

$$Z = A \oplus B \oplus C \oplus D \oplus E \oplus F \oplus G \oplus H \oplus I$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	E	t _{PLH}	0.527 + 0.016N _{std}	0.334 + 0.011N _{std}	0.212 + 0.008N _{std}
		t _{PHL}	0.569 + 0.009N _{std}	0.355 + 0.006N _{std}	0.238 + 0.005N _{std}
I-Z		t _{PLH}	0.305 + 0.016N _{std}	0.198 + 0.011N _{std}	0.134 + 0.008N _{std}
		t _{PHL}	0.328 + 0.010N _{std}	0.205 + 0.007N _{std}	0.149 + 0.005N _{std}
A-Z	H	t _{PLH}	0.548 + 0.007N _{std}	0.349 + 0.005N _{std}	0.232 + 0.004N _{std}
		t _{PHL}	0.591 + 0.004N _{std}	0.370 + 0.003N _{std}	0.258 + 0.002N _{std}
I-Z		t _{PLH}	0.325 + 0.007N _{std}	0.209 + 0.005N _{std}	0.141 + 0.004N _{std}
		t _{PHL}	0.350 + 0.005N _{std}	0.221 + 0.003N _{std}	0.161 + 0.002N _{std}
A-Z	J	t _{PLH}	0.636 + 0.004N _{std}	0.404 + 0.003N _{std}	0.269 + 0.002N _{std}
		t _{PHL}	0.697 + 0.002N _{std}	0.434 + 0.002N _{std}	0.301 + 0.001N _{std}
I-Z		t _{PLH}	0.415 + 0.004N _{std}	0.265 + 0.003N _{std}	0.176 + 0.002N _{std}
		t _{PHL}	0.470 + 0.002N _{std}	0.299 + 0.002N _{std}	0.201 + 0.001N _{std}



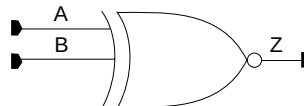
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	J
A	1.266	1.424	1.424
B	0.981	0.982	0.982
C	1.027	1.365	1.365
D	1.268	1.437	1.437
E	0.964	0.964	0.964
F	1.020	1.364	1.364
G	1.273	1.439	1.439
H	0.963	0.964	0.964
I	1.020	1.361	1.361
Internal	12.595	19.107	26.398
Cell Units	68 cells	68 cells	75 cells

Cell: XNOR2

Function: 2-Way XNOR

Boolean Expression: $Z = \overline{A \oplus B}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	A	t _{PLH}	0.136 + 0.062N _{std}	0.088 + 0.041N _{std}	0.059 + 0.029N _{std}
		t _{PHL}	0.137 + 0.039N _{std}	0.097 + 0.024N _{std}	0.073 + 0.017N _{std}
B-Z		t _{PLH}	0.147 + 0.061N _{std}	0.095 + 0.041N _{std}	0.063 + 0.029N _{std}
		t _{PHL}	0.117 + 0.039N _{std}	0.078 + 0.025N _{std}	0.058 + 0.018N _{std}
A-Z	B	t _{PLH}	0.132 + 0.050N _{std}	0.086 + 0.033N _{std}	0.059 + 0.024N _{std}
		t _{PHL}	0.133 + 0.035N _{std}	0.094 + 0.021N _{std}	0.070 + 0.015N _{std}
B-Z		t _{PLH}	0.142 + 0.049N _{std}	0.093 + 0.033N _{std}	0.063 + 0.024N _{std}
		t _{PHL}	0.118 + 0.035N _{std}	0.079 + 0.022N _{std}	0.059 + 0.016N _{std}
A-Z	C	t _{PLH}	0.121 + 0.024N _{std}	0.081 + 0.017N _{std}	0.057 + 0.012N _{std}
		t _{PHL}	0.123 + 0.019N _{std}	0.087 + 0.012N _{std}	0.066 + 0.009N _{std}
B-Z		t _{PLH}	0.129 + 0.024N _{std}	0.086 + 0.016N _{std}	0.060 + 0.012N _{std}
		t _{PHL}	0.113 + 0.019N _{std}	0.077 + 0.012N _{std}	0.059 + 0.009N _{std}
A-Z	D	t _{PLH}	0.182 + 0.017N _{std}	0.125 + 0.011N _{std}	0.092 + 0.008N _{std}
		t _{PHL}	0.189 + 0.013N _{std}	0.124 + 0.009N _{std}	0.085 + 0.006N _{std}
B-Z		t _{PLH}	0.179 + 0.017N _{std}	0.123 + 0.011N _{std}	0.091 + 0.008N _{std}
		t _{PHL}	0.209 + 0.013N _{std}	0.148 + 0.009N _{std}	0.112 + 0.006N _{std}
A-Z	E	t _{PLH}	0.189 + 0.017N _{std}	0.129 + 0.012N _{std}	0.095 + 0.008N _{std}
		t _{PHL}	0.198 + 0.013N _{std}	0.129 + 0.009N _{std}	0.088 + 0.007N _{std}
B-Z		t _{PLH}	0.186 + 0.017N _{std}	0.127 + 0.012N _{std}	0.094 + 0.008N _{std}
		t _{PHL}	0.219 + 0.013N _{std}	0.154 + 0.009N _{std}	0.116 + 0.007N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	F	t _{PLH}	0.184 + 0.011N _{std}	0.126 + 0.008N _{std}	0.093 + 0.005N _{std}
		t _{PHL}	0.195 + 0.009N _{std}	0.128 + 0.006N _{std}	0.088 + 0.004N _{std}
B-Z		t _{PLH}	0.182 + 0.011N _{std}	0.124 + 0.008N _{std}	0.092 + 0.005N _{std}
		t _{PHL}	0.213 + 0.009N _{std}	0.151 + 0.006N _{std}	0.114 + 0.004N _{std}
A-Z	H	t _{PLH}	0.190 + 0.009N _{std}	0.129 + 0.006N _{std}	0.095 + 0.004N _{std}
		t _{PHL}	0.197 + 0.007N _{std}	0.130 + 0.005N _{std}	0.091 + 0.003N _{std}
B-Z		t _{PLH}	0.188 + 0.009N _{std}	0.127 + 0.006N _{std}	0.093 + 0.004N _{std}
		t _{PHL}	0.203 + 0.007N _{std}	0.144 + 0.005N _{std}	0.109 + 0.003N _{std}
A-Z	I	t _{PLH}	0.213 + 0.005N _{std}	0.144 + 0.004N _{std}	0.104 + 0.003N _{std}
		t _{PHL}	0.224 + 0.004N _{std}	0.148 + 0.003N _{std}	0.103 + 0.002N _{std}
B-Z		t _{PLH}	0.211 + 0.005N _{std}	0.142 + 0.004N _{std}	0.103 + 0.003N _{std}
		t _{PHL}	0.231 + 0.004N _{std}	0.163 + 0.003N _{std}	0.121 + 0.002N _{std}
A-Z	J	t _{PLH}	0.239 + 0.004N _{std}	0.160 + 0.003N _{std}	0.116 + 0.002N _{std}
		t _{PHL}	0.257 + 0.003N _{std}	0.170 + 0.002N _{std}	0.118 + 0.001N _{std}
B-Z		t _{PLH}	0.236 + 0.004N _{std}	0.158 + 0.003N _{std}	0.114 + 0.002N _{std}
		t _{PHL}	0.265 + 0.003N _{std}	0.185 + 0.002N _{std}	0.137 + 0.001N _{std}

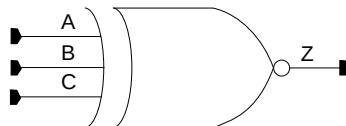
Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins			
	A	B	Internal	Cell Units
A	0.443	0.698	2.098	7 cells
B	0.501	0.796	2.417	7 cells
C	0.845	1.357	4.255	7 cells
D	0.655	0.924	4.398	9 cells
E	0.567	0.806	3.924	9 cells
F	0.749	1.050	5.442	9 cells
H	0.836	1.132	6.294	9 cells
I	0.842	1.139	7.556	10 cells
J	0.842	1.134	9.224	12 cells

Cell: XNOR3

Function: 3-Way XNOR

Boolean Expression: $Z = \overline{A \oplus B \oplus C}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	B	t _{PLH}	0.228 + 0.061N _{std}	0.151 + 0.040N _{std}	0.098 + 0.028N _{std}
		t _{PHL}	0.244 + 0.040N _{std}	0.156 + 0.026N _{std}	0.108 + 0.017N _{std}
C-Z		t _{PLH}	0.143 + 0.062N _{std}	0.099 + 0.040N _{std}	0.073 + 0.028N _{std}
		t _{PHL}	0.154 + 0.038N _{std}	0.106 + 0.025N _{std}	0.078 + 0.018N _{std}
A-Z	C	t _{PLH}	0.229 + 0.031N _{std}	0.152 + 0.021N _{std}	0.100 + 0.016N _{std}
		t _{PHL}	0.261 + 0.023N _{std}	0.168 + 0.015N _{std}	0.114 + 0.010N _{std}
C-Z		t _{PLH}	0.145 + 0.032N _{std}	0.100 + 0.022N _{std}	0.075 + 0.016N _{std}
		t _{PHL}	0.170 + 0.022N _{std}	0.117 + 0.015N _{std}	0.087 + 0.011N _{std}
A-Z	D	t _{PLH}	0.225 + 0.022N _{std}	0.145 + 0.015N _{std}	0.100 + 0.011N _{std}
		t _{PHL}	0.253 + 0.016N _{std}	0.161 + 0.011N _{std}	0.109 + 0.008N _{std}
C-Z		t _{PLH}	0.149 + 0.022N _{std}	0.104 + 0.015N _{std}	0.077 + 0.011N _{std}
		t _{PHL}	0.175 + 0.016N _{std}	0.122 + 0.010N _{std}	0.091 + 0.008N _{std}
A-Z	E	t _{PLH}	0.235 + 0.016N _{std}	0.155 + 0.011N _{std}	0.111 + 0.008N _{std}
		t _{PHL}	0.273 + 0.011N _{std}	0.176 + 0.007N _{std}	0.122 + 0.005N _{std}
C-Z		t _{PLH}	0.160 + 0.016N _{std}	0.110 + 0.011N _{std}	0.081 + 0.008N _{std}
		t _{PHL}	0.189 + 0.010N _{std}	0.129 + 0.007N _{std}	0.096 + 0.005N _{std}
A-Z	F	t _{PLH}	0.244 + 0.010N _{std}	0.161 + 0.007N _{std}	0.116 + 0.005N _{std}
		t _{PHL}	0.286 + 0.005N _{std}	0.190 + 0.003N _{std}	0.133 + 0.003N _{std}
C-Z		t _{PLH}	0.170 + 0.010N _{std}	0.117 + 0.007N _{std}	0.086 + 0.005N _{std}
		t _{PHL}	0.184 + 0.006N _{std}	0.128 + 0.004N _{std}	0.094 + 0.003N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	H	t _{PLH}	0.250 + 0.008N _{std}	0.161 + 0.005N _{std}	0.112 + 0.004N _{std}
		t _{PHL}	0.301 + 0.004N _{std}	0.200 + 0.003N _{std}	0.140 + 0.002N _{std}
C-Z		t _{PLH}	0.177 + 0.008N _{std}	0.121 + 0.005N _{std}	0.089 + 0.004N _{std}
		t _{PHL}	0.206 + 0.005N _{std}	0.141 + 0.003N _{std}	0.103 + 0.002N _{std}
A-Z	I	t _{PLH}	0.278 + 0.005N _{std}	0.182 + 0.004N _{std}	0.130 + 0.003N _{std}
		t _{PHL}	0.336 + 0.003N _{std}	0.222 + 0.002N _{std}	0.154 + 0.001N _{std}
C-Z		t _{PLH}	0.211 + 0.005N _{std}	0.142 + 0.004N _{std}	0.104 + 0.003N _{std}
		t _{PHL}	0.232 + 0.003N _{std}	0.157 + 0.002N _{std}	0.111 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

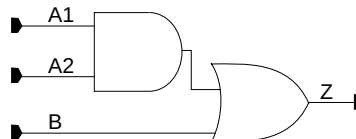
Performance Level	Input Pins				
	A	B	C	Internal	Cell Units
B	1.278	0.889	0.967	5.046	17 cells
C	1.278	0.890	0.964	5.359	17 cells
D	1.276	0.890	1.012	6.003	17 cells
E	1.371	0.985	1.011	6.520	17 cells
F	1.419	0.983	1.319	8.574	17 cells
H	1.420	0.982	1.318	9.213	17 cells
I	1.434	0.987	1.464	12.683	19 cells

Standard Cell Complex Logic

Cell: AO21

Function: 2x1 AND OR

Boolean Expression: $Z = (A1 \bullet A2) + B$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	B	t _{PLH}	0.145 + 0.070N _{std}	0.088 + 0.045N _{std}	0.057 + 0.031N _{std}
		t _{PHL}	0.174 + 0.036N _{std}	0.123 + 0.023N _{std}	0.092 + 0.016N _{std}
B-Z		t _{PLH}	0.134 + 0.070N _{std}	0.085 + 0.045N _{std}	0.067 + 0.031N _{std}
		t _{PHL}	0.192 + 0.036N _{std}	0.132 + 0.023N _{std}	0.060 + 0.016N _{std}
A1-Z	C	t _{PLH}	0.155 + 0.034N _{std}	0.097 + 0.023N _{std}	0.065 + 0.016N _{std}
t _{PHL}		0.168 + 0.028N _{std}	0.118 + 0.018N _{std}	0.087 + 0.013N _{std}	
B-Z		t _{PLH}	0.140 + 0.034N _{std}	0.093 + 0.023N _{std}	0.078 + 0.016N _{std}
		t _{PHL}	0.181 + 0.028N _{std}	0.124 + 0.018N _{std}	0.056 + 0.013N _{std}
A1-Z	D	t _{PLH}	0.148 + 0.022N _{std}	0.094 + 0.015N _{std}	0.064 + 0.011N _{std}
t _{PHL}		0.160 + 0.018N _{std}	0.114 + 0.011N _{std}	0.085 + 0.008N _{std}	
B-Z		t _{PLH}	0.171 + 0.022N _{std}	0.113 + 0.015N _{std}	0.097 + 0.011N _{std}
		t _{PHL}	0.173 + 0.018N _{std}	0.118 + 0.012N _{std}	0.051 + 0.008N _{std}
A1-Z	E	t _{PLH}	0.143 + 0.016N _{std}	0.092 + 0.011N _{std}	0.063 + 0.008N _{std}
t _{PHL}		0.159 + 0.013N _{std}	0.114 + 0.008N _{std}	0.086 + 0.006N _{std}	
B-Z		t _{PLH}	0.180 + 0.016N _{std}	0.120 + 0.011N _{std}	0.104 + 0.008N _{std}
		t _{PHL}	0.172 + 0.013N _{std}	0.118 + 0.008N _{std}	0.049 + 0.006N _{std}
A1-Z	F	t _{PLH}	0.137 + 0.011N _{std}	0.088 + 0.007N _{std}	0.061 + 0.006N _{std}
t _{PHL}		0.157 + 0.008N _{std}	0.113 + 0.005N _{std}	0.085 + 0.004N _{std}	
B-Z		t _{PLH}	0.176 + 0.011N _{std}	0.119 + 0.007N _{std}	0.104 + 0.005N _{std}
		t _{PHL}	0.170 + 0.008N _{std}	0.117 + 0.005N _{std}	0.048 + 0.004N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	H	t _{PLH}	0.143 + 0.008N _{std}	0.092 + 0.006N _{std}	0.063 + 0.004N _{std}
		t _{PHL}	0.179 + 0.005N _{std}	0.129 + 0.003N _{std}	0.097 + 0.002N _{std}
B-Z		t _{PLH}	0.176 + 0.008N _{std}	0.119 + 0.006N _{std}	0.101 + 0.004N _{std}
		t _{PHL}	0.192 + 0.005N _{std}	0.133 + 0.003N _{std}	0.055 + 0.002N _{std}
A1-Z	I	t _{PLH}	0.146 + 0.005N _{std}	0.094 + 0.004N _{std}	0.065 + 0.003N _{std}
		t _{PHL}	0.193 + 0.004N _{std}	0.139 + 0.003N _{std}	0.104 + 0.002N _{std}
B-Z		t _{PLH}	0.178 + 0.005N _{std}	0.121 + 0.004N _{std}	0.103 + 0.003N _{std}
		t _{PHL}	0.206 + 0.004N _{std}	0.142 + 0.003N _{std}	0.059 + 0.002N _{std}
A1-Z	J	t _{PLH}	0.163 + 0.004N _{std}	0.105 + 0.003N _{std}	0.073 + 0.002N _{std}
		t _{PHL}	0.192 + 0.002N _{std}	0.137 + 0.002N _{std}	0.103 + 0.001N _{std}
B-Z		t _{PLH}	0.231 + 0.004N _{std}	0.157 + 0.003N _{std}	0.118 + 0.002N _{std}
		t _{PHL}	0.214 + 0.002N _{std}	0.145 + 0.002N _{std}	0.087 + 0.001N _{std}
A1-Z	K	t _{PLH}	0.174 + 0.003N _{std}	0.114 + 0.002N _{std}	0.081 + 0.001N _{std}
		t _{PHL}	0.187 + 0.002N _{std}	0.133 + 0.001N _{std}	0.099 + 0.001N _{std}
B-Z		t _{PLH}	0.247 + 0.003N _{std}	0.169 + 0.002N _{std}	0.129 + 0.001N _{std}
		t _{PHL}	0.212 + 0.002N _{std}	0.143 + 0.001N _{std}	0.085 + 0.001N _{std}



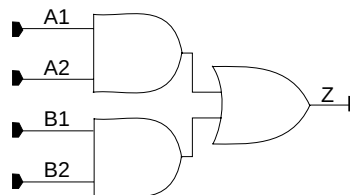
Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins				
	A1	A2	B	Internal	Cell Units
B	0.326	0.317	0.510	1.418	7 cells
C	0.372	0.365	0.617	1.816	7 cells
D	0.499	0.496	0.793	2.433	7 cells
E	0.602	0.600	0.941	3.031	7 cells
F	0.820	0.825	1.286	4.350	7 cells
H	0.828	0.834	1.235	5.136	7 cells
I	0.924	0.930	1.407	6.339	7 cells
J	1.254	1.343	1.232	8.960	11 cells
K	1.557	1.703	1.579	11.724	11 cells

Cell: AO22

Function: 2x2 AND OR

Boolean Expression: $Z = (A1 \bullet A2) + (B1 \bullet B2)$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	B	t _{PLH}	0.137 + 0.074N _{std}	0.084 + 0.047N _{std}	0.051 + 0.032N _{std}
		t _{PHL}	0.177 + 0.036N _{std}	0.126 + 0.022N _{std}	0.073 + 0.016N _{std}
B2-Z		t _{PLH}	0.162 + 0.073N _{std}	0.098 + 0.047N _{std}	0.065 + 0.032N _{std}
		t _{PHL}	0.216 + 0.036N _{std}	0.147 + 0.023N _{std}	0.089 + 0.017N _{std}
A1-Z	C	t _{PLH}	0.125 + 0.034N _{std}	0.079 + 0.023N _{std}	0.050 + 0.016N _{std}
		t _{PHL}	0.152 + 0.028N _{std}	0.108 + 0.018N _{std}	0.064 + 0.013N _{std}
B2-Z		t _{PLH}	0.158 + 0.034N _{std}	0.099 + 0.023N _{std}	0.069 + 0.016N _{std}
		t _{PHL}	0.188 + 0.028N _{std}	0.128 + 0.018N _{std}	0.081 + 0.013N _{std}
A1-Z	D	t _{PLH}	0.123 + 0.021N _{std}	0.078 + 0.015N _{std}	0.050 + 0.011N _{std}
		t _{PHL}	0.156 + 0.017N _{std}	0.112 + 0.011N _{std}	0.067 + 0.008N _{std}
B2-Z		t _{PLH}	0.155 + 0.021N _{std}	0.097 + 0.015N _{std}	0.068 + 0.011N _{std}
		t _{PHL}	0.193 + 0.017N _{std}	0.132 + 0.011N _{std}	0.084 + 0.008N _{std}
A1-Z	E	t _{PLH}	0.123 + 0.016N _{std}	0.079 + 0.011N _{std}	0.050 + 0.008N _{std}
		t _{PHL}	0.161 + 0.013N _{std}	0.116 + 0.009N _{std}	0.070 + 0.006N _{std}
B2-Z		t _{PLH}	0.154 + 0.016N _{std}	0.097 + 0.011N _{std}	0.068 + 0.008N _{std}
		t _{PHL}	0.199 + 0.013N _{std}	0.136 + 0.009N _{std}	0.086 + 0.006N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	F	t _{PLH}	0.137 + 0.010N _{std}	0.087 + 0.007N _{std}	0.055 + 0.005N _{std}
B2-Z		t _{PHL}	0.192 + 0.005N _{std}	0.138 + 0.003N _{std}	0.083 + 0.002N _{std}
		t _{PLH}	0.161 + 0.010N _{std}	0.101 + 0.007N _{std}	0.069 + 0.005N _{std}
		t _{PHL}	0.229 + 0.005N _{std}	0.158 + 0.003N _{std}	0.097 + 0.002N _{std}
A1-Z	H	t _{PLH}	0.145 + 0.007N _{std}	0.094 + 0.005N _{std}	0.061 + 0.004N _{std}
B2-Z		t _{PHL}	0.192 + 0.004N _{std}	0.138 + 0.003N _{std}	0.083 + 0.002N _{std}
		t _{PLH}	0.173 + 0.007N _{std}	0.109 + 0.005N _{std}	0.077 + 0.004N _{std}
		t _{PHL}	0.228 + 0.005N _{std}	0.157 + 0.003N _{std}	0.098 + 0.002N _{std}
A1-Z	I	t _{PLH}	0.142 + 0.005N _{std}	0.091 + 0.003N _{std}	0.057 + 0.003N _{std}
B2-Z		t _{PHL}	0.212 + 0.002N _{std}	0.151 + 0.002N _{std}	0.091 + 0.001N _{std}
		t _{PLH}	0.164 + 0.005N _{std}	0.103 + 0.003N _{std}	0.070 + 0.003N _{std}
		t _{PHL}	0.246 + 0.003N _{std}	0.168 + 0.002N _{std}	0.104 + 0.001N _{std}
A1-Z	J	t _{PLH}	0.151 + 0.004N _{std}	0.097 + 0.003N _{std}	0.064 + 0.002N _{std}
B2-Z		t _{PHL}	0.207 + 0.002N _{std}	0.147 + 0.002N _{std}	0.089 + 0.001N _{std}
		t _{PLH}	0.178 + 0.004N _{std}	0.112 + 0.003N _{std}	0.079 + 0.002N _{std}
		t _{PHL}	0.237 + 0.002N _{std}	0.162 + 0.002N _{std}	0.101 + 0.001N _{std}
A1-Z	K	t _{PLH}	0.159 + 0.003N _{std}	0.103 + 0.002N _{std}	0.068 + 0.001N _{std}
B2-Z		t _{PHL}	0.225 + 0.002N _{std}	0.159 + 0.001N _{std}	0.096 + 0.001N _{std}
		t _{PLH}	0.184 + 0.003N _{std}	0.117 + 0.002N _{std}	0.083 + 0.001N _{std}
		t _{PHL}	0.255 + 0.002N _{std}	0.174 + 0.001N _{std}	0.108 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

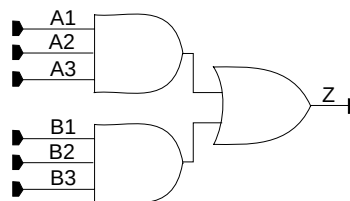
Performance Level	Input Pins					
	A1	A2	B1	B2	Internal	Cell Units
B	0.504	0.451	0.500	0.474	1.793	8 cells
C	0.901	0.864	0.915	0.894	3.514	8 cells
D	0.973	0.951	0.989	0.963	4.099	8 cells
E	1.013	0.990	1.029	1.003	4.491	8 cells
F	0.963	0.921	0.971	0.959	5.328	8 cells
H	1.033	1.007	1.048	1.031	6.126	8 cells
I	1.668	1.730	1.693	1.736	10.205	15 cells
J	1.894	1.986	1.929	2.014	12.053	15 cells
K	1.898	1.990	1.935	2.020	13.359	15 cells

Cell: AO33

Function: 3x3 AND OR

Boolean Expression:

$$Z = (A1 \bullet A2 \bullet A3) + (B1 \bullet B2 \bullet B3)$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	C	t _{PLH}	0.187 + 0.036N _{std}	0.115 + 0.023N _{std}	0.077 + 0.016N _{std}
		t _{PHL}	0.201 + 0.028N _{std}	0.138 + 0.017N _{std}	0.101 + 0.012N _{std}
B2-Z		t _{PLH}	0.207 + 0.036N _{std}	0.125 + 0.023N _{std}	0.083 + 0.016N _{std}
		t _{PHL}	0.221 + 0.028N _{std}	0.152 + 0.017N _{std}	0.112 + 0.011N _{std}
A1-Z	E	t _{PLH}	0.216 + 0.016N _{std}	0.133 + 0.011N _{std}	0.089 + 0.008N _{std}
		t _{PHL}	0.213 + 0.013N _{std}	0.147 + 0.008N _{std}	0.107 + 0.006N _{std}
B2-Z		t _{PLH}	0.234 + 0.016N _{std}	0.141 + 0.011N _{std}	0.094 + 0.008N _{std}
		t _{PHL}	0.232 + 0.013N _{std}	0.161 + 0.008N _{std}	0.116 + 0.006N _{std}
A1-Z	H	t _{PLH}	0.196 + 0.007N _{std}	0.123 + 0.005N _{std}	0.084 + 0.004N _{std}
		t _{PHL}	0.195 + 0.006N _{std}	0.138 + 0.004N _{std}	0.102 + 0.003N _{std}
B2-Z		t _{PLH}	0.212 + 0.007N _{std}	0.130 + 0.005N _{std}	0.088 + 0.004N _{std}
		t _{PHL}	0.216 + 0.006N _{std}	0.152 + 0.004N _{std}	0.112 + 0.003N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

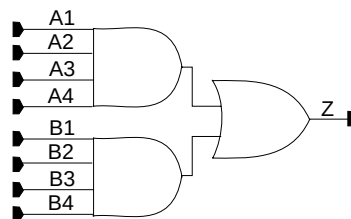
Input Pins	Performance Level		
	C	E	H
A1	0.291	0.336	0.536
A2	0.263	0.310	0.527
A3	0.279	0.325	0.534
B1	0.294	0.339	0.540
B2	0.259	0.307	0.523
B3	0.284	0.330	0.539
Internal	1.781	2.815	5.178
Cell Units	16 cells	16 cells	16 cells

Cell: AO44

Function: 4x4 AND OR

Boolean Expression:

$$Z = (A1 \bullet A2 \bullet A3 \bullet A4) + (B1 \bullet B2 \bullet B3 \bullet B4)$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	C	t _{PLH}	0.238 + 0.035N _{std}	0.144 + 0.022N _{std}	0.096 + 0.015N _{std}
		t _{PHL}	0.218 + 0.028N _{std}	0.148 + 0.017N _{std}	0.107 + 0.012N _{std}
B4-Z		t _{PLH}	0.272 + 0.034N _{std}	0.158 + 0.022N _{std}	0.102 + 0.015N _{std}
		t _{PHL}	0.263 + 0.028N _{std}	0.178 + 0.017N _{std}	0.129 + 0.012N _{std}
A1-Z	E	t _{PLH}	0.263 + 0.015N _{std}	0.158 + 0.010N _{std}	0.105 + 0.007N _{std}
		t _{PHL}	0.252 + 0.013N _{std}	0.172 + 0.008N _{std}	0.123 + 0.005N _{std}
B4-Z		t _{PLH}	0.291 + 0.015N _{std}	0.168 + 0.010N _{std}	0.107 + 0.007N _{std}
		t _{PHL}	0.301 + 0.013N _{std}	0.204 + 0.008N _{std}	0.146 + 0.005N _{std}
A1-Z	H	t _{PLH}	0.230 + 0.007N _{std}	0.142 + 0.005N _{std}	0.096 + 0.004N _{std}
		t _{PHL}	0.227 + 0.006N _{std}	0.160 + 0.004N _{std}	0.117 + 0.003N _{std}
B4-Z		t _{PLH}	0.254 + 0.007N _{std}	0.149 + 0.005N _{std}	0.097 + 0.004N _{std}
		t _{PHL}	0.278 + 0.006N _{std}	0.194 + 0.004N _{std}	0.142 + 0.003N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

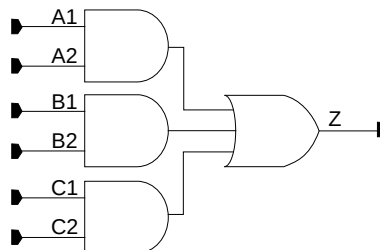
Input Pins	Performance Level		
	C	E	H
A1	0.286	0.320	0.502
A2	0.286	0.320	0.503
A3	0.288	0.323	0.509
A4	0.272	0.308	0.501
B1	0.285	0.320	0.503
B2	0.286	0.320	0.504
B3	0.288	0.323	0.509
B4	0.272	0.308	0.500
Internal	1.903	3.012	5.425
Cell Units	17 cells	17 cells	17 cells

Cell: AO222

Function: 2x2x2 AND OR

Boolean Expression:

$$Z = (A1 \bullet A2) + (B1 \bullet B2) + (C1 \bullet C2)$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	B	t _{PLH}	0.132 + 0.067N _{std}	0.082 + 0.044N _{std}	0.054 + 0.030N _{std}
		t _{PHL}	0.142 + 0.046N _{std}	0.100 + 0.028N _{std}	0.077 + 0.019N _{std}
C2-Z		t _{PLH}	0.174 + 0.067N _{std}	0.108 + 0.043N _{std}	0.074 + 0.030N _{std}
		t _{PHL}	0.198 + 0.047N _{std}	0.133 + 0.029N _{std}	0.084 + 0.019N _{std}
A1-Z	C	t _{PLH}	0.139 + 0.031N _{std}	0.087 + 0.021N _{std}	0.057 + 0.015N _{std}
		t _{PHL}	0.150 + 0.023N _{std}	0.106 + 0.015N _{std}	0.079 + 0.010N _{std}
C2-Z		t _{PLH}	0.164 + 0.031N _{std}	0.102 + 0.021N _{std}	0.070 + 0.015N _{std}
		t _{PHL}	0.197 + 0.024N _{std}	0.133 + 0.015N _{std}	0.082 + 0.010N _{std}
A1-Z	D	t _{PLH}	0.143 + 0.020N _{std}	0.090 + 0.014N _{std}	0.061 + 0.010N _{std}
		t _{PHL}	0.151 + 0.015N _{std}	0.108 + 0.009N _{std}	0.080 + 0.007N _{std}
C2-Z		t _{PLH}	0.166 + 0.020N _{std}	0.103 + 0.014N _{std}	0.071 + 0.010N _{std}
		t _{PHL}	0.205 + 0.015N _{std}	0.139 + 0.009N _{std}	0.086 + 0.007N _{std}
A1-Z	E	t _{PLH}	0.156 + 0.015N _{std}	0.099 + 0.010N _{std}	0.067 + 0.008N _{std}
		t _{PHL}	0.166 + 0.011N _{std}	0.118 + 0.007N _{std}	0.087 + 0.005N _{std}
C2-Z		t _{PLH}	0.173 + 0.015N _{std}	0.108 + 0.010N _{std}	0.075 + 0.007N _{std}
		t _{PHL}	0.208 + 0.011N _{std}	0.141 + 0.007N _{std}	0.087 + 0.005N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	F	t _{PLH}	0.210 + 0.010N _{std}	0.132 + 0.007N _{std}	0.090 + 0.005N _{std}
		t _{PHL}	0.205 + 0.007N _{std}	0.144 + 0.004N _{std}	0.106 + 0.003N _{std}
C2-Z		t _{PLH}	0.176 + 0.010N _{std}	0.111 + 0.007N _{std}	0.078 + 0.005N _{std}
		t _{PHL}	0.217 + 0.007N _{std}	0.148 + 0.004N _{std}	0.091 + 0.003N _{std}
A1-Z	H	t _{PLH}	0.226 + 0.008N _{std}	0.142 + 0.006N _{std}	0.097 + 0.004N _{std}
		t _{PHL}	0.224 + 0.006N _{std}	0.157 + 0.004N _{std}	0.114 + 0.003N _{std}
C2-Z		t _{PLH}	0.181 + 0.008N _{std}	0.114 + 0.005N _{std}	0.080 + 0.004N _{std}
		t _{PHL}	0.227 + 0.006N _{std}	0.154 + 0.004N _{std}	0.095 + 0.003N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

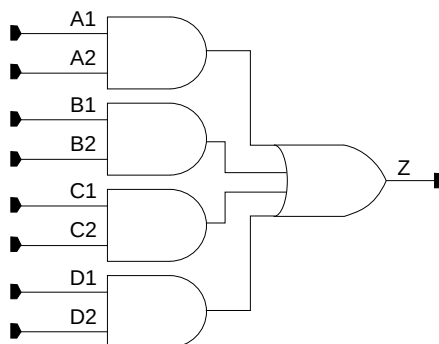
Input Pins	Performance Level					
	B	C	D	E	F	H
A1	0.309	0.367	0.387	0.387	0.430	0.429
A2	0.306	0.364	0.417	0.416	0.401	0.401
B1	0.654	0.958	0.979	0.979	1.014	1.013
B2	0.663	0.976	0.996	0.993	1.028	1.027
C1	0.657	0.979	1.002	1.049	1.050	1.050
C2	0.675	0.992	1.014	1.017	1.060	1.060
Internal	2.161	3.339	3.913	4.492	5.342	5.892
Cell Units	12 cells	12 cells	12 cells	12 cells	13 cells	13 cells

Cell: AO2222

Function: 2x2x2x2 AND OR

Boolean Expression:

$$Z = (A1 \bullet A2) + (B1 \bullet B2) + (C1 \bullet C2) + (D1 \bullet D2)$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	B	t _{PLH}	0.143 + 0.067N _{std}	0.091 + 0.043N _{std}	0.057 + 0.030N _{std}
		t _{PHL}	0.163 + 0.050N _{std}	0.114 + 0.031N _{std}	0.069 + 0.021N _{std}
D2-Z		t _{PLH}	0.162 + 0.067N _{std}	0.101 + 0.043N _{std}	0.069 + 0.030N _{std}
		t _{PHL}	0.205 + 0.051N _{std}	0.138 + 0.031N _{std}	0.085 + 0.021N _{std}
A1-Z	C	t _{PLH}	0.134 + 0.031N _{std}	0.084 + 0.021N _{std}	0.052 + 0.015N _{std}
		t _{PHL}	0.163 + 0.025N _{std}	0.115 + 0.015N _{std}	0.069 + 0.011N _{std}
D2-Z		t _{PLH}	0.152 + 0.031N _{std}	0.094 + 0.021N _{std}	0.064 + 0.015N _{std}
		t _{PHL}	0.201 + 0.025N _{std}	0.136 + 0.016N _{std}	0.084 + 0.011N _{std}
A1-Z	D	t _{PLH}	0.138 + 0.020N _{std}	0.087 + 0.014N _{std}	0.055 + 0.010N _{std}
		t _{PHL}	0.168 + 0.016N _{std}	0.118 + 0.010N _{std}	0.071 + 0.007N _{std}
D2-Z		t _{PLH}	0.155 + 0.020N _{std}	0.096 + 0.014N _{std}	0.066 + 0.010N _{std}
		t _{PHL}	0.206 + 0.016N _{std}	0.139 + 0.010N _{std}	0.086 + 0.007N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	E	t _{PLH}	0.143 + 0.015N _{std}	0.091 + 0.010N _{std}	0.058 + 0.008N _{std}
		t _{PHL}	0.172 + 0.012N _{std}	0.121 + 0.008N _{std}	0.073 + 0.005N _{std}
D2-Z		t _{PLH}	0.161 + 0.015N _{std}	0.101 + 0.010N _{std}	0.070 + 0.007N _{std}
		t _{PHL}	0.209 + 0.012N _{std}	0.142 + 0.008N _{std}	0.088 + 0.006N _{std}
A1-Z	F	t _{PLH}	0.147 + 0.010N _{std}	0.094 + 0.007N _{std}	0.061 + 0.005N _{std}
		t _{PHL}	0.183 + 0.007N _{std}	0.130 + 0.004N _{std}	0.077 + 0.003N _{std}
D2-Z		t _{PLH}	0.190 + 0.010N _{std}	0.119 + 0.007N _{std}	0.083 + 0.005N _{std}
		t _{PHL}	0.222 + 0.007N _{std}	0.150 + 0.004N _{std}	0.093 + 0.003N _{std}
A1-Z	H	t _{PLH}	0.153 + 0.008N _{std}	0.098 + 0.005N _{std}	0.064 + 0.004N _{std}
		t _{PHL}	0.195 + 0.006N _{std}	0.138 + 0.004N _{std}	0.082 + 0.003N _{std}
D2-Z		t _{PLH}	0.193 + 0.008N _{std}	0.121 + 0.005N _{std}	0.085 + 0.004N _{std}
		t _{PHL}	0.234 + 0.006N _{std}	0.158 + 0.004N _{std}	0.097 + 0.003N _{std}

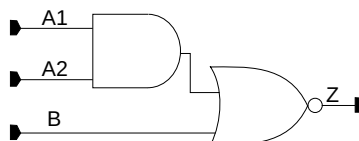
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level					
	B	C	D	E	F	H
A1	0.651	0.977	0.985	0.977	0.987	0.986
A2	0.659	0.993	1.002	0.991	0.996	0.995
B1	0.655	1.002	1.011	1.047	1.057	1.057
B2	0.692	1.031	1.040	1.028	1.027	1.026
C1	0.650	0.976	0.984	0.975	0.985	0.984
C2	0.657	0.991	1.000	0.989	0.998	0.996
D1	0.657	1.001	1.011	1.047	1.057	1.056
D2	0.694	1.032	1.042	1.028	1.035	1.035
Internal	2.522	4.072	4.528	5.141	6.230	6.840
Cell Units	14 cells	14 cells	14 cells	14 cells	16 cells	16 cells

Cell: AOI21

Function: 2x1 AND OR Invert

Boolean Expression: $Z = \overline{(A1 \bullet A2) + B}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	A	t _{PLH}	0.112 + 0.101N _{std}	0.083 + 0.066N _{std}	0.070 + 0.045N _{std}
		t _{PHL}	0.073 + 0.056N _{std}	0.048 + 0.034N _{std}	0.029 + 0.024N _{std}
B-Z		t _{PLH}	0.130 + 0.102N _{std}	0.092 + 0.067N _{std}	0.042 + 0.024N _{std}
		t _{PHL}	0.067 + 0.036N _{std}	0.046 + 0.024N _{std}	0.041 + 0.017N _{std}
A1-Z	B	t _{PLH}	0.091 + 0.051N _{std}	0.070 + 0.034N _{std}	0.055 + 0.024N _{std}
		t _{PHL}	0.086 + 0.043N _{std}	0.056 + 0.026N _{std}	0.037 + 0.019N _{std}
B-Z		t _{PLH}	0.103 + 0.051N _{std}	0.074 + 0.034N _{std}	0.031 + 0.013N _{std}
		t _{PHL}	0.099 + 0.034N _{std}	0.068 + 0.022N _{std}	0.064 + 0.016N _{std}
A1-Z	C	t _{PLH}	0.087 + 0.024N _{std}	0.067 + 0.016N _{std}	0.054 + 0.012N _{std}
		t _{PHL}	0.083 + 0.020N _{std}	0.055 + 0.013N _{std}	0.038 + 0.009N _{std}
B-Z		t _{PLH}	0.098 + 0.024N _{std}	0.069 + 0.017N _{std}	0.028 + 0.007N _{std}
		t _{PHL}	0.111 + 0.020N _{std}	0.078 + 0.013N _{std}	0.074 + 0.010N _{std}
A1-Z	D	t _{PLH}	0.095 + 0.017N _{std}	0.075 + 0.011N _{std}	0.061 + 0.008N _{std}
		t _{PHL}	0.076 + 0.011N _{std}	0.050 + 0.007N _{std}	0.033 + 0.005N _{std}
B-Z		t _{PLH}	0.116 + 0.016N _{std}	0.083 + 0.011N _{std}	0.055 + 0.006N _{std}
		t _{PHL}	0.101 + 0.010N _{std}	0.071 + 0.007N _{std}	0.055 + 0.005N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	E	t _{PLH}	0.097 + 0.013N _{std}	0.076 + 0.009N _{std}	0.062 + 0.006N _{std}
		t _{PHL}	0.074 + 0.008N _{std}	0.049 + 0.005N _{std}	0.033 + 0.004N _{std}
B-Z		t _{PLH}	0.116 + 0.012N _{std}	0.083 + 0.008N _{std}	0.055 + 0.005N _{std}
		t _{PHL}	0.097 + 0.007N _{std}	0.069 + 0.005N _{std}	0.054 + 0.004N _{std}
A1-Z	F	t _{PLH}	0.099 + 0.008N _{std}	0.077 + 0.005N _{std}	0.063 + 0.004N _{std}
		t _{PHL}	0.073 + 0.005N _{std}	0.049 + 0.003N _{std}	0.033 + 0.002N _{std}
B-Z		t _{PLH}	0.119 + 0.008N _{std}	0.084 + 0.006N _{std}	0.054 + 0.003N _{std}
		t _{PHL}	0.097 + 0.004N _{std}	0.069 + 0.003N _{std}	0.055 + 0.002N _{std}
A1-Z	H	t _{PLH}	0.103 + 0.006N _{std}	0.080 + 0.004N _{std}	0.066 + 0.003N _{std}
		t _{PHL}	0.073 + 0.003N _{std}	0.049 + 0.002N _{std}	0.032 + 0.002N _{std}
B-Z		t _{PLH}	0.123 + 0.006N _{std}	0.087 + 0.004N _{std}	0.057 + 0.002N _{std}
		t _{PHL}	0.090 + 0.003N _{std}	0.064 + 0.002N _{std}	0.050 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

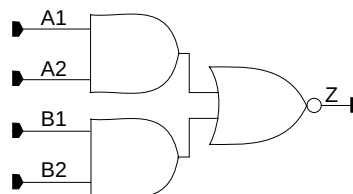
Performance Level	Input Pins				
	A1	A2	B	Internal	Cell Units
A	0.325	0.311	0.504	0.844	5 cells
B	0.467	0.460	0.741	1.248	5 cells
C	0.814	0.816	1.289	2.307	5 cells
D	1.343	1.320	1.309	3.479	7 cells
E	1.697	1.711	1.631	4.493	7 cells
F	2.722	2.732	2.377	7.219	11 cells
H	3.592	3.892	3.377	10.391	16 cells

Cell: AOI22

Function: 2x2 AND OR Invert

Boolean Expression:

$$Z = \overline{(A1 \bullet A2) + (B1 \bullet B2)}$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	A	t _{PLH}	0.125 + 0.092N _{std}	0.093 + 0.060N _{std}	0.063 + 0.031N _{std}
		t _{PHL}	0.083 + 0.055N _{std}	0.055 + 0.034N _{std}	0.035 + 0.024N _{std}
B2-Z		t _{PLH}	0.165 + 0.092N _{std}	0.114 + 0.061N _{std}	0.074 + 0.032N _{std}
		t _{PHL}	0.104 + 0.056N _{std}	0.065 + 0.034N _{std}	0.046 + 0.023N _{std}
A1-Z	B	t _{PLH}	0.111 + 0.046N _{std}	0.085 + 0.031N _{std}	0.054 + 0.017N _{std}
		t _{PHL}	0.078 + 0.030N _{std}	0.050 + 0.019N _{std}	0.032 + 0.014N _{std}
B2-Z		t _{PLH}	0.146 + 0.046N _{std}	0.103 + 0.031N _{std}	0.066 + 0.017N _{std}
		t _{PHL}	0.100 + 0.030N _{std}	0.062 + 0.019N _{std}	0.044 + 0.013N _{std}
A1-Z	C	t _{PLH}	0.105 + 0.023N _{std}	0.081 + 0.016N _{std}	0.052 + 0.009N _{std}
		t _{PHL}	0.075 + 0.015N _{std}	0.048 + 0.010N _{std}	0.032 + 0.007N _{std}
B2-Z		t _{PLH}	0.138 + 0.023N _{std}	0.096 + 0.016N _{std}	0.062 + 0.009N _{std}
		t _{PHL}	0.094 + 0.015N _{std}	0.059 + 0.010N _{std}	0.043 + 0.007N _{std}
A1-Z	D	t _{PLH}	0.111 + 0.015N _{std}	0.085 + 0.010N _{std}	0.055 + 0.006N _{std}
		t _{PHL}	0.081 + 0.010N _{std}	0.053 + 0.007N _{std}	0.035 + 0.005N _{std}
B2-Z		t _{PLH}	0.141 + 0.015N _{std}	0.099 + 0.010N _{std}	0.065 + 0.006N _{std}
		t _{PHL}	0.101 + 0.010N _{std}	0.064 + 0.006N _{std}	0.047 + 0.005N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	E	t _{PLH}	0.112 + 0.012N _{std}	0.086 + 0.008N _{std}	0.056 + 0.004N _{std}
		t _{PHL}	0.080 + 0.008N _{std}	0.054 + 0.005N _{std}	0.036 + 0.004N _{std}
B2-Z		t _{PLH}	0.140 + 0.012N _{std}	0.099 + 0.008N _{std}	0.064 + 0.004N _{std}
		t _{PHL}	0.101 + 0.008N _{std}	0.064 + 0.005N _{std}	0.048 + 0.004N _{std}
A1-Z	F	t _{PLH}	0.110 + 0.008N _{std}	0.084 + 0.005N _{std}	0.055 + 0.003N _{std}
		t _{PHL}	0.082 + 0.006N _{std}	0.055 + 0.004N _{std}	0.038 + 0.003N _{std}
B2-Z		t _{PLH}	0.137 + 0.008N _{std}	0.097 + 0.005N _{std}	0.063 + 0.003N _{std}
		t _{PHL}	0.105 + 0.006N _{std}	0.067 + 0.004N _{std}	0.050 + 0.003N _{std}
A1-Z	H	t _{PLH}	0.110 + 0.006N _{std}	0.084 + 0.004N _{std}	0.056 + 0.002N _{std}
		t _{PHL}	0.083 + 0.004N _{std}	0.056 + 0.003N _{std}	0.039 + 0.002N _{std}
B2-Z		t _{PLH}	0.140 + 0.006N _{std}	0.098 + 0.004N _{std}	0.064 + 0.002N _{std}
		t _{PHL}	0.107 + 0.004N _{std}	0.069 + 0.003N _{std}	0.052 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

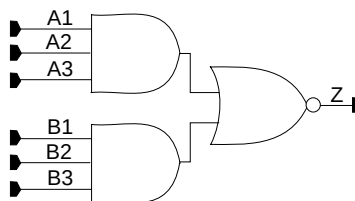
Performance Level	Input Pins					
	A1	A2	B1	B2	Internal	Cell Units
A	0.347	0.299	0.366	0.371	0.947	6 cells
B	0.550	0.521	0.576	0.560	1.549	6 cells
C	0.957	0.945	0.989	0.987	2.842	6 cells
D	1.405	1.467	1.443	1.470	4.454	11 cells
E	1.814	1.888	1.861	1.903	5.910	11 cells
F	2.630	2.613	2.744	2.749	8.299	16 cells
H	3.420	3.442	3.430	3.467	10.927	20 cells

Cell: AOI33

Function: 3x3 AND OR Invert

Boolean Expression:

$$Z = \overline{(A1 \bullet A2 \bullet A3) + (B1 \bullet B2 \bullet B3)}$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	C	t _{PLH}	0.254 + 0.035N _{std}	0.167 + 0.023N _{std}	0.119 + 0.016N _{std}
		t _{PHL}	0.241 + 0.018N _{std}	0.147 + 0.011N _{std}	0.097 + 0.008N _{std}
B2-Z		t _{PLH}	0.287 + 0.035N _{std}	0.189 + 0.023N _{std}	0.134 + 0.016N _{std}
		t _{PHL}	0.250 + 0.018N _{std}	0.151 + 0.011N _{std}	0.098 + 0.008N _{std}
A1-Z	E	t _{PLH}	0.246 + 0.016N _{std}	0.165 + 0.011N _{std}	0.118 + 0.008N _{std}
		t _{PHL}	0.245 + 0.013N _{std}	0.150 + 0.008N _{std}	0.100 + 0.006N _{std}
B2-Z		t _{PLH}	0.272 + 0.016N _{std}	0.183 + 0.011N _{std}	0.132 + 0.008N _{std}
		t _{PHL}	0.250 + 0.013N _{std}	0.150 + 0.008N _{std}	0.099 + 0.006N _{std}
A1-Z	H	t _{PLH}	0.213 + 0.009N _{std}	0.145 + 0.006N _{std}	0.107 + 0.004N _{std}
		t _{PHL}	0.234 + 0.004N _{std}	0.146 + 0.003N _{std}	0.098 + 0.002N _{std}
B2-Z		t _{PLH}	0.231 + 0.009N _{std}	0.159 + 0.006N _{std}	0.117 + 0.004N _{std}
		t _{PHL}	0.231 + 0.004N _{std}	0.142 + 0.003N _{std}	0.094 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

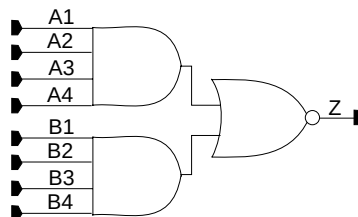
Input Pins	Performance Level		
	C	E	H
A1	0.284	0.329	0.531
A2	0.289	0.335	0.539
A3	0.275	0.322	0.533
B1	0.282	0.327	0.529
B2	0.288	0.334	0.538
B3	0.274	0.320	0.531
Internal	2.302	3.391	5.789
Cell Units	17 cells	17 cells	17 cells

Cell: AOI44

Function: 4x4 AND OR Invert

Boolean Expression:

$$Z = \overline{(A1 \bullet A2 \bullet A3 \bullet A4) + (B1 \bullet B2 \bullet B3 \bullet B4)}$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	C	t _{PLH}	0.258 + 0.034N _{std}	0.170 + 0.022N _{std}	0.119 + 0.015N _{std}
		t _{PHL}	0.260 + 0.018N _{std}	0.156 + 0.011N _{std}	0.102 + 0.008N _{std}
B4-Z		t _{PLH}	0.320 + 0.033N _{std}	0.211 + 0.021N _{std}	0.147 + 0.015N _{std}
		t _{PHL}	0.308 + 0.018N _{std}	0.178 + 0.011N _{std}	0.113 + 0.008N _{std}
A1-Z	E	t _{PLH}	0.262 + 0.016N _{std}	0.176 + 0.011N _{std}	0.126 + 0.008N _{std}
		t _{PHL}	0.252 + 0.013N _{std}	0.153 + 0.008N _{std}	0.101 + 0.006N _{std}
B4-Z		t _{PLH}	0.323 + 0.016N _{std}	0.216 + 0.011N _{std}	0.155 + 0.008N _{std}
		t _{PHL}	0.291 + 0.013N _{std}	0.169 + 0.008N _{std}	0.107 + 0.006N _{std}
A1-Z	H	t _{PLH}	0.228 + 0.008N _{std}	0.154 + 0.006N _{std}	0.114 + 0.004N _{std}
		t _{PHL}	0.241 + 0.004N _{std}	0.148 + 0.003N _{std}	0.099 + 0.002N _{std}
B4-Z		t _{PLH}	0.286 + 0.008N _{std}	0.198 + 0.006N _{std}	0.145 + 0.004N _{std}
		t _{PHL}	0.279 + 0.004N _{std}	0.165 + 0.003N _{std}	0.106 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

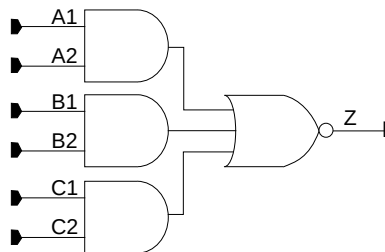
Input Pins	Performance Level		
	C	E	H
A1	0.289	0.324	0.507
A2	0.283	0.317	0.501
A3	0.286	0.321	0.509
A4	0.281	0.317	0.508
B1	0.291	0.326	0.508
B2	0.288	0.322	0.506
B3	0.283	0.318	0.504
B4	0.289	0.325	0.516
Internal	2.396	3.470	5.913
Cell Units	19 cells	19 cells	19 cells

Cell: AOI222

Function: 2x2x2 AND OR Invert

Boolean Expression:

$$Z = \overline{(A1 \bullet A2) + (B1 \bullet B2) + (C1 \bullet C2)}$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	F	t _{PLH}	0.177 + 0.010N _{std}	0.120 + 0.007N _{std}	0.085 + 0.005N _{std}
		t _{PHL}	0.251 + 0.005N _{std}	0.161 + 0.003N _{std}	0.114 + 0.002N _{std}
C2-Z		t _{PLH}	0.246 + 0.010N _{std}	0.162 + 0.007N _{std}	0.103 + 0.005N _{std}
		t _{PHL}	0.294 + 0.005N _{std}	0.186 + 0.003N _{std}	0.132 + 0.002N _{std}
A1-Z	H	t _{PLH}	0.177 + 0.008N _{std}	0.122 + 0.005N _{std}	0.090 + 0.004N _{std}
		t _{PHL}	0.242 + 0.004N _{std}	0.154 + 0.003N _{std}	0.105 + 0.002N _{std}
C2-Z		t _{PLH}	0.250 + 0.008N _{std}	0.163 + 0.005N _{std}	0.103 + 0.004N _{std}
		t _{PHL}	0.281 + 0.004N _{std}	0.176 + 0.003N _{std}	0.121 + 0.002N _{std}
A1-Z	I	t _{PLH}	0.186 + 0.005N _{std}	0.130 + 0.004N _{std}	0.096 + 0.003N _{std}
		t _{PHL}	0.229 + 0.004N _{std}	0.146 + 0.003N _{std}	0.100 + 0.002N _{std}
C2-Z		t _{PLH}	0.264 + 0.005N _{std}	0.175 + 0.004N _{std}	0.110 + 0.003N _{std}
		t _{PHL}	0.269 + 0.004N _{std}	0.169 + 0.003N _{std}	0.116 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

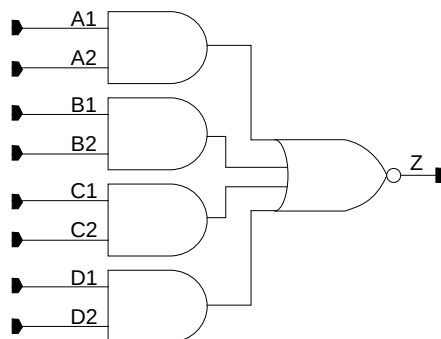
Input Pins	Performance Level		
	F	H	I
A1	0.527	0.522	0.565
A2	0.487	0.489	0.533
B1	0.865	0.968	0.984
B2	0.874	0.982	0.998
C1	0.891	0.998	1.015
C2	0.934	1.037	1.053
Internal	5.650	6.519	7.300
Cell Units	14 cells	14 cells	14 cells

Cell: AOI2222

Function: 2x2x2x2 AND OR Invert

Boolean Expression:

$$Z = \overline{(A1 \bullet A2) + (B1 \bullet B2) + (C1 \bullet C2) + (D1 \bullet D2)}$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	F	t _{PLH}	0.211 + 0.010N _{std}	0.142 + 0.007N _{std}	0.089 + 0.005N _{std}
		t _{PHL}	0.250 + 0.005N _{std}	0.161 + 0.003N _{std}	0.109 + 0.002N _{std}
D2-Z		t _{PLH}	0.241 + 0.010N _{std}	0.159 + 0.007N _{std}	0.102 + 0.005N _{std}
		t _{PHL}	0.276 + 0.005N _{std}	0.174 + 0.003N _{std}	0.124 + 0.002N _{std}
A1-Z	H	t _{PLH}	0.214 + 0.008N _{std}	0.146 + 0.005N _{std}	0.091 + 0.004N _{std}
		t _{PHL}	0.250 + 0.005N _{std}	0.159 + 0.003N _{std}	0.103 + 0.002N _{std}
D2-Z		t _{PLH}	0.245 + 0.008N _{std}	0.162 + 0.005N _{std}	0.102 + 0.004N _{std}
		t _{PHL}	0.257 + 0.005N _{std}	0.160 + 0.003N _{std}	0.110 + 0.002N _{std}
A1-Z	I	t _{PLH}	0.228 + 0.005N _{std}	0.156 + 0.004N _{std}	0.097 + 0.003N _{std}
		t _{PHL}	0.239 + 0.004N _{std}	0.152 + 0.003N _{std}	0.100 + 0.002N _{std}
D2-Z		t _{PLH}	0.260 + 0.005N _{std}	0.173 + 0.004N _{std}	0.109 + 0.003N _{std}
		t _{PHL}	0.250 + 0.004N _{std}	0.156 + 0.003N _{std}	0.107 + 0.002N _{std}

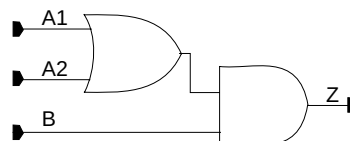
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	F	H	I
A1	0.864	0.967	0.983
A2	0.874	0.982	0.998
B1	0.891	0.998	1.014
B2	0.933	1.036	1.052
C1	0.863	0.966	0.982
C2	0.874	0.982	0.997
D1	0.891	0.998	1.014
D2	0.910	1.014	1.030
Internal	6.211	7.157	7.917
Cell Units	16 cells	16 cells	16 cells

Cell: OA21

Function: 2x1 OR AND

Boolean Expression: $Z = (A1 + A2) \bullet B$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	B	t _{PLH}	0.128 + 0.074N _{std}	0.080 + 0.047N _{std}	0.051 + 0.032N _{std}
		t _{PHL}	0.191 + 0.037N _{std}	0.131 + 0.024N _{std}	0.097 + 0.017N _{std}
B-Z		t _{PLH}	0.141 + 0.074N _{std}	0.087 + 0.047N _{std}	0.029 + 0.032N _{std}
		t _{PHL}	0.157 + 0.036N _{std}	0.113 + 0.023N _{std}	0.094 + 0.016N _{std}
A1-Z	C	t _{PLH}	0.137 + 0.035N _{std}	0.085 + 0.023N _{std}	0.054 + 0.017N _{std}
		t _{PHL}	0.205 + 0.026N _{std}	0.142 + 0.017N _{std}	0.105 + 0.012N _{std}
B-Z		t _{PLH}	0.149 + 0.035N _{std}	0.091 + 0.023N _{std}	0.027 + 0.017N _{std}
		t _{PHL}	0.185 + 0.026N _{std}	0.132 + 0.017N _{std}	0.106 + 0.012N _{std}
A1-Z	D	t _{PLH}	0.158 + 0.022N _{std}	0.098 + 0.015N _{std}	0.065 + 0.011N _{std}
		t _{PHL}	0.201 + 0.016N _{std}	0.140 + 0.011N _{std}	0.103 + 0.008N _{std}
B-Z		t _{PLH}	0.170 + 0.022N _{std}	0.104 + 0.015N _{std}	0.031 + 0.011N _{std}
		t _{PHL}	0.212 + 0.017N _{std}	0.149 + 0.011N _{std}	0.116 + 0.008N _{std}
A1-Z	E	t _{PLH}	0.174 + 0.016N _{std}	0.109 + 0.011N _{std}	0.074 + 0.008N _{std}
		t _{PHL}	0.200 + 0.012N _{std}	0.140 + 0.008N _{std}	0.103 + 0.006N _{std}
B-Z		t _{PLH}	0.188 + 0.016N _{std}	0.115 + 0.011N _{std}	0.034 + 0.008N _{std}
		t _{PHL}	0.240 + 0.012N _{std}	0.168 + 0.008N _{std}	0.128 + 0.006N _{std}
A1-Z	F	t _{PLH}	0.168 + 0.010N _{std}	0.108 + 0.007N _{std}	0.075 + 0.005N _{std}
		t _{PHL}	0.196 + 0.007N _{std}	0.139 + 0.005N _{std}	0.103 + 0.004N _{std}
B-Z		t _{PLH}	0.182 + 0.010N _{std}	0.113 + 0.007N _{std}	0.034 + 0.005N _{std}
		t _{PHL}	0.233 + 0.007N _{std}	0.166 + 0.005N _{std}	0.129 + 0.003N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	H	t _{PLH}	0.161 + 0.007N _{std}	0.105 + 0.005N _{std}	0.073 + 0.004N _{std}
		t _{PHL}	0.191 + 0.005N _{std}	0.137 + 0.004N _{std}	0.102 + 0.003N _{std}
B-Z		t _{PLH}	0.174 + 0.007N _{std}	0.109 + 0.005N _{std}	0.032 + 0.004N _{std}
		t _{PHL}	0.232 + 0.006N _{std}	0.167 + 0.004N _{std}	0.130 + 0.003N _{std}
A1-Z	I	t _{PLH}	0.159 + 0.005N _{std}	0.103 + 0.004N _{std}	0.072 + 0.003N _{std}
		t _{PHL}	0.188 + 0.004N _{std}	0.135 + 0.003N _{std}	0.100 + 0.002N _{std}
B-Z		t _{PLH}	0.172 + 0.005N _{std}	0.108 + 0.004N _{std}	0.032 + 0.003N _{std}
		t _{PHL}	0.228 + 0.004N _{std}	0.166 + 0.003N _{std}	0.130 + 0.002N _{std}
A1-Z	J	t _{PLH}	0.151 + 0.004N _{std}	0.098 + 0.003N _{std}	0.068 + 0.002N _{std}
		t _{PHL}	0.189 + 0.003N _{std}	0.136 + 0.002N _{std}	0.102 + 0.001N _{std}
B-Z		t _{PLH}	0.169 + 0.004N _{std}	0.106 + 0.003N _{std}	0.059 + 0.002N _{std}
		t _{PHL}	0.237 + 0.003N _{std}	0.172 + 0.002N _{std}	0.124 + 0.001N _{std}
A1-Z	K	t _{PLH}	0.152 + 0.003N _{std}	0.099 + 0.002N _{std}	0.069 + 0.001N _{std}
		t _{PHL}	0.186 + 0.002N _{std}	0.134 + 0.001N _{std}	0.100 + 0.001N _{std}
B-Z		t _{PLH}	0.170 + 0.003N _{std}	0.106 + 0.002N _{std}	0.059 + 0.001N _{std}
		t _{PHL}	0.234 + 0.002N _{std}	0.170 + 0.001N _{std}	0.124 + 0.001N _{std}



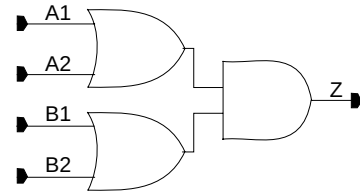
Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins				
	A1	A2	B	Internal	Cell Units
B	0.329	0.315	0.452	1.221	7 cells
C	0.343	0.332	0.452	1.474	7 cells
D	0.370	0.363	0.451	1.845	7 cells
E	0.402	0.398	0.455	2.250	7 cells
F	0.525	0.528	0.592	3.314	7 cells
H	0.668	0.675	0.740	4.303	7 cells
I	0.854	0.869	0.916	5.675	7 cells
J	1.364	1.444	1.049	8.773	15 cells
K	1.728	1.826	1.308	11.414	15 cells

Cell: OA22

Function: 2x2 OR AND

Boolean Expression: $Z = (A1 + A2) \bullet (B1 + B2)$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	B	t _{PLH}	0.165 + 0.068N _{std}	0.104 + 0.044N _{std}	0.054 + 0.030N _{std}
		t _{PHL}	0.171 + 0.038N _{std}	0.120 + 0.024N _{std}	0.085 + 0.017N _{std}
B2-Z		t _{PLH}	0.197 + 0.067N _{std}	0.122 + 0.044N _{std}	0.070 + 0.030N _{std}
		t _{PHL}	0.212 + 0.038N _{std}	0.144 + 0.024N _{std}	0.101 + 0.017N _{std}
A1-Z	C	t _{PLH}	0.161 + 0.035N _{std}	0.101 + 0.023N _{std}	0.052 + 0.017N _{std}
		t _{PHL}	0.183 + 0.025N _{std}	0.129 + 0.016N _{std}	0.091 + 0.011N _{std}
B2-Z		t _{PLH}	0.189 + 0.035N _{std}	0.117 + 0.023N _{std}	0.067 + 0.017N _{std}
		t _{PHL}	0.220 + 0.025N _{std}	0.150 + 0.016N _{std}	0.104 + 0.011N _{std}
A1-Z	D	t _{PLH}	0.161 + 0.023N _{std}	0.103 + 0.016N _{std}	0.053 + 0.011N _{std}
		t _{PHL}	0.186 + 0.016N _{std}	0.131 + 0.011N _{std}	0.092 + 0.008N _{std}
B2-Z		t _{PLH}	0.188 + 0.023N _{std}	0.117 + 0.016N _{std}	0.068 + 0.011N _{std}
		t _{PHL}	0.218 + 0.016N _{std}	0.149 + 0.011N _{std}	0.104 + 0.008N _{std}
A1-Z	E	t _{PLH}	0.160 + 0.017N _{std}	0.102 + 0.012N _{std}	0.052 + 0.009N _{std}
		t _{PHL}	0.189 + 0.012N _{std}	0.134 + 0.008N _{std}	0.094 + 0.006N _{std}
B2-Z		t _{PLH}	0.185 + 0.017N _{std}	0.116 + 0.012N _{std}	0.067 + 0.008N _{std}
		t _{PHL}	0.220 + 0.012N _{std}	0.151 + 0.008N _{std}	0.106 + 0.006N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	F	t _{PLH}	0.157 + 0.011N _{std}	0.101 + 0.007N _{std}	0.052 + 0.005N _{std}
		t _{PHL}	0.189 + 0.008N _{std}	0.136 + 0.005N _{std}	0.096 + 0.004N _{std}
B2-Z		t _{PLH}	0.180 + 0.010N _{std}	0.114 + 0.007N _{std}	0.066 + 0.005N _{std}
		t _{PHL}	0.217 + 0.008N _{std}	0.151 + 0.005N _{std}	0.106 + 0.004N _{std}
A1-Z	H	t _{PLH}	0.154 + 0.008N _{std}	0.099 + 0.005N _{std}	0.051 + 0.004N _{std}
		t _{PHL}	0.186 + 0.006N _{std}	0.134 + 0.004N _{std}	0.095 + 0.003N _{std}
B2-Z		t _{PLH}	0.178 + 0.008N _{std}	0.112 + 0.005N _{std}	0.065 + 0.004N _{std}
		t _{PHL}	0.215 + 0.006N _{std}	0.150 + 0.004N _{std}	0.105 + 0.003N _{std}
A1-Z	I	t _{PLH}	0.169 + 0.005N _{std}	0.109 + 0.004N _{std}	0.058 + 0.003N _{std}
		t _{PHL}	0.207 + 0.004N _{std}	0.149 + 0.003N _{std}	0.105 + 0.002N _{std}
B2-Z		t _{PLH}	0.191 + 0.005N _{std}	0.121 + 0.004N _{std}	0.071 + 0.003N _{std}
		t _{PHL}	0.235 + 0.004N _{std}	0.163 + 0.003N _{std}	0.115 + 0.002N _{std}
A1-Z	J	t _{PLH}	0.169 + 0.004N _{std}	0.109 + 0.003N _{std}	0.057 + 0.002N _{std}
		t _{PHL}	0.202 + 0.003N _{std}	0.145 + 0.002N _{std}	0.103 + 0.001N _{std}
B2-Z		t _{PLH}	0.192 + 0.004N _{std}	0.121 + 0.003N _{std}	0.071 + 0.002N _{std}
		t _{PHL}	0.231 + 0.003N _{std}	0.161 + 0.002N _{std}	0.113 + 0.001N _{std}
A1-Z	K	t _{PLH}	0.175 + 0.003N _{std}	0.113 + 0.002N _{std}	0.060 + 0.001N _{std}
		t _{PHL}	0.206 + 0.002N _{std}	0.149 + 0.001N _{std}	0.105 + 0.001N _{std}
B2-Z		t _{PLH}	0.197 + 0.003N _{std}	0.124 + 0.002N _{std}	0.073 + 0.001N _{std}
		t _{PHL}	0.236 + 0.002N _{std}	0.164 + 0.001N _{std}	0.115 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

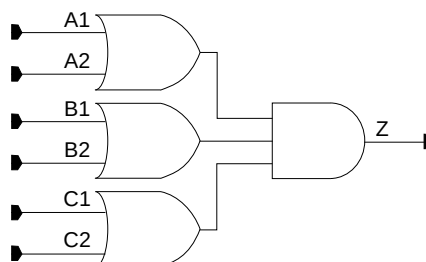
Performance Level	Input Pins					
	A1	A2	B1	B2	Internal	Cell Units
B	0.351	0.397	0.393	0.354	1.544	8 cells
C	0.401	0.446	0.446	0.406	1.927	8 cells
D	0.463	0.509	0.514	0.471	2.419	8 cells
E	0.530	0.576	0.586	0.541	2.923	8 cells
F	0.705	0.740	0.773	0.719	4.086	8 cells
H	0.912	0.944	0.977	0.928	5.317	8 cells
I	0.919	0.951	0.983	0.934	6.372	8 cells
J	1.453	1.540	1.478	1.538	9.657	18 cells
K	1.777	1.879	1.811	1.882	12.746	18 cells

Cell: OA222

Function: 2x2x2 OR AND

Boolean Expression:

$$Z = (A1 + A2) \bullet (B1 + B2) \bullet (C1 + C2)$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	B	t _{PLH}	0.125 + 0.063N _{std}	0.079 + 0.042N _{std}	0.048 + 0.030N _{std}
		t _{PHL}	0.215 + 0.036N _{std}	0.146 + 0.023N _{std}	0.107 + 0.017N _{std}
C2-Z		t _{PLH}	0.192 + 0.063N _{std}	0.119 + 0.042N _{std}	0.070 + 0.030N _{std}
		t _{PHL}	0.295 + 0.039N _{std}	0.192 + 0.026N _{std}	0.132 + 0.018N _{std}
A1-Z	C	t _{PLH}	0.146 + 0.029N _{std}	0.091 + 0.020N _{std}	0.058 + 0.014N _{std}
		t _{PHL}	0.231 + 0.021N _{std}	0.158 + 0.014N _{std}	0.116 + 0.010N _{std}
C2-Z		t _{PLH}	0.226 + 0.029N _{std}	0.138 + 0.020N _{std}	0.079 + 0.014N _{std}
		t _{PHL}	0.287 + 0.022N _{std}	0.190 + 0.015N _{std}	0.131 + 0.010N _{std}
A1-Z	D	t _{PLH}	0.151 + 0.018N _{std}	0.098 + 0.012N _{std}	0.066 + 0.009N _{std}
		t _{PHL}	0.199 + 0.013N _{std}	0.138 + 0.008N _{std}	0.103 + 0.006N _{std}
C2-Z		t _{PLH}	0.251 + 0.018N _{std}	0.155 + 0.012N _{std}	0.089 + 0.009N _{std}
		t _{PHL}	0.244 + 0.013N _{std}	0.164 + 0.009N _{std}	0.112 + 0.006N _{std}
A1-Z	E	t _{PLH}	0.149 + 0.014N _{std}	0.097 + 0.009N _{std}	0.065 + 0.007N _{std}
		t _{PHL}	0.199 + 0.009N _{std}	0.139 + 0.006N _{std}	0.104 + 0.004N _{std}
C2-Z		t _{PLH}	0.242 + 0.014N _{std}	0.150 + 0.009N _{std}	0.087 + 0.007N _{std}
		t _{PHL}	0.241 + 0.010N _{std}	0.162 + 0.006N _{std}	0.111 + 0.005N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	F	t _{PLH}	0.142 + 0.010N _{std}	0.092 + 0.007N _{std}	0.062 + 0.005N _{std}
		t _{PHL}	0.195 + 0.007N _{std}	0.137 + 0.005N _{std}	0.102 + 0.003N _{std}
C2-Z		t _{PLH}	0.226 + 0.010N _{std}	0.141 + 0.007N _{std}	0.082 + 0.005N _{std}
		t _{PHL}	0.234 + 0.007N _{std}	0.159 + 0.005N _{std}	0.109 + 0.003N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

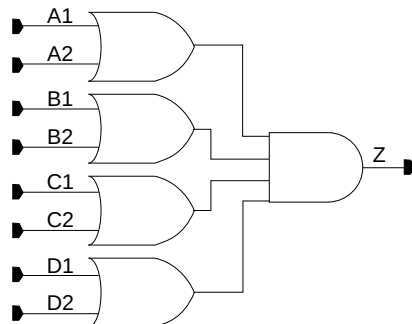
Input Pins	Performance Level				
	B	C	D	E	F
A1	0.328	0.362	0.527	0.638	0.828
A2	0.318	0.359	0.535	0.648	0.843
B1	0.338	0.376	0.539	0.648	0.833
B2	0.334	0.374	0.545	0.657	0.849
C1	0.372	0.409	0.579	0.692	0.882
C2	0.307	0.349	0.527	0.641	0.835
Internal	1.591	2.300	3.712	4.637	5.996
Cell Units	14 cells	14 cells	15 cells	15 cells	15 cells

Cell: OA2222

Function: 2x2x2x2 OR

Boolean Expression:

$$Z = (A1 + A2) \bullet (B1 + B2) \bullet (C1 + C2) \bullet (D1 + D2)$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	B	t _{PLH}	0.177 + 0.063N _{std}	0.109 + 0.042N _{std}	0.056 + 0.030N _{std}
		t _{PHL}	0.251 + 0.037N _{std}	0.170 + 0.023N _{std}	0.119 + 0.016N _{std}
D2-Z		t _{PLH}	0.197 + 0.063N _{std}	0.121 + 0.041N _{std}	0.069 + 0.029N _{std}
		t _{PHL}	0.300 + 0.038N _{std}	0.197 + 0.024N _{std}	0.137 + 0.016N _{std}
A1-Z	C	t _{PLH}	0.207 + 0.029N _{std}	0.129 + 0.020N _{std}	0.069 + 0.014N _{std}
		t _{PHL}	0.261 + 0.022N _{std}	0.176 + 0.014N _{std}	0.121 + 0.010N _{std}
D2-Z		t _{PLH}	0.226 + 0.029N _{std}	0.138 + 0.020N _{std}	0.079 + 0.014N _{std}
		t _{PHL}	0.287 + 0.022N _{std}	0.190 + 0.015N _{std}	0.131 + 0.010N _{std}
A1-Z	D	t _{PLH}	0.226 + 0.018N _{std}	0.143 + 0.012N _{std}	0.078 + 0.009N _{std}
		t _{PHL}	0.229 + 0.013N _{std}	0.156 + 0.008N _{std}	0.107 + 0.006N _{std}
D2-Z		t _{PLH}	0.249 + 0.018N _{std}	0.154 + 0.012N _{std}	0.089 + 0.009N _{std}
		t _{PHL}	0.243 + 0.013N _{std}	0.163 + 0.009N _{std}	0.111 + 0.006N _{std}
A1-Z	E	t _{PLH}	0.222 + 0.014N _{std}	0.141 + 0.009N _{std}	0.077 + 0.007N _{std}
		t _{PHL}	0.228 + 0.010N _{std}	0.157 + 0.006N _{std}	0.108 + 0.005N _{std}
D2-Z		t _{PLH}	0.240 + 0.014N _{std}	0.149 + 0.009N _{std}	0.087 + 0.007N _{std}
		t _{PHL}	0.239 + 0.010N _{std}	0.162 + 0.006N _{std}	0.111 + 0.005N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	F	t _{PLH}	0.211 + 0.010N _{std}	0.134 + 0.007N _{std}	0.073 + 0.005N _{std}
		t _{PHL}	0.223 + 0.007N _{std}	0.154 + 0.005N _{std}	0.106 + 0.003N _{std}
D2-Z		t _{PLH}	0.225 + 0.010N _{std}	0.141 + 0.007N _{std}	0.082 + 0.005N _{std}
		t _{PHL}	0.233 + 0.007N _{std}	0.158 + 0.005N _{std}	0.109 + 0.003N _{std}

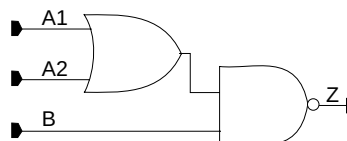
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level				
	B	C	D	E	F
A1	0.338	0.376	0.539	0.649	0.834
A2	0.334	0.375	0.544	0.656	0.848
B1	0.373	0.410	0.580	0.693	0.883
B2	0.309	0.352	0.527	0.641	0.836
C1	0.337	0.375	0.539	0.648	0.833
C2	0.334	0.375	0.544	0.656	0.847
D1	0.372	0.409	0.580	0.692	0.882
D2	0.308	0.350	0.527	0.641	0.836
Internal	1.614	2.425	3.875	4.846	6.269
Cell Units	17 cells	17 cells	17 cells	17 cells	17 cells

Cell: OAI21

Function: 2x1 OR AND Invert

Boolean Expression: $Z = \overline{(A1 + A2) \bullet B}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	A	t _{PLH}	0.106 + 0.095N _{std}	0.079 + 0.062N _{std}	0.064 + 0.043N _{std}
		t _{PHL}	0.072 + 0.056N _{std}	0.047 + 0.034N _{std}	0.031 + 0.024N _{std}
B-Z		t _{PLH}	0.108 + 0.066N _{std}	0.083 + 0.043N _{std}	0.076 + 0.030N _{std}
		t _{PHL}	0.082 + 0.055N _{std}	0.052 + 0.034N _{std}	0.010 + 0.014N _{std}
A1-Z	B	t _{PLH}	0.095 + 0.053N _{std}	0.074 + 0.035N _{std}	0.060 + 0.025N _{std}
		t _{PHL}	0.071 + 0.033N _{std}	0.045 + 0.021N _{std}	0.028 + 0.015N _{std}
B-Z		t _{PLH}	0.102 + 0.039N _{std}	0.081 + 0.026N _{std}	0.076 + 0.018N _{std}
		t _{PHL}	0.082 + 0.033N _{std}	0.050 + 0.021N _{std}	0.006 + 0.009N _{std}
A1-Z	C	t _{PLH}	0.092 + 0.026N _{std}	0.071 + 0.018N _{std}	0.057 + 0.013N _{std}
		t _{PHL}	0.069 + 0.017N _{std}	0.045 + 0.011N _{std}	0.029 + 0.008N _{std}
B-Z		t _{PLH}	0.102 + 0.020N _{std}	0.081 + 0.014N _{std}	0.076 + 0.010N _{std}
		t _{PHL}	0.079 + 0.017N _{std}	0.049 + 0.011N _{std}	0.007 + 0.005N _{std}
A1-Z	D	t _{PLH}	0.096 + 0.017N _{std}	0.075 + 0.012N _{std}	0.061 + 0.009N _{std}
		t _{PHL}	0.072 + 0.011N _{std}	0.047 + 0.007N _{std}	0.031 + 0.005N _{std}
B-Z		t _{PLH}	0.113 + 0.014N _{std}	0.090 + 0.010N _{std}	0.074 + 0.007N _{std}
		t _{PHL}	0.089 + 0.012N _{std}	0.057 + 0.008N _{std}	0.031 + 0.005N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	E	t _{PLH}	0.093 + 0.012N _{std}	0.074 + 0.008N _{std}	0.060 + 0.006N _{std}
		t _{PHL}	0.075 + 0.008N _{std}	0.050 + 0.005N _{std}	0.034 + 0.004N _{std}
B-Z		t _{PLH}	0.121 + 0.011N _{std}	0.097 + 0.008N _{std}	0.081 + 0.006N _{std}
		t _{PHL}	0.085 + 0.008N _{std}	0.053 + 0.005N _{std}	0.028 + 0.003N _{std}
A1-Z	F	t _{PLH}	0.090 + 0.008N _{std}	0.072 + 0.005N _{std}	0.058 + 0.004N _{std}
		t _{PHL}	0.078 + 0.006N _{std}	0.053 + 0.004N _{std}	0.038 + 0.003N _{std}
B-Z		t _{PLH}	0.106 + 0.006N _{std}	0.086 + 0.004N _{std}	0.071 + 0.003N _{std}
		t _{PHL}	0.087 + 0.006N _{std}	0.055 + 0.004N _{std}	0.031 + 0.002N _{std}
A1-Z	H	t _{PLH}	0.092 + 0.006N _{std}	0.068 + 0.004N _{std}	0.052 + 0.003N _{std}
		t _{PHL}	0.088 + 0.004N _{std}	0.059 + 0.003N _{std}	0.042 + 0.002N _{std}
B-Z		t _{PLH}	0.100 + 0.004N _{std}	0.081 + 0.003N _{std}	0.068 + 0.002N _{std}
		t _{PHL}	0.073 + 0.004N _{std}	0.047 + 0.003N _{std}	0.034 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

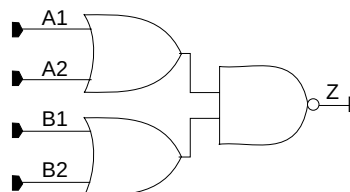
Performance Level	Input Pins				
	A1	A2	B	Internal	Cell Units
A	0.351	0.354	0.453	0.790	5 cells
B	0.486	0.496	0.617	1.203	5 cells
C	0.820	0.835	1.018	2.128	5 cells
D	1.298	1.255	0.929	3.140	7 cells
E	1.717	1.758	1.311	4.251	7 cells
F	2.392	2.479	1.971	6.179	10 cells
H	3.325	3.311	2.682	8.237	13 cells

Cell: OAI22

Function: 2x2 OR AND Invert

Boolean Expression:

$$Z = \overline{(A1 + A2) \bullet (B1 + B2)}$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	A	t _{PLH}	0.100 + 0.067N _{std}	0.076 + 0.045N _{std}	0.060 + 0.032N _{std}
		t _{PHL}	0.099 + 0.052N _{std}	0.066 + 0.032N _{std}	0.034 + 0.019N _{std}
B2-Z		t _{PLH}	0.132 + 0.068N _{std}	0.095 + 0.045N _{std}	0.071 + 0.032N _{std}
		t _{PHL}	0.127 + 0.053N _{std}	0.080 + 0.032N _{std}	0.045 + 0.018N _{std}
A1-Z	B	t _{PLH}	0.094 + 0.038N _{std}	0.073 + 0.026N _{std}	0.057 + 0.019N _{std}
		t _{PHL}	0.100 + 0.030N _{std}	0.065 + 0.019N _{std}	0.031 + 0.012N _{std}
B2-Z		t _{PLH}	0.119 + 0.038N _{std}	0.086 + 0.026N _{std}	0.065 + 0.018N _{std}
		t _{PHL}	0.123 + 0.030N _{std}	0.077 + 0.019N _{std}	0.042 + 0.011N _{std}
A1-Z	C	t _{PLH}	0.097 + 0.019N _{std}	0.074 + 0.013N _{std}	0.057 + 0.009N _{std}
		t _{PHL}	0.105 + 0.016N _{std}	0.069 + 0.010N _{std}	0.035 + 0.006N _{std}
B2-Z		t _{PLH}	0.118 + 0.019N _{std}	0.085 + 0.013N _{std}	0.063 + 0.009N _{std}
		t _{PHL}	0.124 + 0.016N _{std}	0.078 + 0.010N _{std}	0.045 + 0.006N _{std}
A1-Z	D	t _{PLH}	0.098 + 0.013N _{std}	0.076 + 0.009N _{std}	0.059 + 0.006N _{std}
		t _{PHL}	0.103 + 0.010N _{std}	0.068 + 0.007N _{std}	0.035 + 0.004N _{std}
B2-Z		t _{PLH}	0.119 + 0.013N _{std}	0.087 + 0.009N _{std}	0.065 + 0.006N _{std}
		t _{PHL}	0.122 + 0.010N _{std}	0.077 + 0.006N _{std}	0.045 + 0.004N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	E	t _{PLH}	0.096 + 0.010N _{std}	0.075 + 0.007N _{std}	0.059 + 0.005N _{std}
		t _{PHL}	0.102 + 0.008N _{std}	0.068 + 0.005N _{std}	0.035 + 0.003N _{std}
B2-Z		t _{PLH}	0.117 + 0.010N _{std}	0.086 + 0.007N _{std}	0.065 + 0.005N _{std}
		t _{PHL}	0.120 + 0.008N _{std}	0.076 + 0.005N _{std}	0.045 + 0.003N _{std}
A1-Z	F	t _{PLH}	0.094 + 0.006N _{std}	0.075 + 0.004N _{std}	0.059 + 0.003N _{std}
		t _{PHL}	0.102 + 0.004N _{std}	0.068 + 0.003N _{std}	0.035 + 0.002N _{std}
B2-Z		t _{PLH}	0.116 + 0.006N _{std}	0.085 + 0.004N _{std}	0.065 + 0.003N _{std}
		t _{PHL}	0.121 + 0.004N _{std}	0.077 + 0.003N _{std}	0.045 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

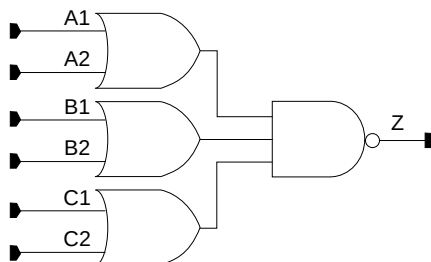
Input Pins	Performance Level					
	A	B	C	D	E	F
A1	0.400	0.570	1.007	1.540	1.965	3.333
A2	0.404	0.584	1.098	1.624	2.056	3.556
B1	0.441	0.617	1.025	1.578	2.007	3.314
B2	0.381	0.564	1.089	1.636	2.077	3.528
Internal	1.045	1.610	3.091	4.604	5.921	10.281
Cell Units	7 cells	7 cells	9 cells	13 cells	13 cells	18 cells

Cell: OAI222

Function: 2x2x OR AND Invert

Boolean Expression:

$$Z = \overline{(A1 + A2) \bullet (B1 + B2) \bullet (C1 + C2)}$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	E	t _{PLH}	0.262 + 0.016N _{std}	0.176 + 0.011N _{std}	0.128 + 0.008N _{std}
		t _{PHL}	0.197 + 0.012N _{std}	0.127 + 0.008N _{std}	0.084 + 0.006N _{std}
C2-Z		t _{PLH}	0.398 + 0.016N _{std}	0.257 + 0.011N _{std}	0.176 + 0.008N _{std}
		t _{PHL}	0.270 + 0.012N _{std}	0.170 + 0.008N _{std}	0.105 + 0.006N _{std}
A1-Z	H	t _{PLH}	0.243 + 0.008N _{std}	0.168 + 0.006N _{std}	0.125 + 0.004N _{std}
		t _{PHL}	0.185 + 0.006N _{std}	0.117 + 0.004N _{std}	0.076 + 0.003N _{std}
C2-Z		t _{PLH}	0.351 + 0.008N _{std}	0.232 + 0.006N _{std}	0.164 + 0.004N _{std}
		t _{PHL}	0.253 + 0.006N _{std}	0.157 + 0.004N _{std}	0.094 + 0.003N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

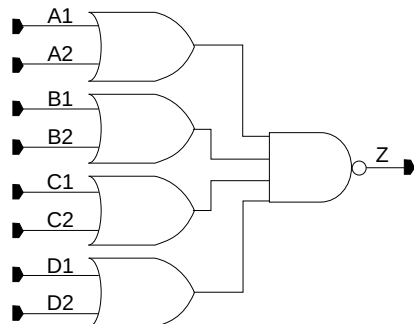
Input Pins	Performance Level	
	E	H
A1	0.338	0.519
A2	0.324	0.508
B1	0.373	0.572
B2	0.367	0.572
C1	0.410	0.615
C2	0.340	0.550
Internal	3.158	5.275
Cell Units	16 cells	16 cells

Cell: OAI2222

Function: 2x2x2x2 OR AND Invert

Boolean Expression:

$$Z = \overline{(A1 + A2) \bullet (B1 + B2) \bullet (C1 + C2) \bullet (D1 + D2)}$$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	E	t _{PLH}	0.307 + 0.016N _{std}	0.206 + 0.011N _{std}	0.144 + 0.008N _{std}
		t _{PHL}	0.234 + 0.012N _{std}	0.146 + 0.008N _{std}	0.082 + 0.006N _{std}
D2-Z		t _{PLH}	0.402 + 0.016N _{std}	0.260 + 0.011N _{std}	0.180 + 0.008N _{std}
		t _{PHL}	0.276 + 0.012N _{std}	0.170 + 0.008N _{std}	0.102 + 0.006N _{std}
A1-Z	H	t _{PLH}	0.279 + 0.008N _{std}	0.191 + 0.006N _{std}	0.135 + 0.004N _{std}
		t _{PHL}	0.218 + 0.006N _{std}	0.137 + 0.004N _{std}	0.076 + 0.003N _{std}
D2-Z		t _{PLH}	0.351 + 0.008N _{std}	0.232 + 0.006N _{std}	0.164 + 0.004N _{std}
		t _{PHL}	0.254 + 0.006N _{std}	0.158 + 0.004N _{std}	0.095 + 0.003N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	E	H
A1	0.370	0.570
A2	0.366	0.572
B1	0.410	0.617
B2	0.341	0.552
C1	0.370	0.570
C2	0.366	0.571
D1	0.408	0.613
D2	0.341	0.551
Internal	2.951	5.680
Cell Units	19 cells	19 cells

Standard Cell Unique Logic

Cell: ADDF

Function: Full Adder

Description:

This is a 3-bit adder with sum (SUM) and carry (COUT) as outputs.



Truth Table

Inputs			Outputs	
A	B	CIN	SUM	COUT
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
CIN- COUT	B	t _{PLH}	0.142 + 0.059N _{std}	0.091 + 0.038N _{std}	0.063 + 0.027N _{std}
		t _{PHL}	0.152 + 0.035N _{std}	0.104 + 0.022N _{std}	0.075 + 0.016N _{std}
B-SUM		t _{PLH}	0.251 + 0.059N _{std}	0.164 + 0.038N _{std}	0.116 + 0.026N _{std}
		t _{PHL}	0.314 + 0.038N _{std}	0.195 + 0.024N _{std}	0.130 + 0.017N _{std}
CIN- COUT	C	t _{PLH}	0.142 + 0.031N _{std}	0.092 + 0.021N _{std}	0.064 + 0.015N _{std}
		t _{PHL}	0.160 + 0.023N _{std}	0.110 + 0.015N _{std}	0.079 + 0.011N _{std}
B-SUM		t _{PLH}	0.251 + 0.031N _{std}	0.165 + 0.021N _{std}	0.117 + 0.015N _{std}
		t _{PHL}	0.327 + 0.020N _{std}	0.204 + 0.013N _{std}	0.136 + 0.009N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
CIN- COUT	D	t _{PLH}	0.154 + 0.021N _{std}	0.098 + 0.014N _{std}	0.068 + 0.010N _{std}
		t _{PHL}	0.173 + 0.016N _{std}	0.118 + 0.010N _{std}	0.085 + 0.008N _{std}
B-SUM		t _{PLH}	0.257 + 0.020N _{std}	0.169 + 0.014N _{std}	0.120 + 0.010N _{std}
		t _{PHL}	0.339 + 0.013N _{std}	0.212 + 0.009N _{std}	0.141 + 0.006N _{std}
CIN- COUT	E	t _{PLH}	0.162 + 0.015N _{std}	0.104 + 0.011N _{std}	0.072 + 0.008N _{std}
		t _{PHL}	0.181 + 0.011N _{std}	0.123 + 0.007N _{std}	0.089 + 0.005N _{std}
B-SUM		t _{PLH}	0.273 + 0.015N _{std}	0.178 + 0.010N _{std}	0.127 + 0.008N _{std}
		t _{PHL}	0.360 + 0.009N _{std}	0.225 + 0.006N _{std}	0.149 + 0.004N _{std}
CIN- COUT	F	t _{PLH}	0.210 + 0.008N _{std}	0.134 + 0.005N _{std}	0.093 + 0.004N _{std}
		t _{PHL}	0.213 + 0.004N _{std}	0.145 + 0.003N _{std}	0.103 + 0.002N _{std}
B-SUM		t _{PLH}	0.300 + 0.006N _{std}	0.197 + 0.004N _{std}	0.140 + 0.003N _{std}
		t _{PHL}	0.442 + 0.005N _{std}	0.279 + 0.003N _{std}	0.187 + 0.002N _{std}

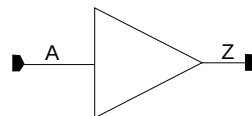
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level				
	B	C	D	E	F
A	1.263	1.308	1.353	1.352	1.504
B	0.874	0.874	0.873	0.873	0.915
CIN	1.245	1.243	1.275	1.275	1.401
Internal	4.853	5.182	5.696	6.193	9.550
Cell Units	24 cells	24 cells	24 cells	24 cells	25 cells

Cell: BUFFER

Function: Buffer

Boolean Expression: $Z = A$



Truth Table

Input	Output
A	Z
1	1
0	0

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-Z	C	t_{PLH}	$0.103 + 0.036N_{std}$	$0.066 + 0.024N_{std}$	$0.045 + 0.017N_{std}$
		t_{PHL}	$0.121 + 0.029N_{std}$	$0.089 + 0.018N_{std}$	$0.068 + 0.013N_{std}$
	D	t_{PLH}	$0.098 + 0.023N_{std}$	$0.064 + 0.016N_{std}$	$0.043 + 0.011N_{std}$
		t_{PHL}	$0.122 + 0.019N_{std}$	$0.090 + 0.012N_{std}$	$0.069 + 0.009N_{std}$
	E	t_{PLH}	$0.103 + 0.017N_{std}$	$0.068 + 0.012N_{std}$	$0.047 + 0.009N_{std}$
		t_{PHL}	$0.123 + 0.014N_{std}$	$0.091 + 0.009N_{std}$	$0.070 + 0.007N_{std}$
	F	t_{PLH}	$0.110 + 0.011N_{std}$	$0.073 + 0.008N_{std}$	$0.051 + 0.006N_{std}$
		t_{PHL}	$0.134 + 0.009N_{std}$	$0.098 + 0.006N_{std}$	$0.075 + 0.005N_{std}$
	H	t_{PLH}	$0.096 + 0.008N_{std}$	$0.062 + 0.006N_{std}$	$0.041 + 0.004N_{std}$
		t_{PHL}	$0.141 + 0.004N_{std}$	$0.106 + 0.003N_{std}$	$0.082 + 0.002N_{std}$
	I	t_{PLH}	$0.104 + 0.005N_{std}$	$0.069 + 0.004N_{std}$	$0.047 + 0.003N_{std}$
		t_{PHL}	$0.152 + 0.004N_{std}$	$0.114 + 0.003N_{std}$	$0.088 + 0.002N_{std}$
	J	t_{PLH}	$0.112 + 0.004N_{std}$	$0.074 + 0.003N_{std}$	$0.050 + 0.002N_{std}$
		t_{PHL}	$0.165 + 0.002N_{std}$	$0.123 + 0.002N_{std}$	$0.095 + 0.001N_{std}$
	K	t_{PLH}	$0.121 + 0.003N_{std}$	$0.081 + 0.002N_{std}$	$0.058 + 0.002N_{std}$
		t_{PHL}	$0.154 + 0.002N_{std}$	$0.115 + 0.002N_{std}$	$0.088 + 0.001N_{std}$

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	L	t _{PLH}	0.104 + 0.003N _{std}	0.070 + 0.002N _{std}	0.050 + 0.001N _{std}
		t _{PHL}	0.123 + 0.002N _{std}	0.092 + 0.001N _{std}	0.071 + 0.001N _{std}
	M	t _{PLH}	0.103 + 0.002N _{std}	0.070 + 0.001N _{std}	0.050 + 0.001N _{std}
		t _{PHL}	0.128 + 0.002N _{std}	0.096 + 0.001N _{std}	0.075 + 0.001N _{std}
	N	t _{PLH}	0.133 + 0.002N _{std}	0.092 + 0.001N _{std}	0.067 + 0.001N _{std}
		t _{PHL}	0.155 + 0.001N _{std}	0.115 + 0.001N _{std}	0.088 + 0.001N _{std}
	O	t _{PLH}	0.133 + 0.001N _{std}	0.091 + 0.001N _{std}	0.067 + 0.001N _{std}
		t _{PHL}	0.155 + 0.001N _{std}	0.115 + 0.001N _{std}	0.088 + 0.001N _{std}

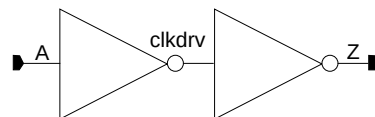
Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins		
	A	Internal	Cell Units
C	0.323	1.497	5 cells
D	0.385	1.937	5 cells
E	0.416	2.292	5 cells
F	0.471	2.910	5 cells
H	0.637	4.116	5 cells
I	0.683	4.988	5 cells
J	0.843	7.178	7 cells
K	0.962	8.299	7 cells
L	1.802	11.518	7 cells
M	1.955	13.489	11 cells
N	1.626	15.150	13 cells
O	1.890	17.886	13 cells

Cell: CLK

Function: Clock Driver

Boolean Expression: $Z = A$



Truth Table

Input	Output
A	Z
1	1
0	0

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-Z	I	t_{PLH}	$0.170 + 0.004N_{std}$	$0.111 + 0.002N_{std}$	$0.081 + 0.002N_{std}$
		t_{PHL}	$0.139 + 0.004N_{std}$	$0.102 + 0.002N_{std}$	$0.076 + 0.002N_{std}$
	K	t_{PLH}	$0.192 + 0.002N_{std}$	$0.126 + 0.001N_{std}$	$0.091 + 0.001N_{std}$
		t_{PHL}	$0.158 + 0.002N_{std}$	$0.115 + 0.001N_{std}$	$0.086 + 0.001N_{std}$
	M	t_{PLH}	$0.179 + 0.001N_{std}$	$0.117 + 0.001N_{std}$	$0.085 + 0.001N_{std}$
		t_{PHL}	$0.152 + 0.001N_{std}$	$0.111 + 0.001N_{std}$	$0.082 + 0.001N_{std}$
	O	t_{PLH}	$0.182 + 0.001N_{std}$	$0.119 + 0.001N_{std}$	$0.086 + 0.000N_{std}$
		t_{PHL}	$0.160 + 0.001N_{std}$	$0.116 + 0.001N_{std}$	$0.086 + 0.000N_{std}$
	Q	t_{PLH}	$0.186 + 0.001N_{std}$	$0.122 + 0.000N_{std}$	$0.089 + 0.000N_{std}$
		t_{PHL}	$0.163 + 0.001N_{std}$	$0.117 + 0.000N_{std}$	$0.087 + 0.000N_{std}$

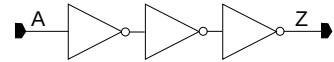
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level				
	I	K	M	O	Q
A	1.125	1.476	2.589	3.412	4.806
Internal	7.415	12.382	21.206	29.733	42.739
Cell Units	7 cells	9 cells	16 cells	24 cells	31 cells

Cell: CLKI

Function: Inverting Clock Driver

Boolean Expression: $Z = \bar{A}$



Truth Table

Input	Output
A	Z
1	0
0	1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-Z	I	t_{PLH}	$0.203 + 0.004N_{std}$	$0.142 + 0.003N_{std}$	$0.103 + 0.002N_{std}$
		t_{PHL}	$0.234 + 0.004N_{std}$	$0.148 + 0.002N_{std}$	$0.104 + 0.002N_{std}$
	K	t_{PLH}	$0.225 + 0.002N_{std}$	$0.155 + 0.001N_{std}$	$0.112 + 0.001N_{std}$
		t_{PHL}	$0.256 + 0.002N_{std}$	$0.162 + 0.001N_{std}$	$0.114 + 0.001N_{std}$
	M	t_{PLH}	$0.230 + 0.001N_{std}$	$0.158 + 0.001N_{std}$	$0.114 + 0.001N_{std}$
		t_{PHL}	$0.256 + 0.001N_{std}$	$0.163 + 0.001N_{std}$	$0.115 + 0.001N_{std}$
	O	t_{PLH}	$0.232 + 0.001N_{std}$	$0.160 + 0.001N_{std}$	$0.116 + 0.000N_{std}$
		t_{PHL}	$0.257 + 0.001N_{std}$	$0.165 + 0.001N_{std}$	$0.117 + 0.000N_{std}$
	Q	t_{PLH}	$0.261 + 0.001N_{std}$	$0.179 + 0.000N_{std}$	$0.130 + 0.000N_{std}$
		t_{PHL}	$0.264 + 0.001N_{std}$	$0.169 + 0.000N_{std}$	$0.120 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level				
	I	K	M	O	Q
A	0.616	0.716	0.915	1.336	1.543
Internal	8.300	11.717	17.663	28.539	39.630
Cell Units	10 cells	12 cells	18 cells	25 cells	34 cells

Cell: CLKCHP

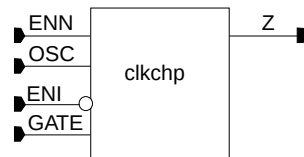
Function: Clock Chopper w/LSSD Test Features

Description:

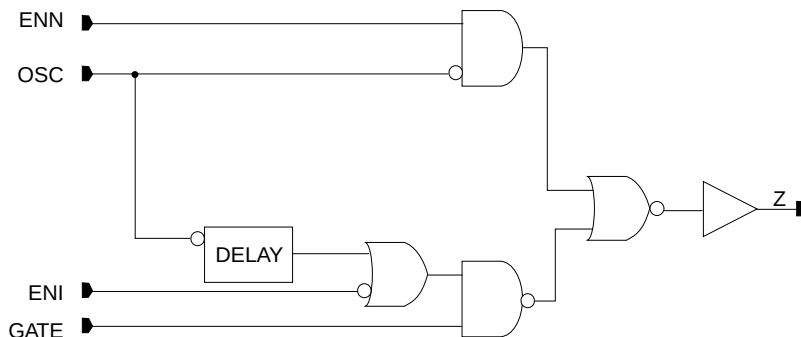
The clock chopper provides a pulse triggered from the signal input rise transition. Two non-overlapping clocks can be generated by feeding two clock choppers from true and complement values of a signal such as an oscillator. Clock separation is controlled by the frequency of the input.

The delay determines the falling edge of the pulse width and changes based on performance level selection. LSSD test is enabled by the use of signals ENN and ENI which enable the normal and delayed path so that each path can be independently checked for stuck fault.

GATE	Clock gating
OSC	Oscillator input
Z	Output
ENN	Gate noninverting path for test
ENI	Gate inverting (delayed) path for test



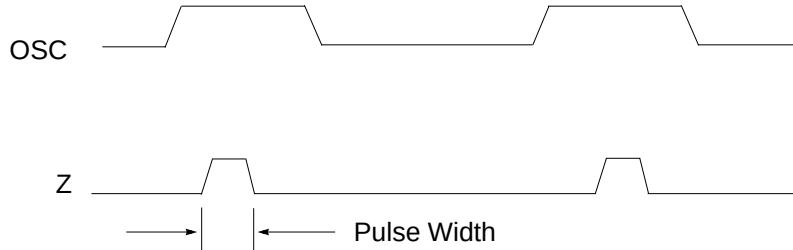
Logical Representation of Clock Chopper



Truth Table

Inputs				Output	Comments
GATE	OSC	ENN	ENI	Z	
1	0-to-1	1	1	0-to-1-to-0	Normal operation
1	X	1	1	0	Steady-state response
1	X	0	1	$\overline{\text{OSC}}$	Noninverting path disabled, inverting path enabled
1	X	1	0	OSC	Noninverting path enabled, inverting path disabled
1	X	0	0	1	Both paths disabled
0	X	X	X	0	Output disabled

Output Waveform



Waveform Calculation

Waveform ¹	Performance Level	Pulse Width in ns		
		$V_{dd} = 1.65V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^{\circ}C$ Process = Fast
PULSE WIDTH	M	$3.044 + 0.000N_{std}$	$1.889 + 0.000N_{std}$	$1.335 + 0.000N_{std}$
	Q	$2.097 + 0.000N_{std}$	$1.290 + 0.000N_{std}$	$0.909 + 0.000N_{std}$
	U	$1.132 + 0.000N_{std}$	$0.698 + 0.000N_{std}$	$0.488 + 0.000N_{std}$

¹. See Output Waveform diagram.



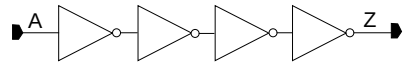
Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
OSC-Z	M	t _{PLH}	0.295 + 0.002N _{std}	0.193 + 0.001N _{std}	0.137 + 0.001N _{std}
		t _{PHL}	3.339 + 0.002N _{std}	2.082 + 0.001N _{std}	1.472 + 0.001N _{std}
	Q	t _{PLH}	0.299 + 0.002N _{std}	0.195 + 0.001N _{std}	0.137 + 0.001N _{std}
		t _{PHL}	2.396 + 0.002N _{std}	1.485 + 0.001N _{std}	1.046 + 0.001N _{std}
	U	t _{PLH}	0.299 + 0.002N _{std}	0.194 + 0.001N _{std}	0.137 + 0.001N _{std}
		t _{PHL}	1.431 + 0.002N _{std}	0.892 + 0.001N _{std}	0.625 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	M	Q	U
ENI	0.301	0.301	0.301
ENN	0.832	0.832	0.832
GATE	0.740	0.740	0.739
Internal	28.031	25.244	22.380
OSC	0.865	0.859	0.852
Cell Units	50 cells	41 cells	32 cells

Cell: CLKG
Function: Large Clock Driver
Boolean Expression: $Z = A$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (x) ¹		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	A	t _{PLH}	0.355 + 0.040x	0.221 + 0.028x	0.153 + 0.021x
		t _{PHL}	0.335 + 0.043x	0.220 + 0.028x	0.155 + 0.021x
	B	t _{PLH}	0.355 + 0.020x	0.222 + 0.014x	0.153 + 0.010x
		t _{PHL}	0.335 + 0.021x	0.220 + 0.014x	0.156 + 0.011x
	C	t _{PLH}	0.355 + 0.014x	0.222 + 0.009x	0.153 + 0.007x
		t _{PHL}	0.336 + 0.014x	0.221 + 0.009x	0.156 + 0.007x
	D	t _{PLH}	0.355 + 0.010x	0.222 + 0.007x	0.153 + 0.005x
		t _{PHL}	0.336 + 0.011x	0.220 + 0.007x	0.156 + 0.005x
	F	t _{PLH}	0.355 + 0.007x	0.222 + 0.005x	0.153 + 0.004x
		t _{PHL}	0.335 + 0.007x	0.220 + 0.005x	0.156 + 0.004x
	I	t _{PLH}	0.357 + 0.005x	0.222 + 0.004x	0.153 + 0.003x
		t _{PHL}	0.335 + 0.005x	0.221 + 0.004x	0.156 + 0.003x
	K	t _{PLH}	0.356 + 0.004x	0.222 + 0.002x	0.153 + 0.002x
		t _{PHL}	0.335 + 0.004x	0.220 + 0.002x	0.156 + 0.002x
	M	t _{PLH}	0.358 + 0.003x	0.223 + 0.002x	0.154 + 0.001x
		t _{PHL}	0.336 + 0.003x	0.221 + 0.002x	0.157 + 0.001x
	O	t _{PLH}	0.360 + 0.002x	0.224 + 0.001x	0.155 + 0.001x
		t _{PHL}	0.337 + 0.002x	0.221 + 0.001x	0.157 + 0.001x
	Q	t _{PLH}	0.362 + 0.002x	0.225 + 0.001x	0.156 + 0.001x
		t _{PHL}	0.338 + 0.001x	0.222 + 0.001x	0.158 + 0.001x
	S	t _{PLH}	0.365 + 0.001x	0.228 + 0.001x	0.159 + 0.001x
		t _{PHL}	0.343 + 0.001x	0.225 + 0.001x	0.160 + 0.000x



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (x) ¹		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	U	t _{PLH}	0.371 + 0.001x	0.232 + 0.001x	0.162 + 0.000x
		t _{PHL}	0.347 + 0.001x	0.228 + 0.000x	0.163 + 0.000x
	W	t _{PLH}	0.408 + 0.001x	0.257 + 0.001x	0.181 + 0.001x
		t _{PHL}	0.373 + 0.000x	0.244 + 0.000x	0.175 + 0.000x
	Y	t _{PLH}	0.404 + 0.001x	0.256 + 0.000x	0.183 + 0.000x
		t _{PHL}	0.378 + 0.000x	0.249 + 0.000x	0.181 + 0.000x

¹. Note the delay table uses x = 0.5 pF.

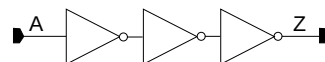
Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins		
	A	Internal	Cell Units
A	1.523	49.504	72 cells
B	3.972	99.817	168 cells
C	6.439	150.165	264 cells
D	8.902	200.207	360 cells
F	13.828	300.132	552 cells
I	18.739	399.606	744 cells
K	28.546	597.257	1128 cells
M	38.263	787.553	1512 cells
O	57.483	1179.856	2280 cells
Q	76.475	1559.629	3048 cells
S	113.375	2301.080	4584 cells
U	149.571	3020.061	6120 cells
W	221.250	4002.659	9192 cells
Y	292.500	5772.610	12264 cells

Cell: CLKGI

Function: Large Inverting Clock Driver

Boolean Expression: $Z = \bar{A}$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (x) ¹		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	A	t _{PLH}	0.328 + 0.043x	0.221 + 0.029x	0.159 + 0.021x
		t _{PHL}	0.333 + 0.041x	0.209 + 0.027x	0.145 + 0.020x
	B	t _{PLH}	0.328 + 0.021x	0.222 + 0.014x	0.160 + 0.011x
		t _{PHL}	0.333 + 0.020x	0.209 + 0.013x	0.145 + 0.010x
	C	t _{PLH}	0.328 + 0.014x	0.222 + 0.010x	0.159 + 0.007x
		t _{PHL}	0.334 + 0.014x	0.210 + 0.009x	0.145 + 0.007x
	D	t _{PLH}	0.328 + 0.011x	0.222 + 0.007x	0.160 + 0.005x
		t _{PHL}	0.333 + 0.010x	0.209 + 0.007x	0.145 + 0.005x
	E	t _{PLH}	0.328 + 0.009x	0.222 + 0.006x	0.160 + 0.004x
		t _{PHL}	0.333 + 0.008x	0.209 + 0.005x	0.145 + 0.004x
	F	t _{PLH}	0.328 + 0.007x	0.222 + 0.005x	0.160 + 0.004x
		t _{PHL}	0.333 + 0.007x	0.209 + 0.004x	0.145 + 0.003x
	H	t _{PLH}	0.328 + 0.006x	0.222 + 0.004x	0.160 + 0.003x
		t _{PHL}	0.333 + 0.006x	0.209 + 0.004x	0.145 + 0.003x
	I	t _{PLH}	0.328 + 0.006x	0.222 + 0.004x	0.160 + 0.003x
		t _{PHL}	0.333 + 0.005x	0.209 + 0.003x	0.145 + 0.002x
	J	t _{PLH}	0.328 + 0.005x	0.222 + 0.003x	0.160 + 0.002x
		t _{PHL}	0.333 + 0.004x	0.209 + 0.003x	0.145 + 0.002x
	K	t _{PLH}	0.328 + 0.004x	0.222 + 0.003x	0.160 + 0.002x
		t _{PHL}	0.333 + 0.003x	0.209 + 0.002x	0.145 + 0.002x
	L	t _{PLH}	0.328 + 0.003x	0.222 + 0.002x	0.160 + 0.002x
		t _{PHL}	0.333 + 0.003x	0.209 + 0.002x	0.145 + 0.001x



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (x) ¹		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-Z	M	t _{PLH}	0.330 + 0.003x	0.223 + 0.002x	0.161 + 0.002x
		t _{PHL}	0.334 + 0.003x	0.209 + 0.002x	0.145 + 0.001x
	N	t _{PLH}	0.329 + 0.002x	0.223 + 0.002x	0.160 + 0.001x
		t _{PHL}	0.334 + 0.002x	0.209 + 0.001x	0.145 + 0.001x
	O	t _{PLH}	0.330 + 0.002x	0.223 + 0.001x	0.161 + 0.001x
		t _{PHL}	0.335 + 0.002x	0.210 + 0.001x	0.146 + 0.001x
	P	t _{PLH}	0.331 + 0.002x	0.224 + 0.001x	0.161 + 0.001x
		t _{PHL}	0.335 + 0.001x	0.210 + 0.001x	0.146 + 0.001x
	Q	t _{PLH}	0.332 + 0.002x	0.225 + 0.001x	0.162 + 0.001x
		t _{PHL}	0.336 + 0.001x	0.211 + 0.001x	0.147 + 0.001x
	R	t _{PLH}	0.334 + 0.001x	0.226 + 0.001x	0.163 + 0.001x
		t _{PHL}	0.338 + 0.001x	0.212 + 0.001x	0.147 + 0.001x
	S	t _{PLH}	0.337 + 0.001x	0.227 + 0.001x	0.165 + 0.001x
		t _{PHL}	0.340 + 0.001x	0.214 + 0.001x	0.149 + 0.000x
	T	t _{PLH}	0.339 + 0.001x	0.229 + 0.001x	0.167 + 0.001x
		t _{PHL}	0.343 + 0.001x	0.215 + 0.000x	0.151 + 0.000x
	U	t _{PLH}	0.343 + 0.001x	0.232 + 0.001x	0.169 + 0.000x
		t _{PHL}	0.346 + 0.001x	0.218 + 0.000x	0.153 + 0.000x

¹. Note the delay table uses x = 0.5 pF.

Capacitance (in units of N_{std}) and Cell Sizes

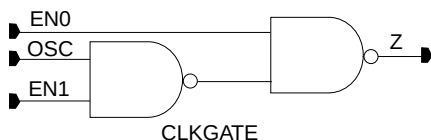
Performance Level	Input Pins		
	A	Internal	Cell Units
A	1.643	47.597	72 cells
B	4.224	96.036	168 cells
C	6.828	144.473	264 cells
D	9.422	192.588	360 cells
E	12.003	241.023	456 cells
F	14.601	288.886	552 cells
H	17.195	337.006	648 cells
I	19.780	384.529	744 cells
J	24.933	479.626	936 cells
K	30.100	574.806	1128 cells
L	35.175	669.379	1320 cells
M	40.258	756.539	1512 cells
N	50.358	950.355	1896 cells
O	60.300	1135.089	2280 cells
P	70.217	1319.839	2664 cells
Q	84.800	1592.564	3240 cells
R	99.196	1864.054	3816 cells
S	118.129	2223.141	4584 cells
T	139.188	2621.216	5448 cells
U	162.488	3060.020	6408 cells

Cell: CLKGATE

Function: Clock Gating Circuit

Description:

This circuit supplies repowering and clock gating functions. With the oscillator connected to OSC and both EN0 = 1 and EN1 = 1, the Z output follows the OSC input. If EN0 = 0, the Z output is forced high. If EN0 = 1 and EN1 = 0, the output is forced low. Timing rules provide setup and hold time requirements for the EN0 and EN1 signals relative to the OSC signal.



Boolean Expression: $Z = \overline{(\overline{OSC} \bullet \overline{EN1})} \bullet EN0$

Truth Table

Inputs			Output
OSC	EN1	EN0	Z
0	1	1	0
1	1	1	1
X	X	0	1
X	0	1	0

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (x) ¹		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
EN0-Z	A	t _{PLH}	0.256 + 0.171x	0.176 + 0.121x	0.129 + 0.090x
		t _{PHL}	0.233 + 0.175x	0.148 + 0.123x	0.102 + 0.094x
OSC-Z		t _{PLH}	0.311 + 0.169x	0.196 + 0.121x	0.135 + 0.090x
		t _{PHL}	0.301 + 0.178x	0.197 + 0.126x	0.139 + 0.096x
EN0-Z	B	t _{PLH}	0.278 + 0.090x	0.192 + 0.061x	0.141 + 0.045x
		t _{PHL}	0.264 + 0.092x	0.167 + 0.062x	0.115 + 0.047x
OSC-Z		t _{PLH}	0.343 + 0.090x	0.215 + 0.062x	0.148 + 0.046x
		t _{PHL}	0.336 + 0.093x	0.218 + 0.062x	0.153 + 0.047x

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (x) ¹		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
EN0-Z	C	t _{PLH}	0.231 + 0.040x	0.160 + 0.028x	0.117 + 0.021x
		t _{PHL}	0.257 + 0.043x	0.165 + 0.028x	0.116 + 0.021x
OSC-Z		t _{PLH}	0.365 + 0.040x	0.229 + 0.028x	0.158 + 0.021x
		t _{PHL}	0.343 + 0.043x	0.225 + 0.028x	0.159 + 0.021x
EN0-Z	D	t _{PLH}	0.231 + 0.020x	0.161 + 0.014x	0.118 + 0.010x
		t _{PHL}	0.258 + 0.021x	0.165 + 0.014x	0.116 + 0.011x
OSC-Z		t _{PLH}	0.366 + 0.020x	0.229 + 0.014x	0.159 + 0.010x
		t _{PHL}	0.344 + 0.021x	0.225 + 0.014x	0.159 + 0.011x
EN0-Z	E	t _{PLH}	0.231 + 0.010x	0.159 + 0.007x	0.117 + 0.005x
		t _{PHL}	0.257 + 0.011x	0.165 + 0.007x	0.116 + 0.005x
OSC-Z		t _{PLH}	0.366 + 0.010x	0.230 + 0.007x	0.159 + 0.005x
		t _{PHL}	0.344 + 0.011x	0.224 + 0.007x	0.159 + 0.005x
EN0-Z	F	t _{PLH}	0.231 + 0.007x	0.160 + 0.005x	0.117 + 0.003x
		t _{PHL}	0.257 + 0.007x	0.165 + 0.005x	0.116 + 0.004x
OSC-Z		t _{PLH}	0.366 + 0.007x	0.230 + 0.005x	0.159 + 0.003x
		t _{PHL}	0.344 + 0.007x	0.225 + 0.005x	0.159 + 0.004x
EN0-Z	I	t _{PLH}	0.231 + 0.005x	0.160 + 0.003x	0.117 + 0.003x
		t _{PHL}	0.257 + 0.005x	0.165 + 0.004x	0.115 + 0.003x
OSC-Z		t _{PLH}	0.366 + 0.005x	0.229 + 0.003x	0.158 + 0.003x
		t _{PHL}	0.343 + 0.005x	0.226 + 0.004x	0.159 + 0.003x
EN0-Z	K	t _{PLH}	0.229 + 0.003x	0.160 + 0.002x	0.117 + 0.002x
		t _{PHL}	0.257 + 0.004x	0.164 + 0.002x	0.115 + 0.002x
OSC-Z		t _{PLH}	0.366 + 0.003x	0.229 + 0.002x	0.158 + 0.002x
		t _{PHL}	0.343 + 0.004x	0.225 + 0.002x	0.159 + 0.002x



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (x) ¹		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
EN0-Z	M	t _{PLH}	0.229 + 0.003x	0.160 + 0.002x	0.117 + 0.001x
		t _{PHL}	0.256 + 0.003x	0.164 + 0.002x	0.115 + 0.001x
OSC-Z		t _{PLH}	0.366 + 0.003x	0.230 + 0.002x	0.158 + 0.001x
		t _{PHL}	0.343 + 0.003x	0.224 + 0.002x	0.158 + 0.001x
EN0-Z	O	t _{PLH}	0.230 + 0.002x	0.159 + 0.001x	0.116 + 0.001x
		t _{PHL}	0.256 + 0.002x	0.164 + 0.001x	0.115 + 0.001x
OSC-Z		t _{PLH}	0.366 + 0.002x	0.228 + 0.001x	0.158 + 0.001x
		t _{PHL}	0.343 + 0.002x	0.224 + 0.001x	0.158 + 0.001x
EN0-Z	Q	t _{PLH}	0.229 + 0.001x	0.159 + 0.001x	0.117 + 0.001x
		t _{PHL}	0.256 + 0.001x	0.164 + 0.001x	0.115 + 0.001x
OSC-Z		t _{PLH}	0.367 + 0.001x	0.228 + 0.001x	0.158 + 0.001x
		t _{PHL}	0.342 + 0.001x	0.224 + 0.001x	0.159 + 0.001x

¹. Note the delay table uses x = 0.5 pF.

Capacitance (in units of N_{std}) and Cell Sizes

Performance Level	Input Pins				
	EN0	EN1	Internal	OSC	Cell Units
A	0.585	0.487	14.592	0.504	20 cells
B	0.733	0.494	23.595	0.498	26 cells
C	1.977	0.939	50.372	0.926	72 cells
D	4.785	2.878	101.711	2.914	168 cells
E	10.438	6.777	204.294	6.888	360 cells
F	16.088	10.675	306.928	10.862	552 cells
I	21.742	14.572	409.475	14.836	744 cells
K	33.042	22.367	614.675	22.792	1128 cells
M	44.346	30.162	819.758	30.733	1512 cells
O	66.958	45.758	1230.133	46.629	2280 cells
Q	89.571	61.346	1640.600	62.529	3048 cells

Cell: CLKSPC

Function: Clock Splitter

Description:

The clock splitter generates two nonoverlapping clock signals from a single oscillator input signal. The clock splitter allows independent control of clocks, and is fully testable.

EN Disables the oscillator

PG1 Enable ZC

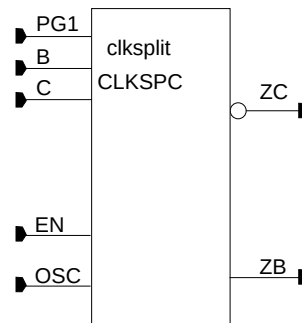
OSC Oscillator input

B LSSD B clock

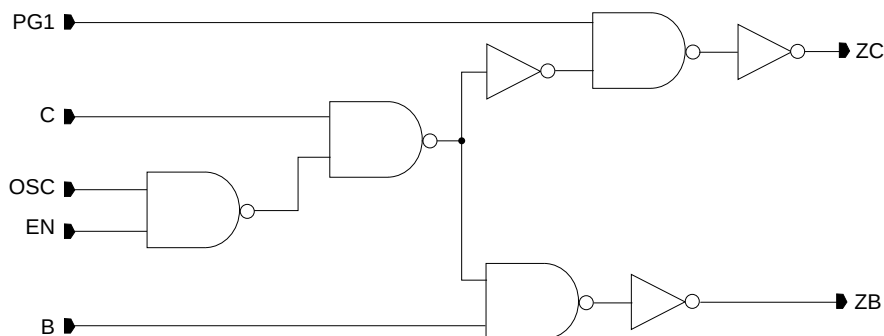
C LSSD C clock

ZB Generated B clock (L2)

ZC Generated C clock (L1)



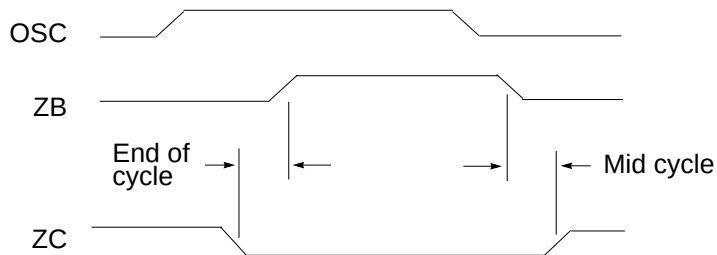
Logical Representation of Clock Splitter



Truth Table

Mode	Inputs					Outputs	
	OSC	EN	PG1	B	C	ZB	ZC
Functional	0	1	1	1	1	0	1
	1	1	1	1	1	1	0
OSC stopped	X	X	X	X	0	B	0
	X	0	X	X	1	0	PG1
Other	0	X	X	X	1	0	PG1
	1	1	X	X	X	B	0
ZC stopped	0	1	0	1	1	0	0
	1	1	0	1	1	1	0
ZB stopped	0	1	1	0	1	0	1
	1	1	1	0	1	0	0

Output Waveform



Waveform Calculation

Waveform ¹	Performance Level	Edge Separation in ns		
		V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
END OF CYCLE	D	0.118 + 0.000N _{std}	0.070 + 0.000N _{std}	0.049 + 0.000N _{std}
MID CYCLE		0.268 + 0.000N _{std}	0.160 + 0.000N _{std}	0.105 + 0.000N _{std}
END OF CYCLE	H	-0.013 + 0.000N _{std}	-0.012 + 0.000N _{std}	-0.006 + 0.000N _{std}
MID CYCLE		0.267 + 0.000N _{std}	0.162 + 0.000N _{std}	0.108 + 0.000N _{std}
END OF CYCLE	K	-0.111 + 0.000N _{std}	-0.066 + 0.000N _{std}	-0.041 + 0.000N _{std}
MID CYCLE		0.264 + 0.000N _{std}	0.157 + 0.000N _{std}	0.104 + 0.000N _{std}

¹. See *Output Waveform* diagram.

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
OSC-ZB	D	t _{PLH}	0.377 + 0.003N _{std}	0.234 + 0.002N _{std}	0.163 + 0.001N _{std}
		t _{PHL}	0.349 + 0.003N _{std}	0.231 + 0.002N _{std}	0.162 + 0.001N _{std}
OSC-ZC		t _{PLH}	0.617 + 0.003N _{std}	0.391 + 0.002N _{std}	0.267 + 0.001N _{std}
		t _{PHL}	0.259 + 0.003N _{std}	0.164 + 0.002N _{std}	0.114 + 0.001N _{std}
OSC-ZB	H	t _{PLH}	0.365 + 0.003N _{std}	0.225 + 0.002N _{std}	0.156 + 0.001N _{std}
		t _{PHL}	0.362 + 0.003N _{std}	0.236 + 0.002N _{std}	0.165 + 0.001N _{std}
OSC-ZC		t _{PLH}	0.629 + 0.003N _{std}	0.398 + 0.002N _{std}	0.273 + 0.001N _{std}
		t _{PHL}	0.378 + 0.003N _{std}	0.237 + 0.002N _{std}	0.162 + 0.001N _{std}
OSC-ZB	K	t _{PLH}	0.365 + 0.003N _{std}	0.225 + 0.002N _{std}	0.155 + 0.001N _{std}
		t _{PHL}	0.358 + 0.003N _{std}	0.235 + 0.002N _{std}	0.164 + 0.001N _{std}
OSC-ZC		t _{PLH}	0.622 + 0.003N _{std}	0.392 + 0.002N _{std}	0.268 + 0.001N _{std}
		t _{PHL}	0.476 + 0.003N _{std}	0.291 + 0.002N _{std}	0.196 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	D	H	K
B	0.841	0.842	0.841
C	0.642	0.636	0.637
EN	0.686	0.632	0.599
OSC	1.097	0.936	0.843
PG1	0.809	0.810	0.810
Internal	12.511	12.467	12.225
Cell Units	27 cells	27 cells	27 cells

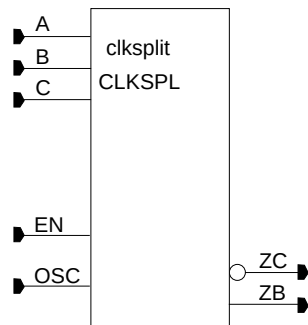
Cell: CLKSPL

Function: Clock Splitter

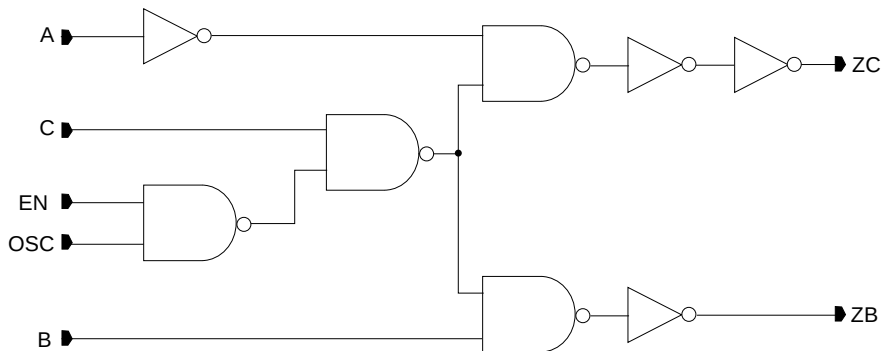
Description:

The clock splitter generates two nonoverlapping clock signals from a single oscillator input signal. The clock splitter allows independent control of clocks, and is fully testable. The A input is tied to "0" when the splitter is used with latches that have a LSSD A clock pin. However, when the splitter is used with MPH latches, the A input is connected to the LSSD A clock.

EN	Disables the oscillator
A	MPH A clock
OSC	Oscillator input
B	LSSD B clock
C	LSSD C clock
ZB	Generated B clock (L2)
ZC	Generated C clock (L1)



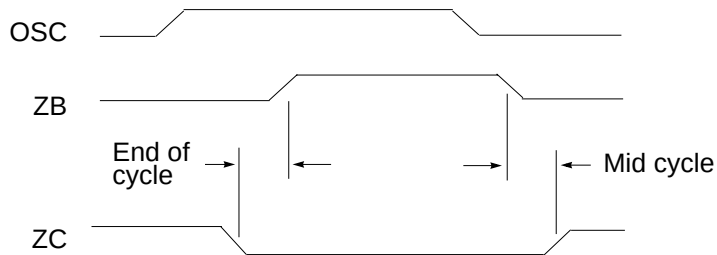
Logical Representation of Clock Splitter



Truth Table

Mode	Inputs					Outputs	
	OSC	EN	A	B	C	ZB	ZC
Functional	0	1	0	1	1	0	1
	1	1	0	1	1	1	0
OSC stopped	X	X	X	X	0	B	A
	X	0	X	X	1	0	1
Test	X	X	0	0	0	0	0
	1	1	0	0	X	0	0
	X	X	1	0	X	0	1
	0	X	X	X	1	0	1
	X	0	X	X	1	0	1
	X	X	X	1	0	1	A
	1	1	1	X	X	B	1

Output Waveform



Waveform Calculation

Waveform ¹	Performance Level	Edge Separation in ns		
		V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
END OF CYCLE	D	0.075 + 0.000N _{std}	0.044 + 0.000N _{std}	0.031 + 0.000N _{std}
MID CYCLE		0.261 + 0.000N _{std}	0.159 + 0.000N _{std}	0.105 + 0.000N _{std}
END OF CYCLE	H	-0.013 + 0.000N _{std}	-0.011 + 0.000N _{std}	-0.006 + 0.000N _{std}
MID CYCLE		0.268 + 0.000N _{std}	0.166 + 0.000N _{std}	0.113 + 0.000N _{std}
END OF CYCLE	K	-0.123 + 0.000N _{std}	-0.071 + 0.000N _{std}	-0.043 + 0.000N _{std}
MID CYCLE		0.262 + 0.000N _{std}	0.162 + 0.000N _{std}	0.109 + 0.000N _{std}

¹. See *Output Waveform* diagram.

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
OSC-ZB	D	t _{PLH}	0.374 + 0.003N _{std}	0.233 + 0.002N _{std}	0.162 + 0.001N _{std}
		t _{PHL}	0.350 + 0.003N _{std}	0.230 + 0.002N _{std}	0.162 + 0.001N _{std}
OSC-ZC		t _{PLH}	0.611 + 0.003N _{std}	0.389 + 0.002N _{std}	0.267 + 0.001N _{std}
		t _{PHL}	0.299 + 0.003N _{std}	0.189 + 0.002N _{std}	0.131 + 0.001N _{std}
OSC-ZB	H	t _{PLH}	0.367 + 0.003N _{std}	0.226 + 0.002N _{std}	0.156 + 0.001N _{std}
		t _{PHL}	0.363 + 0.003N _{std}	0.237 + 0.002N _{std}	0.165 + 0.001N _{std}
OSC-ZC		t _{PLH}	0.631 + 0.003N _{std}	0.403 + 0.002N _{std}	0.278 + 0.001N _{std}
		t _{PHL}	0.380 + 0.003N _{std}	0.237 + 0.002N _{std}	0.162 + 0.001N _{std}
OSC-ZB	K	t _{PLH}	0.368 + 0.003N _{std}	0.227 + 0.002N _{std}	0.157 + 0.001N _{std}
		t _{PHL}	0.360 + 0.003N _{std}	0.235 + 0.002N _{std}	0.165 + 0.001N _{std}
OSC-ZC		t _{PLH}	0.622 + 0.003N _{std}	0.397 + 0.002N _{std}	0.274 + 0.001N _{std}
		t _{PHL}	0.491 + 0.003N _{std}	0.298 + 0.002N _{std}	0.200 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

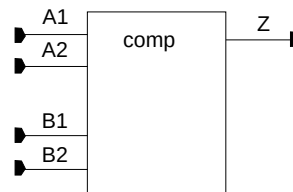
Input Pins	Performance Level		
	D	H	K
A	1.191	1.295	1.296
B	0.841	0.841	0.841
C	0.647	0.642	0.643
EN	0.693	0.635	0.597
OSC	1.116	0.939	0.834
Internal	12.843	12.890	12.537
Cell Units	28 cells	28 cells	28 cells

Cell: COMP2

Function: 2-Bit Comparator

Description:

The output of the 2-bit comparator is a "1" when the A1/B1 pairs are the same AND the A2/B2 pairs are the same. The A1/B1 pair does not need to have the same value as the A2/B2 pair.



Truth Table

Inputs				Output
A1	B1	A2	B2	Z
0	1	X	X	0
1	0	X	X	0
X	X	0	1	0
X	X	1	0	0
0	0	0	0	1
0	0	1	1	1
1	1	0	0	1
1	1	1	1	1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	B	t _{PLH}	0.227 + 0.065N _{std}	0.152 + 0.041N _{std}	0.110 + 0.028N _{std}
		t _{PHL}	0.242 + 0.036N _{std}	0.152 + 0.023N _{std}	0.099 + 0.017N _{std}
B1-Z		t _{PLH}	0.224 + 0.064N _{std}	0.150 + 0.041N _{std}	0.109 + 0.028N _{std}
		t _{PHL}	0.279 + 0.037N _{std}	0.189 + 0.023N _{std}	0.136 + 0.017N _{std}
A1-Z	C	t _{PLH}	0.215 + 0.032N _{std}	0.145 + 0.021N _{std}	0.106 + 0.015N _{std}
		t _{PHL}	0.244 + 0.021N _{std}	0.153 + 0.013N _{std}	0.099 + 0.010N _{std}
B1-Z		t _{PLH}	0.212 + 0.032N _{std}	0.143 + 0.021N _{std}	0.105 + 0.015N _{std}
		t _{PHL}	0.281 + 0.021N _{std}	0.192 + 0.013N _{std}	0.140 + 0.010N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A1-Z	D	t _{PLH}	0.209 + 0.021N _{std}	0.142 + 0.014N _{std}	0.104 + 0.010N _{std}
		t _{PHL}	0.242 + 0.014N _{std}	0.152 + 0.009N _{std}	0.099 + 0.007N _{std}
B1-Z		t _{PLH}	0.205 + 0.021N _{std}	0.139 + 0.014N _{std}	0.103 + 0.010N _{std}
		t _{PHL}	0.281 + 0.014N _{std}	0.193 + 0.009N _{std}	0.142 + 0.007N _{std}
A1-Z	E	t _{PLH}	0.204 + 0.016N _{std}	0.140 + 0.010N _{std}	0.104 + 0.007N _{std}
		t _{PHL}	0.238 + 0.010N _{std}	0.150 + 0.007N _{std}	0.098 + 0.005N _{std}
B1-Z		t _{PLH}	0.201 + 0.016N _{std}	0.137 + 0.010N _{std}	0.102 + 0.008N _{std}
		t _{PHL}	0.277 + 0.010N _{std}	0.192 + 0.007N _{std}	0.142 + 0.005N _{std}
A1-Z	F	t _{PLH}	0.218 + 0.011N _{std}	0.151 + 0.007N _{std}	0.111 + 0.005N _{std}
		t _{PHL}	0.267 + 0.006N _{std}	0.168 + 0.004N _{std}	0.110 + 0.003N _{std}
B1-Z		t _{PLH}	0.215 + 0.011N _{std}	0.148 + 0.007N _{std}	0.109 + 0.005N _{std}
		t _{PHL}	0.306 + 0.006N _{std}	0.211 + 0.004N _{std}	0.154 + 0.003N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level				
	B	C	D	E	F
A1	0.369	0.454	0.549	0.658	0.665
A2	0.369	0.453	0.549	0.657	0.665
B1	0.545	0.666	0.806	0.963	0.961
B2	0.541	0.661	0.801	0.959	0.959
Internal	2.494	3.447	4.540	5.676	7.010
Cell Units	18 cells	18 cells	18 cells	18 cells	20 cells

Cell: DECAP

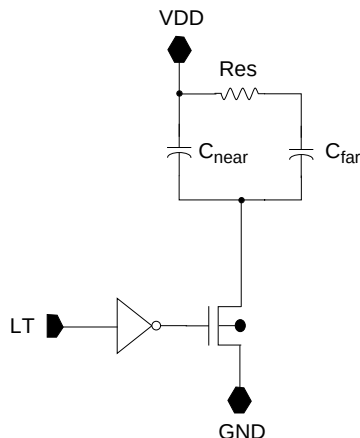
Function: V_{dd} - GND Decoupling Capacitor

Description:

The DECAP cell is an MOS capacitor, which can be placed on a chip to provide local noise decoupling from V_{dd} to GND. It should be intermixed about the chip and placed near switching circuits. The LT pin is used at test to eliminate potential leakage current. The slew of the LT pin is non-critical. The DECAP cell is modeled as a pi network (see diagram and table below), where C_{near} is defined as the capacitance closest to the switching event.

Be aware that these cells have high polysilicon density, which could cause checking concerns at the chip level. Blocks of DECAP cells should not exceed 3 mm^2 as this could effect the lithography of neighboring devices.

LT Leakage test input pin



Truth Table

Input	Mode
LT	
0	Decoupling - normal mode
1	Leakage test - decoupling off

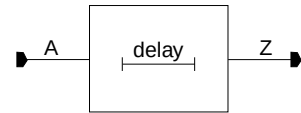
Capacitance, Resistance and Cell Sizes

Input Pins	Performance Level			
	A	B	C	D
LT (pF)	0.0043	0.0043	0.0043	0.0084
C_{near} (pF)	0.01079	0.01429	0.01997	0.03582
Resistance (ohms)	320.6	158.1	170.5	85.2
C_{far} (pF)	0.1741	0.2395	0.4108	1.264
Cell Units	24 cells	35 cells	48 cells	2 x 48 cells

Cell: DELAY4

Function: Delay Line

Boolean Expression: $Z = A$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-Z	C	t_{PLH}	$0.372 + 0.006N_{std}$	$0.242 + 0.004N_{std}$	$0.174 + 0.003N_{std}$
		t_{PHL}	$0.349 + 0.007N_{std}$	$0.228 + 0.005N_{std}$	$0.163 + 0.003N_{std}$
	F	t_{PLH}	$0.306 + 0.006N_{std}$	$0.198 + 0.004N_{std}$	$0.140 + 0.003N_{std}$
		t_{PHL}	$0.285 + 0.007N_{std}$	$0.189 + 0.005N_{std}$	$0.135 + 0.004N_{std}$
	J	t_{PLH}	$0.257 + 0.006N_{std}$	$0.165 + 0.004N_{std}$	$0.117 + 0.003N_{std}$
		t_{PHL}	$0.252 + 0.007N_{std}$	$0.171 + 0.005N_{std}$	$0.123 + 0.004N_{std}$

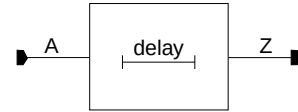
Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	C	F	J
A	0.615	0.614	0.613
Internal	6.383	5.989	6.400
Cell Units	10 cells	10 cells	10 cells

Cell: DELAY6

Function: Delay Line

Boolean Expression: $Z = A$



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-Z	A	t_{PLH}	$2.487 + 0.006N_{std}$	$1.512 + 0.004N_{std}$	$1.085 + 0.003N_{std}$
		t_{PHL}	$2.486 + 0.004N_{std}$	$1.531 + 0.003N_{std}$	$1.087 + 0.002N_{std}$
	B	t_{PLH}	$1.550 + 0.007N_{std}$	$0.968 + 0.004N_{std}$	$0.699 + 0.003N_{std}$
		t_{PHL}	$1.567 + 0.007N_{std}$	$0.968 + 0.005N_{std}$	$0.692 + 0.003N_{std}$
	C	t_{PLH}	$0.746 + 0.006N_{std}$	$0.480 + 0.004N_{std}$	$0.346 + 0.003N_{std}$
		t_{PHL}	$0.720 + 0.007N_{std}$	$0.461 + 0.005N_{std}$	$0.332 + 0.003N_{std}$
	F	t_{PLH}	$0.611 + 0.006N_{std}$	$0.393 + 0.004N_{std}$	$0.281 + 0.003N_{std}$
		t_{PHL}	$0.588 + 0.007N_{std}$	$0.378 + 0.005N_{std}$	$0.269 + 0.003N_{std}$
	J	t_{PLH}	$0.516 + 0.006N_{std}$	$0.327 + 0.004N_{std}$	$0.231 + 0.003N_{std}$
		t_{PHL}	$0.501 + 0.007N_{std}$	$0.325 + 0.005N_{std}$	$0.231 + 0.004N_{std}$
	M	t_{PLH}	$0.347 + 0.006N_{std}$	$0.220 + 0.004N_{std}$	$0.152 + 0.003N_{std}$
		t_{PHL}	$0.339 + 0.007N_{std}$	$0.223 + 0.005N_{std}$	$0.157 + 0.004N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level					
	A	B	C	F	J	M
A	0.508	0.599	0.615	0.614	0.613	0.611
Internal	17.561	14.963	9.086	8.498	8.057	7.406
Cell Units	15 cells	15 cells	15 cells	15 cells	15 cells	15 cells

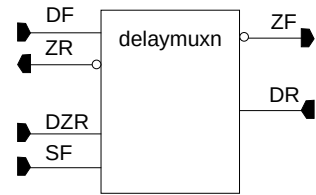
Cell: DELAYMUXN

Function: Programmable Delay Element

Description:

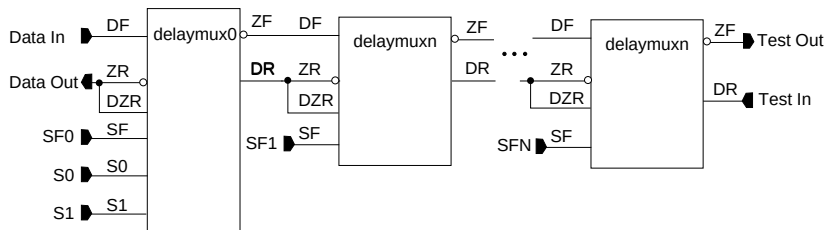
Provides one unit of a programmable delay line. When SF is a logic 1, then $ZF = \overline{DF}$ and $ZR = \overline{DR}$. When SF is a logic 0, then $ZR = \overline{DF}$ and $ZF = \overline{DZR}$.

- DF Data input (forward path)
- DR Data input (return path)
- DZR Data input (must be connected to ZR of same circuit for an accurate delay and dual mode operation)
- ZF Data output (forward path)
- ZR Data output (return path)
- SF Logic 1 selects forward path



This circuit is pin-typed so that ZR must connect to one and only one DR pin of another DELAYMUXN or DELAYMUX0 circuit and must connect to its own DZR pin. ZR can also connect to the input of another circuit; however, for balanced delays, any additional circuit load on ZR (other than the required DR and DZR connections) should be duplicated as a load on ZF.

A programmable delay line is configured by attaching multiple DELAYMUXN elements to only one DELAYMUX0 element as follows:



If all select bits SF0, SF1, SF2, ..., SFN are set to a logic 0, the minimum delay (data in to data out) is achieved. As each select bit SF0, SF1, SF2 is switched to a logic 1, the delay from data in to data out is increased by the sum of the delays from DR to ZR and DF to ZF. Connecting the DZR pin of the DELAYMUX0 to the ZR pin of the DELAYMUX0 allows data to pass down the chain from data in toward test out while passing through all the delay stages if all the SF inputs are set to logic "0".

This fast setup mode allows the ZR and ZF nodes to be sensed with latches at each stage to capture how far down the delay chain a switching edge has progressed relative to a capture clock fed to the latches. This latched data can be used directly by the delay muxes to program the correct delay in the path. The DELAYMUX0 S0 and S1 inputs can then be adjusted to further refine the delay.



Truth Table

Inputs				Outputs	
SF	DF	DR	DZR	ZF	ZR
0	X	X	X	$\overline{\text{DZR}}$	$\overline{\text{DF}}$
1	X	X	X	$\overline{\text{DF}}$	$\overline{\text{DR}}$

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
DF-ZF	H	t _{PLH}	0.093 + 0.006N _{std}	0.071 + 0.004N _{std}	0.057 + 0.003N _{std}
		t _{PHL}	0.103 + 0.005N _{std}	0.071 + 0.003N _{std}	0.051 + 0.003N _{std}
SF-ZF		t _{PLH}	0.190 + 0.005N _{std}	0.135 + 0.004N _{std}	0.101 + 0.003N _{std}
		t _{PHL}	0.162 + 0.005N _{std}	0.109 + 0.003N _{std}	0.078 + 0.003N _{std}
DR-ZR		t _{PLH}	0.093 + 0.005N _{std}	0.071 + 0.004N _{std}	0.057 + 0.003N _{std}
		t _{PHL}	0.109 + 0.006N _{std}	0.075 + 0.004N _{std}	0.054 + 0.003N _{std}
SF-ZR		t _{PLH}	0.197 + 0.005N _{std}	0.140 + 0.004N _{std}	0.104 + 0.003N _{std}
		t _{PHL}	0.178 + 0.006N _{std}	0.120 + 0.004N _{std}	0.086 + 0.003N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	H
DF	4.000
DR	3.195
DZR	3.032
Internal	15.817
SF	2.063
Cell Units	17 cells

Cell: DELAYMUX0

Function: Programmable Fine Delay Element

Description:

Provides delay increments of 1/4 of a DELAYMUXN unit delay. When SF is a logic 1, then $ZF = DF$ and $ZR = DR$. When SF is a logic 0, then $ZR = \overline{DF}$ and $ZF = \overline{DZR}$.

DF Data input (forward path)

DR Data input (return path)

DZR Data input (used for fast setup mode)

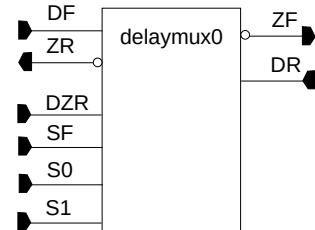
ZF Data output (forward path)

ZR Data output (return path)

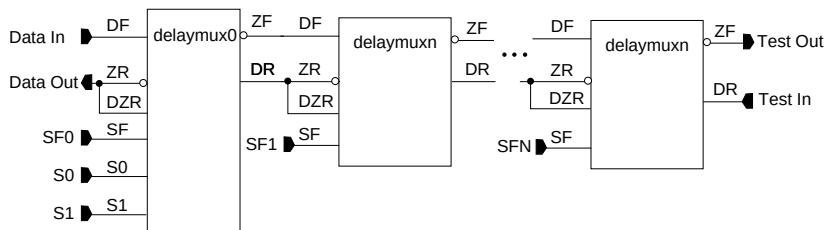
SF Logic 1 selects forward path

S0 Least significant bit of fine delay adjust (1 = add 1/4 delay)

S1 Most significant bit of fine delay adjust (1 = add 1/2 delay)



A programmable delay line is configured by attaching multiple DELAYMUXN elements to only one DELAYMUX0 element as follows:



If all select bits SF0, SF1, SF2, ..., SFn are set to a logic 0, the minimum delay (data in to data out) is achieved. As each select bit SF0, SF1, SF2 is switched to a logic 1, the delay from data in to data out is increased by the sum of the delays from DR to ZR and DF to ZF. Connecting the DZR pin of the DELAYMUX0 to the ZR pin of the DELAYMUX0 allows data to pass down the chain from data in toward test out while passing through all the delay stages if all the SF inputs are set to logic "0".

This fast setup mode allows the ZR and ZF nodes to be sensed with latches at each stage to capture how far down the delay chain a switching edge has progressed relative to a capture clock fed to the latches. This latched data can be used directly by the delay muxes to program the correct delay in the path. The DELAYMUX0 S0 and S1 inputs can then be adjusted to further refine the delay.



Truth Table

Inputs						Outputs	
SF	S0	S1	DF	DR	DZR	ZF	ZR
0	X	X	X	X	X	$\overline{\text{DZR}}$	$\overline{\text{DF}}$
1	X	X	X	X	X	$\overline{\text{DF}}$	$\overline{\text{DR}}$

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
DF-ZF	H	t _{PLH}	0.128 + 0.006N _{std}	0.092 + 0.004N _{std}	0.070 + 0.003N _{std}
		t _{PHL}	0.123 + 0.005N _{std}	0.085 + 0.003N _{std}	0.061 + 0.003N _{std}
SF-ZF		t _{PLH}	0.292 + 0.006N _{std}	0.183 + 0.004N _{std}	0.125 + 0.003N _{std}
		t _{PHL}	0.291 + 0.005N _{std}	0.182 + 0.003N _{std}	0.124 + 0.003N _{std}
DR-ZR		t _{PLH}	0.121 + 0.006N _{std}	0.089 + 0.004N _{std}	0.069 + 0.003N _{std}
		t _{PHL}	0.136 + 0.006N _{std}	0.092 + 0.004N _{std}	0.066 + 0.003N _{std}
SF-ZR		t _{PLH}	0.319 + 0.006N _{std}	0.207 + 0.004N _{std}	0.145 + 0.003N _{std}
		t _{PHL}	0.338 + 0.006N _{std}	0.218 + 0.004N _{std}	0.152 + 0.003N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

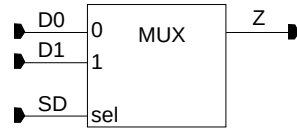
Input Pins	Performance Level
	H
DF	7.492
DR	3.758
DZR	3.732
Internal	26.185
S0	3.592
S1	2.094
SF	4.215
Cell Units	75 cells

Cell: MUX21

Function: 2:1 Multiplexer

Description:

Selects data from D0 or D1 based on the value of the SD input pin



Truth Table

Inputs			Output
SD	D0	D1	Z
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D0-Z	C	t _{PLH}	0.117 + 0.034N _{std}	0.070 + 0.023N _{std}	0.044 + 0.016N _{std}
		t _{PHL}	0.184 + 0.029N _{std}	0.127 + 0.018N _{std}	0.094 + 0.013N _{std}
SD-Z		t _{PLH}	0.205 + 0.034N _{std}	0.140 + 0.023N _{std}	0.102 + 0.016N _{std}
		t _{PHL}	0.228 + 0.029N _{std}	0.144 + 0.018N _{std}	0.096 + 0.013N _{std}
D0-Z	D	t _{PLH}	0.119 + 0.023N _{std}	0.072 + 0.016N _{std}	0.046 + 0.012N _{std}
		t _{PHL}	0.188 + 0.019N _{std}	0.130 + 0.012N _{std}	0.096 + 0.009N _{std}
SD-Z		t _{PLH}	0.207 + 0.023N _{std}	0.141 + 0.016N _{std}	0.103 + 0.012N _{std}
		t _{PHL}	0.232 + 0.018N _{std}	0.147 + 0.012N _{std}	0.098 + 0.009N _{std}
D0-Z	E	t _{PLH}	0.124 + 0.017N _{std}	0.075 + 0.012N _{std}	0.049 + 0.009N _{std}
		t _{PHL}	0.192 + 0.014N _{std}	0.133 + 0.009N _{std}	0.098 + 0.007N _{std}
SD-Z		t _{PLH}	0.213 + 0.017N _{std}	0.146 + 0.012N _{std}	0.106 + 0.009N _{std}
		t _{PHL}	0.237 + 0.014N _{std}	0.150 + 0.009N _{std}	0.100 + 0.007N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D0-Z	F	t _{PLH}	0.137 + 0.011N _{std}	0.085 + 0.007N _{std}	0.056 + 0.005N _{std}
		t _{PHL}	0.201 + 0.009N _{std}	0.139 + 0.006N _{std}	0.102 + 0.004N _{std}
SD-Z		t _{PLH}	0.230 + 0.011N _{std}	0.156 + 0.007N _{std}	0.114 + 0.005N _{std}
		t _{PHL}	0.247 + 0.009N _{std}	0.157 + 0.006N _{std}	0.105 + 0.004N _{std}
D0-Z	H	t _{PLH}	0.139 + 0.008N _{std}	0.086 + 0.006N _{std}	0.057 + 0.004N _{std}
		t _{PHL}	0.207 + 0.005N _{std}	0.143 + 0.003N _{std}	0.105 + 0.002N _{std}
SD-Z		t _{PLH}	0.222 + 0.009N _{std}	0.152 + 0.006N _{std}	0.111 + 0.004N _{std}
		t _{PHL}	0.265 + 0.005N _{std}	0.170 + 0.003N _{std}	0.115 + 0.002N _{std}
D0-Z	I	t _{PLH}	0.154 + 0.006N _{std}	0.097 + 0.004N _{std}	0.066 + 0.003N _{std}
		t _{PHL}	0.207 + 0.004N _{std}	0.144 + 0.003N _{std}	0.105 + 0.002N _{std}
SD-Z		t _{PLH}	0.224 + 0.006N _{std}	0.153 + 0.004N _{std}	0.112 + 0.003N _{std}
		t _{PHL}	0.253 + 0.004N _{std}	0.164 + 0.003N _{std}	0.112 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

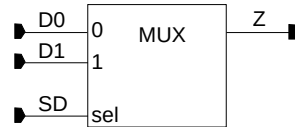
Input Pins	Performance Level					
	C	D	E	F	H	I
D0	0.733	0.732	0.745	0.789	0.933	1.047
D1	0.792	0.791	0.804	0.846	0.970	1.081
SD	1.107	1.104	1.113	1.140	1.290	1.469
Internal	3.044	3.271	3.591	4.304	5.554	6.774
Cell Units	9 cells	9 cells	9 cells	9 cells	9 cells	9 cells

Cell: MUX21BAL

Function: Balanced 2:1 Multiplexer

Description:

Selects data from D0 or D1 based on the value of the SD input pin. Delay of D0 to Z equals delay of D1 to Z. Rising data delay equals falling data delay. Rising select delay equals falling select delay.



Truth Table

Inputs			Output
SD	D0	D1	Z
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D0-Z	H	t _{PLH}	0.178 + 0.005N _{std}	0.118 + 0.004N _{std}	0.086 + 0.003N _{std}
		t _{PHL}	0.197 + 0.004N _{std}	0.138 + 0.003N _{std}	0.100 + 0.002N _{std}
D1-Z		t _{PLH}	0.178 + 0.005N _{std}	0.118 + 0.004N _{std}	0.085 + 0.003N _{std}
		t _{PHL}	0.200 + 0.004N _{std}	0.139 + 0.003N _{std}	0.101 + 0.002N _{std}
SD-Z		t _{PLH}	0.264 + 0.005N _{std}	0.180 + 0.004N _{std}	0.131 + 0.003N _{std}
		t _{PHL}	0.288 + 0.004N _{std}	0.185 + 0.003N _{std}	0.127 + 0.002N _{std}
D0-Z	J	t _{PLH}	0.221 + 0.003N _{std}	0.146 + 0.002N _{std}	0.105 + 0.001N _{std}
		t _{PHL}	0.247 + 0.002N _{std}	0.170 + 0.001N _{std}	0.122 + 0.001N _{std}
D1-Z		t _{PLH}	0.222 + 0.003N _{std}	0.147 + 0.002N _{std}	0.106 + 0.001N _{std}
		t _{PHL}	0.250 + 0.002N _{std}	0.172 + 0.001N _{std}	0.123 + 0.001N _{std}
SD-Z		t _{PLH}	0.316 + 0.003N _{std}	0.200 + 0.002N _{std}	0.138 + 0.001N _{std}
		t _{PHL}	0.342 + 0.002N _{std}	0.218 + 0.001N _{std}	0.149 + 0.001N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D0-Z	L	t _{PLH}	0.262 + 0.002N _{std}	0.172 + 0.001N _{std}	0.124 + 0.001N _{std}
		t _{PHL}	0.291 + 0.001N _{std}	0.199 + 0.001N _{std}	0.142 + 0.001N _{std}
D1-Z		t _{PLH}	0.264 + 0.002N _{std}	0.173 + 0.001N _{std}	0.124 + 0.001N _{std}
		t _{PHL}	0.294 + 0.001N _{std}	0.201 + 0.001N _{std}	0.143 + 0.001N _{std}
SD-Z		t _{PLH}	0.359 + 0.002N _{std}	0.226 + 0.001N _{std}	0.156 + 0.001N _{std}
		t _{PHL}	0.384 + 0.001N _{std}	0.244 + 0.001N _{std}	0.166 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

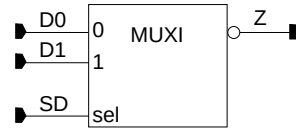
Input Pins	Performance Level		
	H	J	L
D0	0.881	0.915	0.934
D1	0.959	0.990	1.006
SD	1.711	1.696	1.696
Internal	9.283	13.112	17.934
Cell Units	16 cells	19 cells	22 cells

Cell: MUX21I

Function: 2:1 Multiplexer with Inverted Output

Description:

Selects data from D0 or D1 based on the value of the SD input pin.



Truth Table

Inputs			Output
SD	D0	D1	Z
0	0	X	1
0	1	X	0
1	X	0	1
1	X	1	0

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D0-Z	B	t _{PLH}	0.115 + 0.039N _{std}	0.084 + 0.026N _{std}	0.065 + 0.018N _{std}
		t _{PHL}	0.071 + 0.020N _{std}	0.042 + 0.013N _{std}	0.025 + 0.010N _{std}
SD-Z		t _{PLH}	0.129 + 0.038N _{std}	0.081 + 0.026N _{std}	0.051 + 0.018N _{std}
		t _{PHL}	0.160 + 0.018N _{std}	0.114 + 0.011N _{std}	0.087 + 0.008N _{std}
D0-Z	C	t _{PLH}	0.103 + 0.029N _{std}	0.076 + 0.020N _{std}	0.058 + 0.014N _{std}
		t _{PHL}	0.082 + 0.019N _{std}	0.050 + 0.012N _{std}	0.033 + 0.009N _{std}
SD-Z		t _{PLH}	0.110 + 0.029N _{std}	0.069 + 0.019N _{std}	0.043 + 0.014N _{std}
		t _{PHL}	0.156 + 0.018N _{std}	0.112 + 0.011N _{std}	0.086 + 0.008N _{std}
D0-Z	D	t _{PLH}	0.099 + 0.021N _{std}	0.073 + 0.014N _{std}	0.056 + 0.010N _{std}
		t _{PHL}	0.085 + 0.015N _{std}	0.053 + 0.010N _{std}	0.036 + 0.007N _{std}
SD-Z		t _{PLH}	0.118 + 0.021N _{std}	0.076 + 0.014N _{std}	0.050 + 0.010N _{std}
		t _{PHL}	0.150 + 0.014N _{std}	0.107 + 0.009N _{std}	0.081 + 0.006N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D0-Z	E	t _{PLH}	0.114 + 0.011N _{std}	0.081 + 0.008N _{std}	0.061 + 0.006N _{std}
		t _{PHL}	0.099 + 0.008N _{std}	0.061 + 0.005N _{std}	0.041 + 0.004N _{std}
SD-Z		t _{PLH}	0.160 + 0.011N _{std}	0.103 + 0.007N _{std}	0.069 + 0.005N _{std}
		t _{PHL}	0.202 + 0.008N _{std}	0.141 + 0.005N _{std}	0.105 + 0.003N _{std}
D0-Z	F	t _{PLH}	0.213 + 0.011N _{std}	0.144 + 0.008N _{std}	0.103 + 0.006N _{std}
		t _{PHL}	0.194 + 0.009N _{std}	0.120 + 0.006N _{std}	0.080 + 0.005N _{std}
SD-Z		t _{PLH}	0.219 + 0.011N _{std}	0.136 + 0.008N _{std}	0.087 + 0.006N _{std}
		t _{PHL}	0.270 + 0.009N _{std}	0.183 + 0.006N _{std}	0.134 + 0.005N _{std}
D0-Z	H	t _{PLH}	0.209 + 0.008N _{std}	0.140 + 0.006N _{std}	0.102 + 0.004N _{std}
		t _{PHL}	0.205 + 0.004N _{std}	0.128 + 0.003N _{std}	0.086 + 0.002N _{std}
SD-Z		t _{PLH}	0.214 + 0.008N _{std}	0.133 + 0.006N _{std}	0.086 + 0.004N _{std}
		t _{PHL}	0.279 + 0.004N _{std}	0.189 + 0.003N _{std}	0.138 + 0.002N _{std}
D0-Z	I	t _{PLH}	0.214 + 0.005N _{std}	0.144 + 0.004N _{std}	0.104 + 0.003N _{std}
		t _{PHL}	0.221 + 0.004N _{std}	0.138 + 0.003N _{std}	0.093 + 0.002N _{std}
SD-Z		t _{PLH}	0.217 + 0.005N _{std}	0.135 + 0.004N _{std}	0.087 + 0.003N _{std}
		t _{PHL}	0.294 + 0.004N _{std}	0.199 + 0.003N _{std}	0.145 + 0.002N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

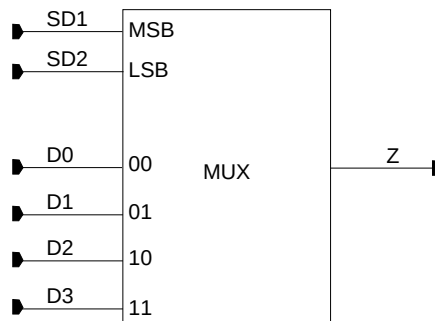
Performance Level	Input Pins				
	D0	D1	SD	Internal	Cell Units
B	0.710	0.771	1.169	2.265	7 cells
C	0.809	0.870	1.353	2.706	7 cells
D	1.014	1.076	1.608	3.451	7 cells
E	1.957	1.901	2.384	6.484	15 cells
F	0.828	0.876	1.357	5.201	12 cells
H	0.831	0.876	1.354	6.259	12 cells
I	0.832	0.876	1.353	7.140	12 cells

Cell: MUX41

Function: 4:1 Multiplexer

Description:

Selects data from D0, D1, D2, or D3 based on the values of the SD1 and SD2 input pins.



Truth Table

Inputs		Output
SD1	SD2	Z
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D0-Z	D	t _{PLH}	0.187 + 0.023N _{std}	0.113 + 0.016N _{std}	0.073 + 0.011N _{std}
		t _{PHL}	0.249 + 0.017N _{std}	0.162 + 0.011N _{std}	0.113 + 0.008N _{std}
SD2-Z		t _{PLH}	0.276 + 0.023N _{std}	0.183 + 0.016N _{std}	0.131 + 0.011N _{std}
		t _{PHL}	0.284 + 0.017N _{std}	0.189 + 0.011N _{std}	0.138 + 0.008N _{std}
D0-Z	F	t _{PLH}	0.206 + 0.010N _{std}	0.127 + 0.007N _{std}	0.085 + 0.005N _{std}
		t _{PHL}	0.267 + 0.006N _{std}	0.175 + 0.004N _{std}	0.121 + 0.003N _{std}
SD2-Z		t _{PLH}	0.298 + 0.010N _{std}	0.199 + 0.007N _{std}	0.140 + 0.005N _{std}
		t _{PHL}	0.305 + 0.006N _{std}	0.204 + 0.004N _{std}	0.146 + 0.003N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D0-Z	J	t _{PLH}	0.269 + 0.004N _{std}	0.170 + 0.003N _{std}	0.117 + 0.002N _{std}
		t _{PHL}	0.338 + 0.003N _{std}	0.227 + 0.002N _{std}	0.159 + 0.001N _{std}
SD2-Z		t _{PLH}	0.323 + 0.004N _{std}	0.216 + 0.003N _{std}	0.154 + 0.002N _{std}
		t _{PHL}	0.335 + 0.003N _{std}	0.224 + 0.002N _{std}	0.160 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

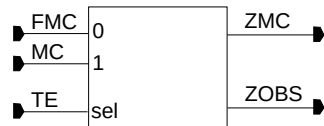
Input Pins	Performance Level		
	D	F	J
D0	0.851	0.879	0.876
D1	0.880	0.892	0.917
D2	0.853	0.882	0.880
D3	0.866	0.896	0.900
SD1	0.736	0.865	1.746
SD2	1.293	1.419	2.470
Internal	4.162	6.017	11.547
Cell Units	22 cells	22 cells	24 cells

Cell: MCMUX

Function: 2:1 Mode Control Mux

Description:

Selects data from functional mode control (FMC) or mode control (MC) based on the value of the test enable (TE) input pin. Data from FMC will always be observed on ZOBS.



Truth Table

Inputs			Outputs	
TE	MC	FMC	ZMC	ZOBS
0	X	X	FMC	FMC
1	X	X	MC	FMC

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{Std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
FMC-ZMC	M	t _{PLH}	0.272 + 0.002N _{Std}	0.174 + 0.001N _{Std}	0.120 + 0.001N _{Std}
		t _{PHL}	0.340 + 0.002N _{Std}	0.229 + 0.001N _{Std}	0.164 + 0.001N _{Std}
MC-ZMC		t _{PLH}	0.257 + 0.002N _{Std}	0.164 + 0.001N _{Std}	0.111 + 0.001N _{Std}
		t _{PHL}	0.324 + 0.002N _{Std}	0.218 + 0.001N _{Std}	0.157 + 0.001N _{Std}
FMC-ZOBS		t _{PLH}	0.112 + 0.016N _{Std}	0.076 + 0.011N _{Std}	0.054 + 0.008N _{Std}
		t _{PHL}	0.164 + 0.014N _{Std}	0.120 + 0.010N _{Std}	0.093 + 0.007N _{Std}

Capacitance (in units of N_{std}) and Cell Sizes

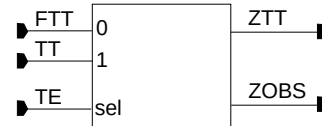
Input Pins	Performance Level
	M
FMC	0.949
MC	0.975
TE	1.490
Internal	140.342
Cell Units	20 cells

Cell: TTMUX

Function: 2:1 Termination Test Mux

Description:

Selects data from functional termination test (FTT) or termination test (TT) based on the value of the test enable (TE) input pin. Data from FTT will always be observed on ZOBS.



Truth Table

Inputs			Outputs	
TE	TT	FTT	ZTT	ZOBS
0	X	X	FTT	FTT
1	X	X	TT	FTT

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
FTT-ZOBS	M	t _{PLH}	0.112 + 0.016N _{std}	0.076 + 0.011N _{std}	0.054 + 0.008N _{std}
		t _{PHL}	0.164 + 0.014N _{std}	0.120 + 0.010N _{std}	0.093 + 0.007N _{std}
FTT-ZTT		t _{PLH}	0.272 + 0.002N _{std}	0.174 + 0.001N _{std}	0.120 + 0.001N _{std}
		t _{PHL}	0.340 + 0.002N _{std}	0.229 + 0.001N _{std}	0.164 + 0.001N _{std}
TT-ZTT		t _{PLH}	0.257 + 0.002N _{std}	0.164 + 0.001N _{std}	0.111 + 0.001N _{std}
		t _{PHL}	0.324 + 0.002N _{std}	0.218 + 0.001N _{std}	0.157 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	M
FTT	0.949
TE	1.490
TT	0.975
Internal	140.445
Cell Units	20 cells

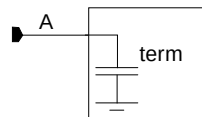
Cell: TERM

Function: Net Terminator

Description:

The net terminator is used to add additional capacitive load to a net. Additional load will vary the rise and fall time of the net.

Capacitive loads vary by performance level, as show in the table below.



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level			
	A	B	C	D
A	0.821	1.416	2.150	2.798
Internal	0.000	0.000	0.000	0.000
Cell Units	3 cells	3 cells	3 cells	3 cells

Standard Cell LSSD Latches



Cell: L2S0101_LPC

Function: L2* Latch, LSSD, +L1, +L2 Outputs, Low Power

Description:

This is a low-power L1/L2 LSSD latch that can accept data into L1 and L2 independently with two separate C clocks. However, in the scan mode, it is a normal L1/L2 LSSD latch (that is, A and B clocks are used to scan in and out the data). The L1 and L2 parts of this latch can be used separately in any logic path.

A A clock

B B clock

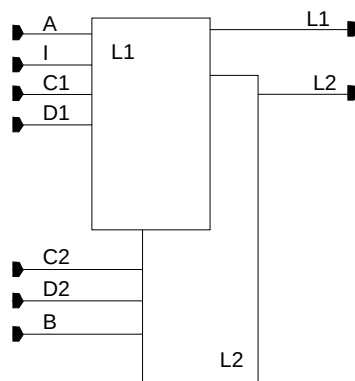
C1, C2 C clocks

D1, D2 Data

I Scan-in

L1 +L1 output (in phase with respect to data input)

L2 +L2 output (in phase with respect to data input)



LSSD Latch L1 Truth Table

Inputs				Output
A	I	C1	D1	L1
0	X	0	X	NC
1	X	0	X	I
0	X	1	X	D1

LSSD Latch L2 Truth Table

Inputs			Output
B	C2	D2	L2
0	0	X	NC
1	0	X	L1
0	1	X	D2

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D1-L1	E	t _{PLH}	0.186 + 0.014N _{std}	0.129 + 0.009N _{std}	0.099 + 0.007N _{std}
		t _{PHL}	0.378 + 0.007N _{std}	0.235 + 0.004N _{std}	0.157 + 0.003N _{std}
C2-L2		t _{PLH}	0.174 + 0.014N _{std}	0.112 + 0.009N _{std}	0.078 + 0.007N _{std}
		t _{PHL}	0.329 + 0.007N _{std}	0.198 + 0.004N _{std}	0.127 + 0.003N _{std}
D2-L2		t _{PLH}	0.182 + 0.014N _{std}	0.127 + 0.009N _{std}	0.097 + 0.007N _{std}
		t _{PHL}	0.358 + 0.007N _{std}	0.223 + 0.004N _{std}	0.149 + 0.003N _{std}

Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D1-L1	H	t _{PLH}	0.231 + 0.008N _{std}	0.155 + 0.005N _{std}	0.114 + 0.004N _{std}
		t _{PHL}	0.444 + 0.004N _{std}	0.271 + 0.003N _{std}	0.178 + 0.002N _{std}
C2-L2		t _{PLH}	0.207 + 0.008N _{std}	0.128 + 0.005N _{std}	0.088 + 0.004N _{std}
		t _{PHL}	0.386 + 0.004N _{std}	0.228 + 0.003N _{std}	0.143 + 0.002N _{std}
D2-L2		t _{PLH}	0.223 + 0.008N _{std}	0.150 + 0.005N _{std}	0.111 + 0.004N _{std}
		t _{PHL}	0.418 + 0.004N _{std}	0.255 + 0.003N _{std}	0.168 + 0.002N _{std}
D1-L1	K	t _{PLH}	0.333 + 0.003N _{std}	0.216 + 0.002N _{std}	0.152 + 0.002N _{std}
		t _{PHL}	0.391 + 0.003N _{std}	0.247 + 0.002N _{std}	0.171 + 0.002N _{std}
C2-L2		t _{PLH}	0.303 + 0.003N _{std}	0.186 + 0.002N _{std}	0.123 + 0.002N _{std}
		t _{PHL}	0.334 + 0.003N _{std}	0.204 + 0.002N _{std}	0.136 + 0.002N _{std}
D2-L2		t _{PLH}	0.304 + 0.003N _{std}	0.199 + 0.002N _{std}	0.141 + 0.002N _{std}
		t _{PHL}	0.364 + 0.003N _{std}	0.231 + 0.002N _{std}	0.160 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	0.523	0.523	0.522
B	0.530	0.530	0.530
C1	0.318	0.318	0.318
C2	0.315	0.315	0.318
D1	0.592	0.593	0.593
D2	0.595	0.595	0.594
I	0.747	0.772	0.850
Internal	7.960	9.797	12.608
Cell Units	30 cells	32 cells	38 cells



Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.280976	0.331505	0.232099
Hold	-0.142326	-0.177683	-0.109785

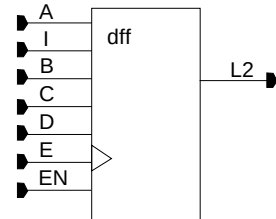
¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

Cell: LDE0001

Function: D Mimic FF, LSSD, w/Clock Enable, +L2 Output

Description:

This is a combination of a clock splitter and an LPH0001 LPC L1/L2 latch. The operation is a D mimic flip-flop. When the EN pin is low, the E clock to the latch is disabled. To avoid chopping of the clocks to the L1 and L2 portions of the latch, the state of the EN pin should only be changed while the E is low.



- A A clock
- B B clock
- C C clock
- D Data in
- E E clock
- EN Clock enable
- I Scan-in
- L2 +L2 output (in phase with respect to input)

LSSD Latch L1 Truth Table

Inputs						L1 State
EN	A	I	C	D	E	
X	0	X	0	X	X	NC
X	1	X	0	X	X	I
X	0	X	1	X	0	D
1	0	X	1	X	1	NC
0	0	X	1	X	X	D

LSSD Latch L2 Truth Table

Inputs					Output L2
L1	B	C	E	EN	
X	0	X	X	X	NC
X	1	1	0	X	NC
X	1	X	1	1	L1
X	1	1	X	0	NC
X	1	0	X	X	L1



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
E-L2	E	t _{PLH}	0.335 + 0.013N _{std}	0.210 + 0.009N _{std}	0.141 + 0.007N _{std}
		t _{PHL}	0.338 + 0.014N _{std}	0.213 + 0.009N _{std}	0.143 + 0.007N _{std}
	H	t _{PLH}	0.347 + 0.006N _{std}	0.216 + 0.004N _{std}	0.144 + 0.003N _{std}
		t _{PHL}	0.351 + 0.006N _{std}	0.220 + 0.004N _{std}	0.148 + 0.003N _{std}
	K	t _{PLH}	0.372 + 0.003N _{std}	0.232 + 0.002N _{std}	0.155 + 0.002N _{std}
		t _{PHL}	0.375 + 0.003N _{std}	0.236 + 0.002N _{std}	0.158 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	1.093	1.093	1.093
B	1.024	1.023	1.023
C	0.904	0.905	0.905
D	0.931	0.931	0.931
E	0.949	0.949	0.949
EN	0.977	0.977	0.977
I	0.471	0.471	0.471
Internal	15.675	16.909	19.592
Cell Units	41 cells	42 cells	44 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.042258	0.047417	0.047417
Hold	0.022322	0.025864	0.025864

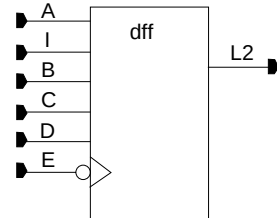
¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

Cell: LDF0001

Function: Falling Edge Triggered D Mimic FF, LSSD, +L2 Output

Description:

This is a D mimic flip-flop triggered at the falling edge of E clock. It consists of a combination of a clock splitter and an LSSD latch. When the C pin is low, the E clock is disabled.



- A A clock
- B B clock
- C C clock
- D Data in
- E E clock
- I Scan-in
- L2 +L2 output (in phase with respect to input)

LSSD Latch L1 Truth Table

Inputs					L1 State
A	I	C	D	E	
0	X	0	X	X	NC
1	X	0	X	X	I
0	X	1	X	0	NC
0	X	1	X	1	D

LSSD Latch L2 Truth Table

Inputs				Output L2
L1	B	C	E	
X	0	X	X	NC
X	1	X	0	L1
X	1	1	1	NC
X	1	0	X	L1



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
E-L2	E	t _{PLH}	0.399 + 0.013N _{std}	0.258 + 0.009N _{std}	0.182 + 0.007N _{std}
		t _{PHL}	0.415 + 0.014N _{std}	0.270 + 0.009N _{std}	0.190 + 0.007N _{std}
	H	t _{PLH}	0.413 + 0.006N _{std}	0.267 + 0.004N _{std}	0.188 + 0.003N _{std}
		t _{PHL}	0.431 + 0.006N _{std}	0.280 + 0.004N _{std}	0.197 + 0.003N _{std}
	K	t _{PLH}	0.438 + 0.003N _{std}	0.283 + 0.002N _{std}	0.199 + 0.002N _{std}
		t _{PHL}	0.455 + 0.002N _{std}	0.294 + 0.002N _{std}	0.207 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	1.100	1.100	1.100
B	0.970	0.970	0.970
C	0.854	0.854	0.854
D	0.897	0.897	0.897
E	1.501	1.501	1.501
I	0.483	0.483	0.483
Internal	16.520	17.745	20.536
Cell Units	36 cells	36 cells	38 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.070500	0.074201	0.074201
Hold	-0.001991	0.003325	0.003325

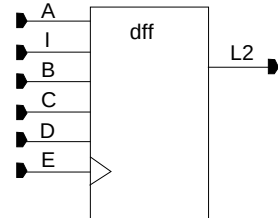
¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

Cell: LDR0001

Function: Rising Edge Triggered D Mimic FF, LSSD, +L2 Output

Description:

This is a D mimic flip-flop triggered at the rising edge of E clock. It consists of a combination of a clock splitter and an LSSD latch. When the C pin is low, the E clock is disabled.



- A A clock
- B B clock
- C C clock
- D Data in
- E E clock
- I Scan-in
- L2 +L2 output (in phase with respect to input)

LSSD Latch L1 Truth Table

Inputs					L1 State
A	I	C	D	E	
0	X	0	X	X	NC
1	X	0	X	X	I
0	X	1	X	0	D
0	X	1	X	1	NC

LSSD Latch L2 Truth Table

Inputs				Output
L1	B	C	E	
X	0	X	X	NC
X	1	1	0	NC
X	1	X	1	L1
X	1	0	X	L1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
E-L2	E	t _{PLH}	0.415 + 0.013N _{std}	0.259 + 0.009N _{std}	0.179 + 0.007N _{std}
		t _{PHL}	0.418 + 0.014N _{std}	0.262 + 0.009N _{std}	0.182 + 0.007N _{std}
	H	t _{PLH}	0.424 + 0.006N _{std}	0.266 + 0.004N _{std}	0.184 + 0.003N _{std}
		t _{PHL}	0.430 + 0.006N _{std}	0.271 + 0.004N _{std}	0.187 + 0.003N _{std}
	K	t _{PLH}	0.449 + 0.003N _{std}	0.282 + 0.002N _{std}	0.196 + 0.002N _{std}
		t _{PHL}	0.453 + 0.002N _{std}	0.287 + 0.002N _{std}	0.199 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	1.102	1.102	1.102
B	1.066	1.066	1.069
C	0.951	0.951	0.951
D	0.891	0.891	0.891
E	1.500	1.500	1.500
I	0.475	0.475	0.475
Internal	15.275	16.513	19.390
Cell Units	40 cells	40 cells	42 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.034782	0.034746	0.038077
Hold	0.049474	0.049474	0.049474

¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

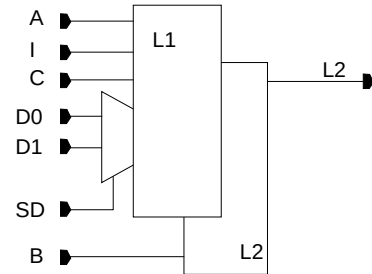
Cell: LMX0001

Function: D Latch, LSSD, +L2 Output w/MUX21 Input

Description:

This is a standard L1/L2 LSSD latch that is fully testable through scan rings using A and B clocks. This latch is also known as “master-slave” and is level-sensitive. Selects data from D0 or D1 based on the value of the SD input pin.

- A A clock
- B B clock
- C C clock
- D0 Data
- D1 Data
- I Scan-in
- SD Select data
- L2 +L2 output (in phase with respect to data input)



LSSD Latch L1 Truth Table

Inputs						L1 State
SD	D0	D1	A	I	C	
X	X	X	0	X	0	NC
X	X	X	1	X	0	I
0	X	X	0	X	1	D0
1	X	X	0	X	1	D1

LSSD Latch L2 Truth Table

Inputs		Output L2
L1	B	
X	0	NC
X	1	L1



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
B-L2	E	t _{PLH}	0.179 + 0.011N _{std}	0.114 + 0.007N _{std}	0.074 + 0.006N _{std}
		t _{PHL}	0.159 + 0.009N _{std}	0.098 + 0.006N _{std}	0.061 + 0.004N _{std}
	H	t _{PLH}	0.192 + 0.005N _{std}	0.122 + 0.004N _{std}	0.081 + 0.003N _{std}
		t _{PHL}	0.183 + 0.005N _{std}	0.114 + 0.003N _{std}	0.072 + 0.002N _{std}
	K	t _{PLH}	0.216 + 0.003N _{std}	0.139 + 0.002N _{std}	0.091 + 0.001N _{std}
		t _{PHL}	0.222 + 0.002N _{std}	0.140 + 0.001N _{std}	0.090 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	1.166	1.166	1.166
B	1.430	1.431	1.431
C	1.387	1.387	1.387
D0	2.324	2.324	2.324
D1	2.322	2.322	2.322
I	0.628	0.628	0.628
SD	1.831	1.831	1.831
Internal	6.926	8.464	12.579
Cell Units	29 cells	29 cells	32 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.218893	0.218893	0.218893
Hold	-0.110658	-0.110658	-0.110658

¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

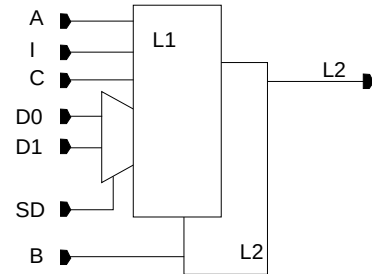
Cell: LMX0001_LPC

Function: D Latch, LSSD, +L2 Output w/MUX21 Input, Low Power

Description:

This is a low-power L1/L2 LSSD latch that is fully testable through scan rings using A and B clocks. This latch is also known as “master-slave” and is level-sensitive. Selects data from D0 or D1 based on the value of the SD input pin.

- A A clock
- B B clock
- C C clock
- D0 Data
- D1 Data
- I Scan-in
- SD Select data
- L2 +L2 output (in phase with respect to data input)



LSSD Latch L1 Truth Table

Inputs						L1 State
SD	D0	D1	A	I	C	
X	X	X	0	X	0	NC
X	X	X	1	X	0	I
0	X	X	0	X	1	D0
1	X	X	0	X	1	D1

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	L2
X	0	NC
X	1	L1



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
B-L2	E	t _{PLH}	0.155 + 0.014N _{std}	0.097 + 0.009N _{std}	0.067 + 0.007N _{std}
		t _{PHL}	0.247 + 0.009N _{std}	0.149 + 0.006N _{std}	0.096 + 0.004N _{std}
	H	t _{PLH}	0.186 + 0.008N _{std}	0.116 + 0.005N _{std}	0.080 + 0.004N _{std}
		t _{PHL}	0.296 + 0.005N _{std}	0.179 + 0.003N _{std}	0.114 + 0.002N _{std}
	K	t _{PLH}	0.300 + 0.003N _{std}	0.182 + 0.002N _{std}	0.118 + 0.002N _{std}
		t _{PHL}	0.276 + 0.003N _{std}	0.172 + 0.002N _{std}	0.117 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	0.524	0.524	0.524
B	0.343	0.343	0.342
C	0.317	0.317	0.317
D0	1.346	1.346	1.346
D1	1.261	1.261	1.261
I	0.357	0.357	0.358
SD	0.731	0.731	0.731
Internal	6.087	7.975	11.300
Cell Units	25 cells	25 cells	29 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.276757	0.280023	0.277923
Hold	-0.151524	-0.154415	-0.152094

¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

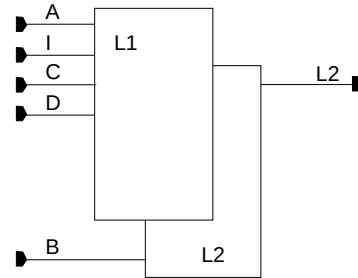
Cell: LPH0001

Function: D Latch, LSSD, +L2 Output

Description:

This is a standard L1/L2 LSSD latch that is fully testable through scan rings using A and B clocks. This latch is also known as “master-slave” and is level-sensitive.

- A A clock
- B B clock
- C C clock
- D Data
- I Scan-in
- L2 +L2 output (in phase with respect to data input)



LSSD Latch L1 Truth Table

Inputs				L1 State
A	I	C	D	
0	X	0	X	NC
1	X	0	X	I
0	X	1	X	D

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	
X	0	NC
X	1	L1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
B-L2	E	t _{PLH}	0.167 + 0.011N _{std}	0.108 + 0.007N _{std}	0.072 + 0.006N _{std}
		t _{PHL}	0.161 + 0.009N _{std}	0.102 + 0.006N _{std}	0.065 + 0.004N _{std}
	H	t _{PLH}	0.180 + 0.006N _{std}	0.115 + 0.004N _{std}	0.075 + 0.003N _{std}
		t _{PHL}	0.184 + 0.004N _{std}	0.115 + 0.003N _{std}	0.073 + 0.002N _{std}
	K	t _{PLH}	0.202 + 0.003N _{std}	0.130 + 0.002N _{std}	0.086 + 0.001N _{std}
		t _{PHL}	0.224 + 0.002N _{std}	0.142 + 0.001N _{std}	0.091 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	1.211	1.211	1.211
B	1.428	1.428	1.429
C	1.550	1.550	1.550
D	0.767	0.767	0.767
I	0.638	0.638	0.638
Internal	6.387	7.707	11.000
Cell Units	24 cells	24 cells	27 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.191098	0.188789	0.188789
Hold	-0.087629	-0.087591	-0.087591

¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

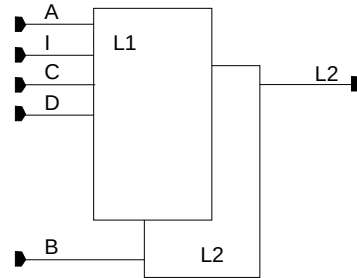
Cell: LPH0001_LPC

Function: D Latch, LSSD, +L2 Output, Low Power

Description:

This is a low-power L1/L2 LSSD latch that is fully testable through scan rings using A and B clocks. This latch is also known as “master-slave” and is level-sensitive.

- A A clock
- B B clock
- C C clock
- D Data
- I Scan-in
- L2 +L2 output (in phase with respect to data input)



LSSD Latch L1 Truth Table

Inputs				L1 State
A	I	C	D	
0	X	0	X	NC
1	X	0	X	I
0	X	1	X	D

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	
X	0	NC
X	1	L1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
B-L2	E	t _{PLH}	0.158 + 0.014N _{std}	0.102 + 0.009N _{std}	0.072 + 0.007N _{std}
		t _{PHL}	0.251 + 0.008N _{std}	0.155 + 0.005N _{std}	0.101 + 0.004N _{std}
	H	t _{PLH}	0.187 + 0.008N _{std}	0.117 + 0.005N _{std}	0.081 + 0.004N _{std}
		t _{PHL}	0.300 + 0.005N _{std}	0.182 + 0.003N _{std}	0.116 + 0.002N _{std}
	K	t _{PLH}	0.300 + 0.003N _{std}	0.182 + 0.002N _{std}	0.118 + 0.002N _{std}
		t _{PHL}	0.277 + 0.003N _{std}	0.173 + 0.002N _{std}	0.117 + 0.002N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	0.524	0.524	0.524
B	0.343	0.343	0.342
C	0.318	0.318	0.318
D	0.594	0.594	0.595
I	0.357	0.357	0.358
Internal	5.551	6.971	10.163
Cell Units	20 cells	20 cells	24 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.214454	0.215784	0.215233
Hold	-0.103317	-0.105301	-0.102132

¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

Cell: LPH0002

Function: D Latch, LSSD, L2N Output

Description:

This is a standard L1/L2 LSSD latch that is fully testable through scan rings using A and B clocks. This latch is also known as "master-slave" and is level-sensitive.

A A clock

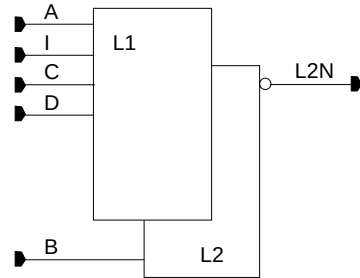
B B clock

C C clock

D Data

I Scan-in

L2N -L2 output (out of phase with respect to data input)



LSSD Latch L1 Truth Table

Inputs				L1 State
A	I	C	D	
0	X	0	X	NC
1	X	0	X	I
0	X	1	X	D

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	L2N
X	0	NC
X	1	$\overline{L1}$

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
B-L2N	E	t_{PLH}	$0.094 + 0.011N_{std}$	$0.061 + 0.007N_{std}$	$0.038 + 0.006N_{std}$
		t_{PHL}	$0.157 + 0.009N_{std}$	$0.106 + 0.006N_{std}$	$0.073 + 0.004N_{std}$
	H	t_{PLH}	$0.110 + 0.006N_{std}$	$0.070 + 0.004N_{std}$	$0.045 + 0.003N_{std}$
		t_{PHL}	$0.181 + 0.005N_{std}$	$0.119 + 0.003N_{std}$	$0.080 + 0.002N_{std}$
	K	t_{PLH}	$0.147 + 0.003N_{std}$	$0.095 + 0.002N_{std}$	$0.064 + 0.001N_{std}$
		t_{PHL}	$0.234 + 0.002N_{std}$	$0.155 + 0.002N_{std}$	$0.105 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	1.211	1.211	1.211
B	1.564	1.541	1.516
C	1.550	1.550	1.550
D	0.767	0.767	0.767
I	0.638	0.638	0.638
Internal	5.576	7.045	10.545
Cell Units	24 cells	24 cells	27 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.191098	0.188789	0.188789
Hold	-0.087629	-0.087591	-0.087591

¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

Cell: LPH0101

Function: D Latch, LSSD, +L1, +L2 Outputs

Description:

This is a standard L1/L2 LSSD latch that is fully testable through scan rings using A and B clocks. This latch is also known as “master-slave” and is level-sensitive.

A A clock

B B clock

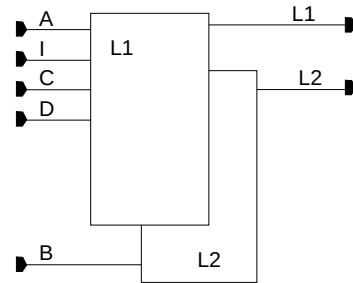
C C clock

D Data

I Scan-in

L1 +L1 output (in phase with respect to data input)

L2 +L2 output (in phase with respect to data input)



LSSD Latch L1 Truth Table

Inputs				Output
A	I	C	D	L1
0	X	0	X	NC
1	X	0	X	I
0	X	1	X	D

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	L2
X	0	NC
X	1	L1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D-L1	E	t _{PLH}	0.141 + 0.011N _{std}	0.094 + 0.007N _{std}	0.065 + 0.005N _{std}
		t _{PHL}	0.233 + 0.009N _{std}	0.166 + 0.006N _{std}	0.125 + 0.004N _{std}
B-L2		t _{PLH}	0.166 + 0.011N _{std}	0.107 + 0.007N _{std}	0.072 + 0.006N _{std}
		t _{PHL}	0.160 + 0.009N _{std}	0.102 + 0.006N _{std}	0.065 + 0.004N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D-L1	H	t _{PLH}	0.163 + 0.005N _{std}	0.105 + 0.004N _{std}	0.072 + 0.003N _{std}
		t _{PHL}	0.273 + 0.005N _{std}	0.193 + 0.003N _{std}	0.143 + 0.002N _{std}
B-L2		t _{PLH}	0.178 + 0.006N _{std}	0.113 + 0.004N _{std}	0.075 + 0.003N _{std}
		t _{PHL}	0.183 + 0.005N _{std}	0.115 + 0.003N _{std}	0.072 + 0.002N _{std}
D-L1	K	t _{PLH}	0.202 + 0.003N _{std}	0.131 + 0.002N _{std}	0.091 + 0.001N _{std}
		t _{PHL}	0.339 + 0.002N _{std}	0.237 + 0.002N _{std}	0.174 + 0.001N _{std}
B-L2		t _{PLH}	0.202 + 0.003N _{std}	0.129 + 0.002N _{std}	0.086 + 0.001N _{std}
		t _{PHL}	0.223 + 0.002N _{std}	0.141 + 0.001N _{std}	0.091 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	1.212	1.212	1.215
B	1.428	1.428	1.429
C	1.550	1.553	1.558
D	0.768	0.769	0.769
I	0.637	0.637	0.638
Internal	10.474	12.730	18.387
Cell Units	27 cells	27 cells	32 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.222257	0.252030	0.303508
Hold	-0.110458	-0.128303	-0.168972

^{1.} Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

Cell: LPH0101_LPC

Function: D Latch, LSSD, +L1, +L2 Outputs, Low Power

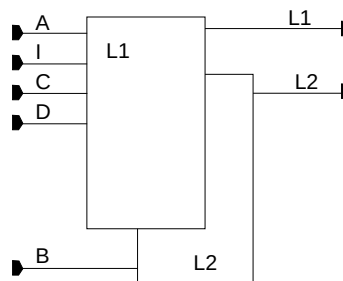
Description:

This is a low-power L1/L2 LSSD latch that is fully testable through scan rings using A and B clocks. This latch is also known as "master-slave" and is level-sensitive.

A A clock
B B clock
C C clock
D Data
I Scan-in

L1 +L1 output (in phase with respect to data input)

L2 +L2 output (in phase with respect to data input)



LSSD Latch L1 Truth Table

Inputs				Output
A	I	C	D	L1
0	X	0	X	NC
1	X	0	X	I
0	X	1	X	D

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	L2
X	0	NC
X	1	L1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D-L1	E	t _{PLH}	0.199 + 0.014N _{std}	0.138 + 0.009N _{std}	0.105 + 0.007N _{std}
		t _{PHL}	0.398 + 0.007N _{std}	0.246 + 0.004N _{std}	0.164 + 0.003N _{std}
B-L2		t _{PLH}	0.158 + 0.014N _{std}	0.102 + 0.009N _{std}	0.072 + 0.007N _{std}
		t _{PHL}	0.250 + 0.008N _{std}	0.155 + 0.005N _{std}	0.101 + 0.004N _{std}
D-L1	H	t _{PLH}	0.237 + 0.008N _{std}	0.159 + 0.005N _{std}	0.118 + 0.004N _{std}
		t _{PHL}	0.457 + 0.004N _{std}	0.278 + 0.003N _{std}	0.182 + 0.002N _{std}
B-L2		t _{PLH}	0.187 + 0.008N _{std}	0.117 + 0.005N _{std}	0.081 + 0.004N _{std}
		t _{PHL}	0.299 + 0.005N _{std}	0.181 + 0.003N _{std}	0.116 + 0.002N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D-L1	K	t _{PLH}	0.340 + 0.003N _{std}	0.222 + 0.002N _{std}	0.155 + 0.002N _{std}
		t _{PHL}	0.381 + 0.003N _{std}	0.240 + 0.002N _{std}	0.165 + 0.002N _{std}
B-L2		t _{PLH}	0.300 + 0.003N _{std}	0.182 + 0.002N _{std}	0.118 + 0.002N _{std}
		t _{PHL}	0.277 + 0.003N _{std}	0.173 + 0.002N _{std}	0.117 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	0.525	0.524	0.524
B	0.343	0.343	0.342
C	0.318	0.318	0.318
D	0.593	0.594	0.595
I	0.357	0.357	0.358
Internal	9.524	11.235	13.963
Cell Units	22 cells	22 cells	29 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.299079	0.344963	0.248168
Hold	-0.157394	-0.184678	-0.121764

¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

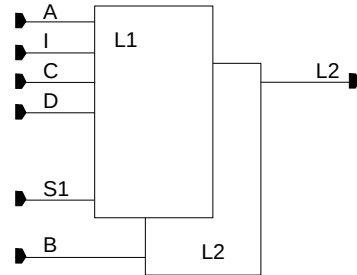
Cell: LPH1001_LPC

Function: D Latch, LSSD, +L2 Output, +Asyn Set L1, Low Power

Description:

This is a low-power L1/L2 LSSD latch that is fully testable through scan rings using A and B clocks. This latch is also known as “master-slave” and is level-sensitive. S1 pin (asynchronous set L1) will set the L1 latch any-time it is activated. The pin S1 is positive active.

- A A clock
- B B clock
- C C clock
- D Data
- I Scan-in
- S1 Direct set for L1 (positive active)
- L2 +L2 output (in phase with respect to data input)



LSSD Latch L1 Truth Table

Inputs					L1 State
S1	A	I	C	D	
0	0	X	0	X	NC
1	X	X	X	X	1
0	1	X	0	X	I
0	0	X	1	X	D

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	L2
X	0	NC
X	1	L1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
B-L2	E	t _{PLH}	0.157 + 0.014N _{std}	0.100 + 0.009N _{std}	0.071 + 0.007N _{std}
		t _{PHL}	0.247 + 0.009N _{std}	0.152 + 0.006N _{std}	0.099 + 0.004N _{std}
	H	t _{PLH}	0.186 + 0.008N _{std}	0.116 + 0.005N _{std}	0.080 + 0.004N _{std}
		t _{PHL}	0.296 + 0.005N _{std}	0.179 + 0.003N _{std}	0.114 + 0.002N _{std}
	K	t _{PLH}	0.300 + 0.003N _{std}	0.182 + 0.002N _{std}	0.118 + 0.002N _{std}
		t _{PHL}	0.276 + 0.003N _{std}	0.172 + 0.002N _{std}	0.117 + 0.002N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	0.524	0.524	0.524
B	0.343	0.343	0.342
C	0.317	0.317	0.317
D	0.504	0.504	0.504
I	0.357	0.357	0.358
S1	0.593	0.593	0.593
Internal	7.838	9.308	10.276
Cell Units	23 cells	23 cells	27 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.334722	0.338861	0.337250
Hold	-0.193556	-0.195493	-0.193332

¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

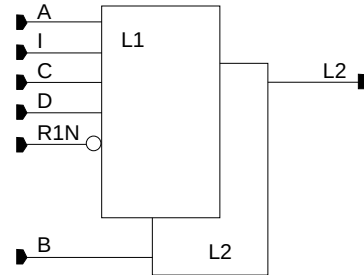
Cell: LPH4001_LPC

Function: D Latch, LSSD, +L2 Output, -Asyn Reset L1, Low Power

Description:

This is a low-power L1/L2 LSSD latch that is fully testable through scan rings using A and B clocks. This latch is also known as “master-slave” and is level-sensitive. R1N resets the L1 latch anytime it is activated. The pin R1N is negative active.

- A A clock
- B B clock
- C C clock
- D Data
- I Scan-in
- R1N Direct reset for L1 (negative active)
- L2 +L2 output (in phase with respect to data input)



LSSD Latch L1 Truth Table

Inputs					L1 State
R1N	A	I	C	D	
1	0	X	0	X	NC
0	X	X	X	X	0
1	0	X	1	X	D
1	1	X	0	X	I

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	L2
X	0	NC
X	1	L1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
B-L2	E	t _{PLH}	0.158 + 0.014N _{std}	0.102 + 0.009N _{std}	0.072 + 0.007N _{std}
		t _{PHL}	0.250 + 0.008N _{std}	0.155 + 0.005N _{std}	0.101 + 0.004N _{std}
	H	t _{PLH}	0.187 + 0.008N _{std}	0.117 + 0.005N _{std}	0.081 + 0.004N _{std}
		t _{PHL}	0.299 + 0.005N _{std}	0.182 + 0.003N _{std}	0.116 + 0.002N _{std}
	K	t _{PLH}	0.300 + 0.003N _{std}	0.182 + 0.002N _{std}	0.118 + 0.002N _{std}
		t _{PHL}	0.277 + 0.003N _{std}	0.173 + 0.002N _{std}	0.117 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	0.524	0.524	0.524
B	0.343	0.343	0.342
C	0.317	0.317	0.317
D	0.570	0.570	0.570
I	0.357	0.357	0.358
R1N	0.633	0.633	0.633
Internal	8.516	9.876	13.033
Cell Units	23 cells	23 cells	27 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.358340	0.360650	0.363663
Hold	-0.210771	-0.212029	-0.213918

¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

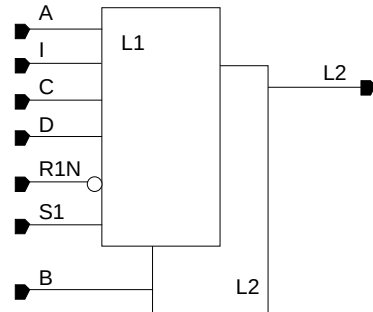
Cell: LPH6001

Function: D Latch, LSSD, +L2 Output, +Asyn Set L1, -Asyn Reset L1

Description:

This is a L1/L2 LSSD latch that is fully testable through scan rings using A and B clocks. This latch is also known as "master-slave" and is level-sensitive. S1 sets the L1 latch anytime it is activated. R1N resets the L1 latch if S1 is not active. The R1N input is negative active. The S1 input is positive active and is the dominant input.

- A A clock
- B B clock
- C C clock
- D Data
- I Scan-in
- R1N Direct reset for L1 (negative active)
- S1 Direct set for L1 (positive active)
- L2 +L2 output (in phase with respect to data input)



LSSD Latch L1 Truth Table

Inputs						L1 State
S1	R1N	A	I	C	D	
1	X	X	X	X	X	1
0	0	X	X	X	X	0
0	1	1	X	0	X	I
0	1	0	X	1	X	D
0	1	0	X	0	X	NC

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	
X	0	NC
X	1	L1

**Propagation Delays**

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
B-L2	E	t_{PLH}	$0.119 + 0.011N_{std}$	$0.079 + 0.008N_{std}$	$0.053 + 0.006N_{std}$
		t_{PHL}	$0.207 + 0.009N_{std}$	$0.134 + 0.006N_{std}$	$0.089 + 0.004N_{std}$
	H	t_{PLH}	$0.136 + 0.006N_{std}$	$0.088 + 0.004N_{std}$	$0.060 + 0.003N_{std}$
		t_{PHL}	$0.234 + 0.005N_{std}$	$0.150 + 0.003N_{std}$	$0.098 + 0.002N_{std}$
	K	t_{PLH}	$0.240 + 0.003N_{std}$	$0.151 + 0.002N_{std}$	$0.100 + 0.001N_{std}$
		t_{PHL}	$0.302 + 0.002N_{std}$	$0.190 + 0.002N_{std}$	$0.125 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	1.167	1.167	1.167
B	1.574	1.577	1.570
C	1.550	1.550	1.550
D	0.767	0.767	0.767
I	0.621	0.621	0.621
R1N	1.078	1.078	1.078
S1	1.182	1.182	1.182
Internal	11.374	12.982	17.602
Cell Units	32 cells	32 cells	36 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.254529	0.256672	0.256672
Hold	-0.120155	-0.122530	-0.122530

¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

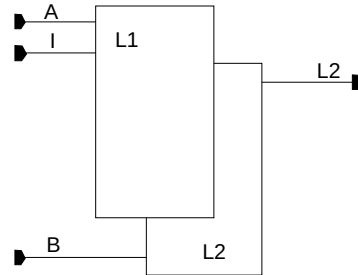
Cell: LSC0001_LPC

Function: Scan-Only Latch, LSSD, Low Power

Description:

The low-power scan-only latch is used only in the scan ring and has scan-in input.

- A A clock
- B B clock
- I Scan-in
- L2 +L2 output (in phase with respect to scan-in input)



LSSD Latch L1 Truth Table

Inputs		L1 State
A	I	
0	X	NC
1	X	I

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	L2
X	0	NC
X	1	L1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
B-L2	E	t _{PLH}	0.154 + 0.014N _{std}	0.099 + 0.009N _{std}	0.068 + 0.007N _{std}
		t _{PHL}	0.283 + 0.008N _{std}	0.174 + 0.005N _{std}	0.114 + 0.004N _{std}
	H	t _{PLH}	0.184 + 0.008N _{std}	0.115 + 0.005N _{std}	0.078 + 0.004N _{std}
		t _{PHL}	0.341 + 0.005N _{std}	0.205 + 0.003N _{std}	0.132 + 0.002N _{std}
	K	t _{PLH}	0.302 + 0.003N _{std}	0.183 + 0.002N _{std}	0.118 + 0.002N _{std}
		t _{PHL}	0.277 + 0.003N _{std}	0.174 + 0.002N _{std}	0.118 + 0.002N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	0.317	0.317	0.317
B	0.341	0.341	0.344
I	0.885	0.887	0.932
Internal	5.623	7.096	10.186
Cell Units	16 cells	16 cells	19 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.195589	0.195590	0.194771
Hold	-0.092706	-0.092706	-0.092706

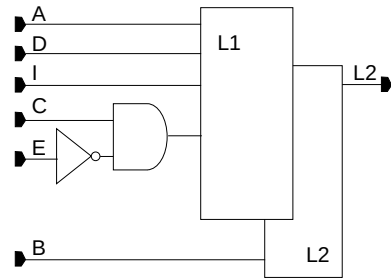
¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

Cell: LTL0001

Function: Transparent Latch, LSSD, + L2 Output

Description:

This is a transparent/LSSD latch that is fully testable through scan rings using A and B clocks. In normal use, the A pin is held low and the B and C pins are held high while the E pin is clocked, resulting in a transparent latch function (+L2 output = D input while E pin = 0). For LSSD mode, the E pin is held low and the A, B, and C pins can be used for the LSSD capture and scan functions of a "master-slave" latch.



- A A clock
- B B clock
- C C clock
- D Data
- E Oscillator clock (negative active)
- I Scan-in
- L2 +L2 output (in phase with respect to data input)

LSSD Latch L1 Truth Table

Inputs					L1 State
E	A	I	C	D	
0	0	X	0	X	NC
0	1	X	0	X	I
0	0	X	1	X	D
1	0	X	1	X	NC

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	
X	0	NC
X	1	L1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D-L2	E	t _{PLH}	0.359 + 0.017N _{std}	0.224 + 0.012N _{std}	0.151 + 0.009N _{std}
		t _{PHL}	0.432 + 0.014N _{std}	0.273 + 0.010N _{std}	0.192 + 0.007N _{std}
E-L2		t _{PLH}	0.795 + 0.016N _{std}	0.327 + 0.012N _{std}	0.322 + 0.008N _{std}
		t _{PHL}	0.533 + 0.014N _{std}	0.336 + 0.010N _{std}	0.234 + 0.007N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D-L2	H	t _{PLH}	0.388 + 0.008N _{std}	0.398 + 0.005N _{std}	0.262 + 0.004N _{std}
		t _{PHL}	0.503 + 0.007N _{std}	0.317 + 0.004N _{std}	0.222 + 0.003N _{std}
E-L2		t _{PLH}	0.824 + 0.008N _{std}	0.503 + 0.005N _{std}	0.340 + 0.004N _{std}
		t _{PHL}	0.605 + 0.007N _{std}	0.381 + 0.004N _{std}	0.268 + 0.003N _{std}
D-L2	K	t _{PLH}	0.472 + 0.003N _{std}	0.453 + 0.002N _{std}	0.300 + 0.002N _{std}
		t _{PHL}	0.648 + 0.003N _{std}	0.410 + 0.002N _{std}	0.284 + 0.001N _{std}
E-L2		t _{PLH}	0.911 + 0.003N _{std}	0.558 + 0.002N _{std}	0.378 + 0.002N _{std}
		t _{PHL}	0.750 + 0.003N _{std}	0.475 + 0.002N _{std}	0.330 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
A	1.095	1.095	1.095
B	1.637	1.637	1.638
C	0.871	0.871	0.871
D	0.935	0.933	0.933
E	0.992	0.992	0.992
I	0.474	0.474	0.474
Internal	5.891	7.127	11.693
Cell Units	30 cells	31 cells	34 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.084079	0.084079	0.084079
Hold	-0.012658	-0.012658	-0.012656

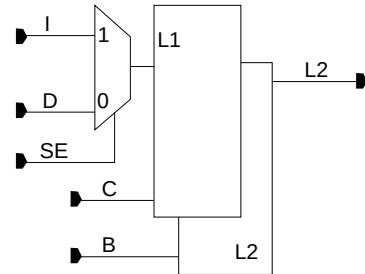
¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

Cell: MPH0001_LPC

Function: D MUX Latch, LSSD, +L2 Output

Description:

This is a MUX scan L1/L2 LSSD latch which uses the scan enable (SE) pin to multiplex either the normal data (D) or scan data (I) into the L1 portion of the latch. When the B and C clock inputs are driven from the CLKSP1 (clock splitter), full D flip-flop with scan operation can be achieved, as well as full LSSD testability.



B B clock

C C clock

D Data

SE Scan enable

I Scan-in

L2 +L2 output (in phase with respect to data input)

LSSD Latch L1 Truth Table

Inputs				L1 State
I	C	D	SE	
X	0	X	X	NC
X	1	X	0	D
X	1	X	1	I

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	L2
X	0	NC
X	1	L1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
B-L2	E	t _{PLH}	0.158 + 0.013N _{std}	0.105 + 0.009N _{std}	0.082 + 0.007N _{std}
		t _{PHL}	0.247 + 0.008N _{std}	0.156 + 0.006N _{std}	0.111 + 0.004N _{std}
	H	t _{PLH}	0.188 + 0.007N _{std}	0.124 + 0.005N _{std}	0.097 + 0.004N _{std}
		t _{PHL}	0.295 + 0.005N _{std}	0.186 + 0.003N _{std}	0.131 + 0.002N _{std}
	K	t _{PLH}	0.297 + 0.003N _{std}	0.186 + 0.002N _{std}	0.133 + 0.002N _{std}
		t _{PHL}	0.273 + 0.003N _{std}	0.177 + 0.002N _{std}	0.132 + 0.002N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
B	0.341	0.341	0.344
C	0.317	0.317	0.317
D	1.163	1.163	1.163
I	1.201	1.203	1.269
SE	0.722	0.722	0.722
Internal	5.749	7.383	10.505
Cell Units	21 cells	21 cells	24 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.235146	0.235146	0.236394
Hold	-0.120817	-0.120817	-0.122346

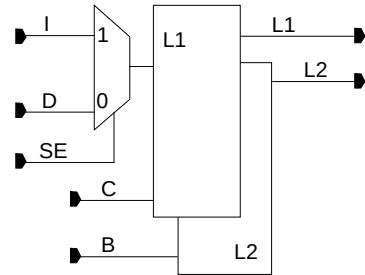
¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

Cell: MPH0101_LPC

Function: D MUX Latch, LSSD, +L1, +L2 Output

Description:

This is a MUX scan L1/L2 LSSD latch which uses the scan enable (SE) pin to multiplex either the normal data (D) or scan data (I) into the L1 portion of the latch. This latch is also known as “master-slave” and is level-sensitive. When the B and C clock inputs are driven from the CLKSP1 (clock splitter), full D flip-flop with scan operation can be achieved, as well as full LSSD testability.



B B clock

C C clock

D Data

I Scan-in

SE Scan enable

L1 +L1 output (in phase with respect to data input)

L2 +L2 output (in phase with respect to data input)

LSSD Latch L1 Truth Table

Inputs				Output
I	C	D	SE	L1
X	0	X	X	NC
X	1	X	0	D
X	1	X	1	I

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	L2
X	0	NC
X	1	L1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D-L1	E	t _{PLH}	0.223 + 0.013N _{std}	0.154 + 0.009N _{std}	0.124 + 0.007N _{std}
		t _{PHL}	0.392 + 0.007N _{std}	0.252 + 0.005N _{std}	0.186 + 0.004N _{std}
B-L2		t _{PLH}	0.158 + 0.013N _{std}	0.105 + 0.009N _{std}	0.082 + 0.007N _{std}
		t _{PHL}	0.247 + 0.008N _{std}	0.156 + 0.006N _{std}	0.111 + 0.004N _{std}



Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D-L1	H	t _{PLH}	0.255 + 0.008N _{std}	0.175 + 0.005N _{std}	0.139 + 0.004N _{std}
		t _{PHL}	0.446 + 0.004N _{std}	0.285 + 0.003N _{std}	0.208 + 0.002N _{std}
B-L2		t _{PLH}	0.188 + 0.007N _{std}	0.124 + 0.005N _{std}	0.097 + 0.004N _{std}
		t _{PHL}	0.295 + 0.005N _{std}	0.186 + 0.003N _{std}	0.131 + 0.002N _{std}
D-L1	K	t _{PLH}	0.360 + 0.003N _{std}	0.235 + 0.002N _{std}	0.175 + 0.002N _{std}
		t _{PHL}	0.394 + 0.003N _{std}	0.259 + 0.002N _{std}	0.199 + 0.002N _{std}
B-L2		t _{PLH}	0.297 + 0.003N _{std}	0.185 + 0.002N _{std}	0.133 + 0.002N _{std}
		t _{PHL}	0.273 + 0.003N _{std}	0.177 + 0.002N _{std}	0.132 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
B	0.341	0.341	0.344
C	0.317	0.317	0.317
D	1.189	1.189	1.215
I	1.252	1.255	1.412
SE	0.722	0.722	0.722
Internal	8.603	10.421	12.965
Cell Units	24 cells	24 cells	30 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.315836	0.356868	0.275081
Hold	-0.173414	-0.199083	-0.151624

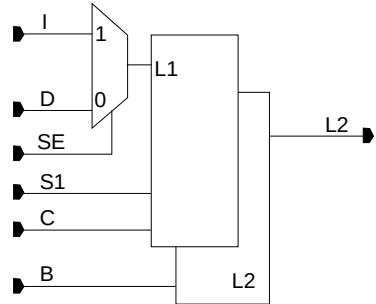
¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

Cell: MPH1001_LPC

Function: D MUX Latch, LSSD, + L2 Output, +Asyn Set L1

Description:

This is a MUX scan L1/L2 LSSD latch which uses the scan enable (SE) pin to multiplex either the normal data (D) or scan data (I) into the L1 portion of the latch. This latch is also known as “master slave” and is level-sensitive. When the B and C clock inputs are driven from the CLKSP1 (clock splitter), full D flip-flop with scan operation can be achieved, as well as full LSSD testability. S1 = 1 (asynchronous set L1) will set the L1 latch regardless of the states of pins C, D, I, or SE.



- B B clock
- C C clock
- D Data
- I Scan-in
- SE Scan enable
- S1 Direct set of L1 (positive active)
- L2 +L2 output (in phase with respect to data input)

LSSD Latch L1 Truth Table

Inputs					L1 State
S1	I	C	D	SE	
0	X	0	X	X	NC
0	X	1	X	0	D
0	X	1	X	1	I
1	X	X	X	X	1

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	L2
X	0	NC
X	1	L1



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
B-L2	E	t _{PLH}	0.158 + 0.013N _{std}	0.105 + 0.009N _{std}	0.082 + 0.007N _{std}
		t _{PHL}	0.247 + 0.008N _{std}	0.156 + 0.006N _{std}	0.111 + 0.004N _{std}
	H	t _{PLH}	0.188 + 0.007N _{std}	0.124 + 0.005N _{std}	0.097 + 0.004N _{std}
		t _{PHL}	0.295 + 0.005N _{std}	0.186 + 0.003N _{std}	0.131 + 0.002N _{std}
	K	t _{PLH}	0.297 + 0.003N _{std}	0.185 + 0.002N _{std}	0.133 + 0.002N _{std}
		t _{PHL}	0.273 + 0.003N _{std}	0.177 + 0.002N _{std}	0.132 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
B	0.341	0.341	0.344
C	0.316	0.316	0.316
D	1.098	1.098	1.099
I	1.181	1.182	1.249
S1	0.586	0.586	0.586
SE	0.721	0.721	0.721
Internal	7.825	9.418	12.563
Cell Units	25 cells	25 cells	28 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.339500	0.338163	0.337306
Hold	-0.197736	-0.196754	-0.194586

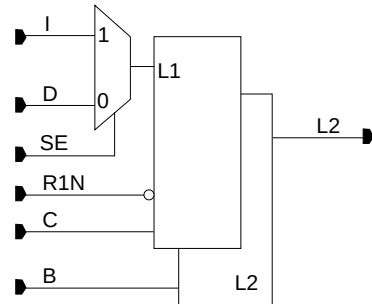
¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.

Cell: MPH4001_LPC

Function: D MUX Latch, LSSD, +L2 Output, -Asyn Reset L1

Description:

This is a MUX scan L1/L2 LSSD latch which uses the scan enable (SE) pin to multiplex either the normal data (D) or scan data (I) into the L1 portion of the latch. This latch is also known as “master-slave” and is level-sensitive. When the B and C clock inputs are driven from the CLKSP (clock splitter), full D flip-flop with scan operation can be achieved, as well as full LSSD testability. R1N = 0 (asynchronous reset L1) will reset the L1 latch regardless of the states of pins C, D, I, or SE.



- B B clock
- C C clock
- D Data
- I Scan-in
- R1N Direct reset of L1 (negative active)
- SE Scan enable
- L2 +L2 output (in phase with respect to data input)

LSSD Latch L1 Truth Table

Inputs					L1 State
R1N	I	C	D	SE	
1	X	0	X	X	NC
1	X	1	X	0	D
1	X	1	X	1	I
0	X	X	X	X	0

LSSD Latch L2 Truth Table

Inputs		Output
L1	B	
X	0	NC
X	1	L1



Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
B-L2	E	t _{PLH}	0.158 + 0.013N _{std}	0.105 + 0.009N _{std}	0.082 + 0.007N _{std}
		t _{PHL}	0.247 + 0.008N _{std}	0.156 + 0.006N _{std}	0.111 + 0.004N _{std}
	H	t _{PLH}	0.188 + 0.007N _{std}	0.124 + 0.005N _{std}	0.097 + 0.004N _{std}
		t _{PHL}	0.295 + 0.005N _{std}	0.186 + 0.003N _{std}	0.131 + 0.002N _{std}
	K	t _{PLH}	0.297 + 0.003N _{std}	0.186 + 0.002N _{std}	0.133 + 0.002N _{std}
		t _{PHL}	0.273 + 0.003N _{std}	0.177 + 0.002N _{std}	0.132 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	E	H	K
B	0.341	0.341	0.344
C	0.317	0.317	0.317
D	1.129	1.129	1.129
I	1.210	1.211	1.274
R1N	0.631	0.631	0.631
SE	0.721	0.721	0.721
Internal	8.483	10.079	13.210
Cell Units	25 cells	25 cells	28 cells

Latch Setup and Hold Delays (ns)

Condition ¹	Performance Level		
	E	H	K
Setup	0.359235	0.359235	0.360650
Hold	-0.211544	-0.211544	-0.213212

¹. Setup and hold calculated using worst case conditions; clock and data slew rate = 0.2 ns.



Standard Cell Data Path

Technology Library Data Path Elements

Data path elements are library cells specifically designed for use in bit stacking structures. The pins of these library cells are positioned to facilitate wiring. The internal circuits are designed for input to output data-flow speed. Usage of the data path elements can only be done through instantiation during synthesis; the synthesis tools will not infer them. Restrictions on the use of the data path elements, specifically multiplexer cells MUX41I_DP and MUX81I_DP and decoder cells DEC24_DP and DEC38_DP, are described below.

Multiplexer and Decoder Restrictions

One, and only one, multiplexer select input must be active at any given time. To ensure this condition is met, a specific decoder must be used in conjunction with each multiplexer. All select inputs of each multiplexer must be connected to the outputs of a single decoder. No decoder output can be connected to more than one select input on any one multiplexer, but can be connected to a select input on each of several multiplexers. A multiplexer select input cannot be left floating, tied high, or tied low. More specifically, MUX41I_DP select inputs must be connected to DEC24_DP outputs, and MUX81I_DP select inputs must be connected to DEC38_DP outputs. There are checks in the release-to-layout and release-to-manufacturing sign-offs to ensure that these restrictions have not been violated.

Cell: DEC24_DP

Function: 2-to-4 Decoder

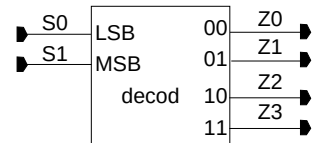
Description:

Two-to-four decoder designed for data path structures. Outputs are active high.

S0 LSB decode input

S1 MSB decode input

Z0-Z3 Decode outputs



Truth Table

Inputs		Outputs			
S1	S0	Z0	Z1	Z2	Z3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
S0-Z0	J	t _{PLH}	0.205 + 0.004N _{std}	0.140 + 0.003N _{std}	0.103 + 0.002N _{std}
		t _{PHL}	0.182 + 0.003N _{std}	0.121 + 0.002N _{std}	0.086 + 0.002N _{std}
S1-Z3		t _{PLH}	0.144 + 0.004N _{std}	0.093 + 0.003N _{std}	0.067 + 0.002N _{std}
		t _{PHL}	0.150 + 0.003N _{std}	0.111 + 0.002N _{std}	0.085 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	J
S0	2.810
S1	2.841
Internal	8.852
Cell Units	36 cells



Cell: DEC38_DP

Function: 3-to-8 Decoder

Description:

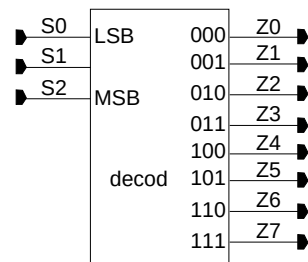
Three-to-eight decoder designed for data path structures. Outputs are active high.

S0 LSB decode input

S1 MSB-1 decode input

S2 MSB decode input

Z0-Z7 Decode outputs



Truth Table

Inputs			Outputs							
S2	S1	S0	Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
S0-Z0	J	t _{PLH}	0.268 + 0.004N _{std}	0.180 + 0.003N _{std}	0.131 + 0.002N _{std}
		t _{PHL}	0.249 + 0.003N _{std}	0.165 + 0.002N _{std}	0.115 + 0.002N _{std}
S2-Z7		t _{PLH}	0.168 + 0.004N _{std}	0.106 + 0.003N _{std}	0.073 + 0.002N _{std}
		t _{PHL}	0.197 + 0.003N _{std}	0.142 + 0.002N _{std}	0.109 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	J
S0	4.921
S1	4.999
S2	4.780
Internal	9.802
Cell Units	78 cells

Cell: MUX41I_DP

Function: 4:1 Multiplexer with Inverting Output

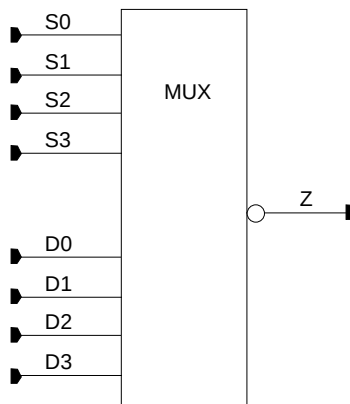
Description:

Four-to-one inverting multiplexer. Specifically designed for data path structures. Select lines (S0-S3) must all be driven from outputs (Z0-Z3) of the same DEC24_DP.

S0 - S3 Select inputs

D0 - D3 Data inputs

Z Outputs



Truth Table

Inputs ¹					Output ²
S0	S1	S2	S3	Dx	Z
1	0	0	0	X	$\overline{D0}$
0	1	0	0	X	$\overline{D1}$
0	0	1	0	X	$\overline{D2}$
0	0	0	1	X	$\overline{D3}$

1. One and only one input can be selected at any given time. Having two or more, or none, selected is not allowed.
2. Output is the inversion of the data input.

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D0-Z	F	t _{PLH}	0.120 + 0.011N _{std}	0.090 + 0.008N _{std}	0.070 + 0.006N _{std}
		t _{PHL}	0.117 + 0.008N _{std}	0.077 + 0.005N _{std}	0.050 + 0.004N _{std}
S0-Z		t _{PLH}	0.130 + 0.011N _{std}	0.082 + 0.007N _{std}	0.048 + 0.006N _{std}
		t _{PHL}	0.145 + 0.008N _{std}	0.095 + 0.005N _{std}	0.063 + 0.004N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	F
D0	2.578
D1	2.579
D2	2.586
D3	2.577
S0	0.796
S1	0.798
S2	0.802
S3	0.796
Internal	4.000
Cell Units	21 cells

Cell: MUX81I_DP

Function: 8:1 Multiplexer with Inverted Output

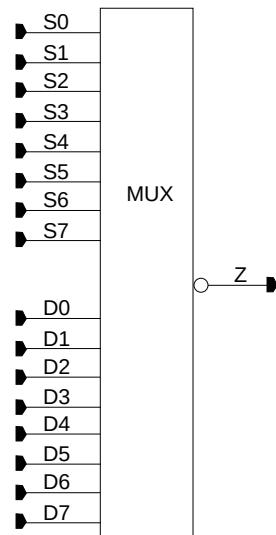
Description:

Eight-to-one inverting multiplexer. Specifically designed for use in data path structures. Select lines (S0 - S7) must all be driven from outputs (Z0 - Z7) of the same DEC38_DP.

S0 - S7 Select inputs

D0 - D7 Data inputs

Z Output



Truth Table

Inputs ¹									Output ²
S0	S1	S2	S3	S4	S5	S6	S7	Dx	Z
1	0	0	0	0	0	0	0	X	$\overline{D0}$
0	1	0	0	0	0	0	0	X	$\overline{D1}$
0	0	1	0	0	0	0	0	X	$\overline{D2}$
0	0	0	1	0	0	0	0	X	$\overline{D3}$
0	0	0	0	1	0	0	0	X	$\overline{D4}$
0	0	0	0	0	1	0	0	X	$\overline{D5}$
0	0	0	0	0	0	1	0	X	$\overline{D6}$
0	0	0	0	0	0	0	1	X	$\overline{D7}$

1. One and only one input can be selected at any given time. Having two or more, or none, selected is not allowed.
2. Output is the inversion of the data input.

Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
D0-Z	F	t _{PLH}	0.147 + 0.011N _{std}	0.105 + 0.008N _{std}	0.080 + 0.006N _{std}
		t _{PHL}	0.141 + 0.008N _{std}	0.093 + 0.005N _{std}	0.063 + 0.004N _{std}
D7-Z		t _{PLH}	0.148 + 0.011N _{std}	0.105 + 0.008N _{std}	0.081 + 0.006N _{std}
		t _{PHL}	0.142 + 0.008N _{std}	0.094 + 0.005N _{std}	0.064 + 0.004N _{std}
S0-Z		t _{PLH}	0.172 + 0.011N _{std}	0.115 + 0.008N _{std}	0.078 + 0.005N _{std}
		t _{PHL}	0.177 + 0.008N _{std}	0.119 + 0.005N _{std}	0.083 + 0.004N _{std}
S7-Z		t _{PLH}	0.172 + 0.011N _{std}	0.115 + 0.008N _{std}	0.078 + 0.005N _{std}
		t _{PHL}	0.177 + 0.008N _{std}	0.119 + 0.005N _{std}	0.083 + 0.004N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	F
D0	3.558
D1	3.554
D2	3.562
D3	3.554
D4	3.562
D5	3.554
D6	3.564
D7	3.566
S0	0.837
S1	0.848
S2	0.793
S3	0.788
S4	0.782



Capacitance (in units of N_{std}) and Cell Sizes (Continued)

Input Pins	Performance Level
	F
S5	0.779
S6	0.775
S7	0.773
Internal	4.592
Cell Units	39 cells



Standard Cell Pseudocells

Cell: CG_AND

Function: Clock Gate, AND Pseudocell

Description:

This pseudocell implements an AND clock-gating function for edge-triggered designs. This cell is a placeholder. When clock splitter CLKSPC (or CLKSPC) is inserted, the signal attached to the GATE pin of this pseudocell will be connected to the EN pin of the splitter, and the pseudocell will be removed.

OSC Edge clock input

GATE Clock gate

Z Edge clock output



Truth Table

Inputs		Output
OSC	GATE	Z
X	0	0
0	X	0
1	1	1

Cell: CG_DELAY

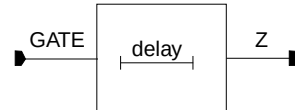
Function: Clock Gate, Delay Pseudocell

Boolean Expression: $Z = GATE$

Description:

In edge-triggered designs implementing register clock gating, this CG_DELAY_H pseudocell introduces a delay approximating that of a clock splitter. This cell is a placeholder to be placed in the path of the gating signal. When clock splitter CLKSPC_H (or CLKSPH_H) is inserted, this delay cell is removed.

GATE Clock gate input
Z Edge clock output



Cell: CG_OR

Function: Clock Gate, OR Pseudocell

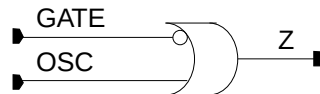
Description:

This pseudocell implements an OR clock-gating function for edge-triggered designs. This cell is a placeholder. When clock splitter CLKSPC (or CLKSPPL) is inserted, the signal attached to the GATE pin of this pseudocell will control the C pin of the splitter, and the pseudocell will be removed.

OSC Edge clock input

GATE Clock gate

Z Edge clock output



Truth Table

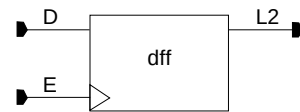
Inputs		Output
OSC	GATE	Z
X	0	1
0	1	0
1	X	1

Cell: D_LDE0001

Function: D-FF Pseudocell, +L2 Output

Description:

This is a standard positive edge-triggered D-FF. It is inferred by the synthesis tools and replaced by real technology cell LDE0001.



Truth Table

Inputs		Output
D	E	L2
X	R	D
X	F	NC

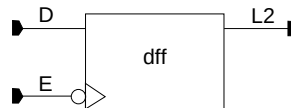
Cell: D_LDF0001

Function: Falling Edge Triggered D-FF Pseudocell, +L2 Output

Description:

This is a falling edge triggered D-FF. It is inferred by the synthesis tools and replaced by the real technology cell LDF0001.

D Data
E E clock (falling edge clock)
L2 L2 output (in phase with respect to input)



Truth Table

Inputs		Output
D	E	L2
X	R	NC
X	F	D

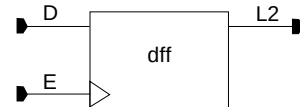
Cell: D_LDR0001

Function: Rising Edge Triggered D-FF Pseudocell, +L2 Output

Description:

This is a standard rising edge-triggered D-FF. It is inferred by the synthesis tools and replaced by the real technology cell LDR0001.

D Data
E E clock (rising edge clock)
L2 L2 output (in phase with respect to input)



Truth Table

Inputs		Output
D	E	L2
X	R	D
X	F	NC

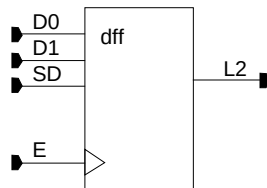
Cell: D_F_LMX0001

Function: D MUX Latch Pseudocell, +L2 Output

Description:

This is a standard positive edge-triggered D-FF. It is inferred by the synthesis tools and replaced by the F_LMX0001 cell.

- D0 Data in 0
- D1 Data in 1
- SD Data select
- E E clock (positive edge clock)
- L2 +L2 output (in phase with respect to input)



Truth Table

Inputs				Output
D0	D1	SD	E	L2
X	X	0	R	D0
X	X	1	R	D1
X	X	X	F	NC

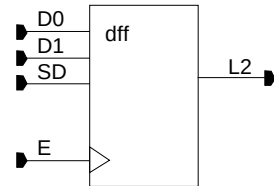
Cell: D_F_LMX0001_LPC

Function: D MUX Latch Pseudocell w/Enable, +L2 Output, Low Power

Description:

This is a low-power positive edge-triggered D-FF. It is inferred by the synthesis tools and replaced by the F_LMX0001_LPC cell.

D0 Data In 0
D1 Data In 1
SD Data select
E E clock (positive edge clock)
L2 +L2 output (in phase with respect to input)



Truth Table

Inputs				Output
D0	D1	SD	E	L2
X	X	0	R	D0
X	X	1	R	D1
X	X	X	F	NC

Cell: D_F_LPH0001

Function: D Latch Pseudocell, +L2 Output

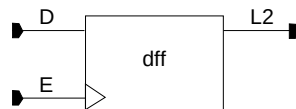
Description:

This is a standard positive edge-triggered D-FF. It is inferred by the synthesis tools and replaced by the F_LPH0001 cell.

D Data

E E clock (positive edge clock)

L2 +L2 output (in phase with respect to input)



Truth Table

Inputs		Output
D	E	L2
X	R	D
X	F	NC

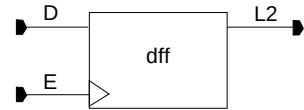
Cell: D_F_LPH0001_LPC

Function: D Latch Pseudocell, +L2 Output, Low Power

Description:

This is a low-power positive edge-triggered D-FF. It is inferred by the synthesis tools and replaced by the F_LPH0001_LPC cell.

D Data
E E clock (positive edge clock)
L2 +L2 output (in phase with respect to input)



Truth Table

Inputs		Output
D	E	L2
X	R	D
X	F	NC

Cell: D_F_LPH0002

Function: D Latch Pseudocell, -L2 Output

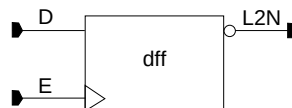
Description:

This is a standard positive edge-triggered D-FF. It is inferred by the synthesis tools and replaced by the F_LPH0002 cell.

D Data

E E clock (positive edge clock)

L2N -L2 output (out of phase with respect to input)



Truth Table

Inputs		Output
D	E	L2N
X	R	$\bar{D}$
X	F	NC

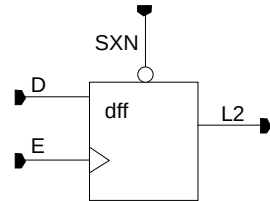
Cell: D_F_LPH2021_LPC

Function: D-FF Pseudocell, +L2 Output, -Asyn Set

Description:

This is a standard positive edge-triggered D-FF. It is inferred by the synthesis tools. When replaced by the F_LPH1001_LPC cell, additional gates are added to preserve the asynchronous set function.

D Data
E E clock (positive edge clock)
L2 +L2 output (in phase with respect to input)
SXN Direct set (negative active)



Truth Table

Inputs			Output
D	E	SXN	L2
X	R	1	D
X	F	1	NC
X	X	0	1

Cell: D_F_LPH4041_LPC

Function: D Latch Pseudocell, +L2 Output, -Asyn Reset

Description:

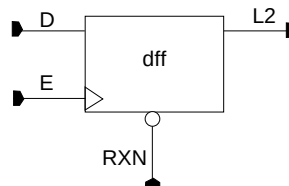
This is a standard positive edge-triggered D-FF. It is inferred by the synthesis tools. When replaced by the F_LPH4001_LPC cell, additional gates are added to preserve the asynchronous reset function.

D Data

E E clock (positive edge clock)

L2 +L2 output (in phase with respect to input)

RXN Direct reset (negative active)



Truth Table

Inputs			Output
D	E	RXN	L2
X	R	1	D
X	F	1	NC
X	X	0	0

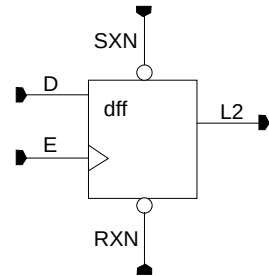
Cell: D_F_LPH8081

Function: D-FF Pseudocell, +L2 Output, -Asyn Set, -Asyn Reset

Description:

This is a standard positive edge-triggered D-FF. It is inferred by the synthesis tools. When replaced by the F_LPH6001 cell, additional gates are added to preserve the asynchronous set and reset functions.

D Data
E E clock (positive edge clock)
L2 +L2 output (in phase with respect to input)
RXN Direct reset (negative active)
SXN Direct set (negative active)



Truth Table

Inputs				Output
D	E	RXN	SXN	L2
X	R	1	1	D
X	F	1	1	NC
X	X	X	0	1
X	X	0	1	0

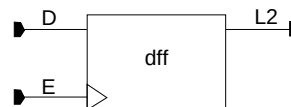
Cell: D_F_MPH0001_LPC

Function: D-FF Pseudocell, +L2 Output, Low Power

Description:

This is a standard positive edge-triggered D-FF. It is inferred by the synthesis tools and replaced by the F_MPH0001_LPC cell.

D Data
E Positive edge clock
L2 +L2 output



Truth Table

Inputs		Output
D	E	L2
X	R	D
X	F	NC

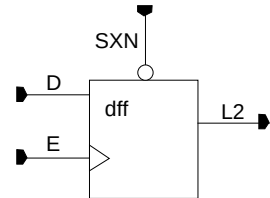
Cell: D_F_MPH2021_LPC

Function: D-FF Pseudocell, +L2 Output, -Asyn Set

Description:

This is a standard positive edge-triggered D-FF. It is inferred by the synthesis tools. When replaced by the F_MPH1001_LPC cell, additional gates are added to preserve the asynchronous set function.

- D Data
- E E clock (positive edge clock)
- L2 +L2 output (in phase with respect to input)
- SXN Direct set (negative active)



Truth Table

Inputs			Output
D	E	SXN	L2
X	R	1	D
X	F	1	NC
X	X	0	1

Cell: D_F_MPH4041_LPC

Function: D Latch Pseudocell, +L2 Output, -Asyn Reset

Description:

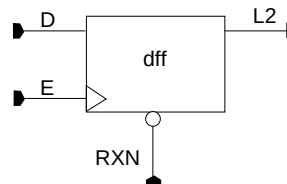
This is a standard positive edge-triggered D-FF. It is inferred by the synthesis tools. When replaced by the F_MPH4001_LPC cell, additional gates are added to preserve the asynchronous reset function.

D Data

E E clock (positive edge clock)

L2 +L2 output (in phase with respect to input)

RXN Direct reset (negative active)



Truth Table

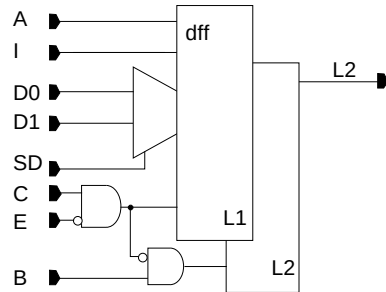
Inputs			Output
D	E	RXN	L2
X	R	1	D
X	F	1	NC
X	X	0	0

Cell: F_LMX0001

Function: D MUX Latch Pseudocell w/Enable, +L2 Output

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the proper C and B clocks for L1 and L2, respectively. The B and C inputs must be held high during normal system operation. This cell is replaced by real technology cell LMX0001 and shared clock splitters.



A	A clock
B	B clock
C	C clock
D0	Data-in 0
D1	Data-in 1
SD	Data select
I	Scan-in
E	Clock in
L2	+L2 output (in phase with input)

D-FF Operation

Inputs								Output
SD	A	I	C	E	D0	D1	B	L2
0	0	X	1	R	X	X	1	D0
1	0	X	1	R	X	X	1	D1
X	0	X	1	F	X	X	1	NC

LSSD Latch L1 Truth Table

Inputs							L1 State
SD	A	I	C	E	D0	D1	
X	0	X	0	X	X	X	NC
X	1	X	0	X	X	X	I
0	0	X	1	0	X	X	D0
1	0	X	1	0	X	X	D1
X	0	X	X	1	X	X	NC



LSSD Latch L2 Truth Table

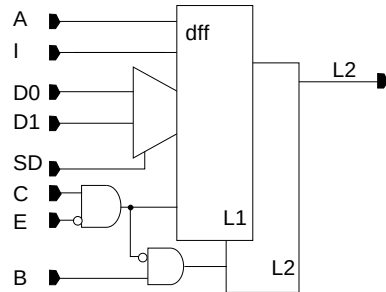
Inputs			Output
E	B	C	L2
X	0	X	NC
0	1	1	NC
X	1	0	L1
1	1	X	L1

Cell: F_LMX0001_LPC

Function: D MUX Latch Pseudocell w/Enable, +L2 Output, Low Power

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the proper C and B clocks for L1 and L2, respectively. The B and C inputs must be held high during normal system operation. This cell is replaced by real technology cell LMX0001_LPC and shared clock splitters.



A	A clock
B	B clock
C	C clock
D0	Data-in 0
D1	Data-in 1
SD	Data select
I	Scan-in
E	Clock in
L2	+L2 output (in phase with input)

D-FF Operation

Inputs								Output
SD	A	I	C	E	D0	D1	B	L2
0	0	X	1	R	X	X	1	D0
1	0	X	1	R	X	X	1	D1
X	0	X	1	F	X	X	1	NC

LSSD Latch L1 Truth Table

Inputs							L1 State
SD	A	I	C	E	D0	D1	
X	0	X	0	X	X	X	NC
X	1	X	0	X	X	X	I
0	0	X	1	0	X	X	D0
1	0	X	1	0	X	X	D1
X	0	X	X	1	X	X	NC



LSSD Latch L2 Truth Table

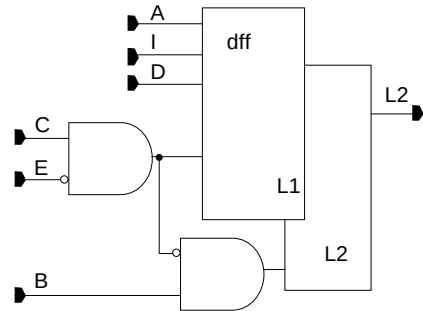
Inputs			Output
E	B	C	L2
X	0	X	NC
0	1	1	NC
X	1	0	L1
1	1	X	L1

Cell: F_LPH0001

Function: D Latch Pseudocell, +L2 Output

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the proper C and B clocks for L1 and L2, respectively. The B and C inputs must be held high during normal system operation. This cell is replaced by real technology cell LPH0001 and shared clock splitters.



A	A clock
B	B clock
C	C clock
D	Data
E	E clock
I	Scan-in
L2	+L2 output (in phase with respect to input)

D-FF Operation

Input						Output
A	I	C	E	D	B	L2
0	X	1	R	X	1	D
0	X	1	F	X	1	NC

LSSD Latch L1 Truth Table

Inputs					L1 State
A	I	C	E	D	
0	X	0	X	X	NC
1	X	0	X	X	I
0	X	1	0	X	D
0	X	1	1	X	NC



LSSD Latch L2 Truth Table

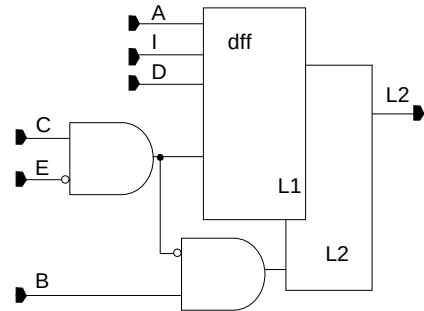
Inputs			Output
E	B	C	L2
X	0	X	NC
0	1	1	NC
X	1	0	L1
1	1	X	L1

Cell: F_LPH0001_LPC

Function: D Latch Pseudocell, +L2 Output, Low Power

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the proper C and B clocks for L1 and L2, respectively. The B and C inputs must be held high during normal system operation. This cell is replaced by real technology cell LPH0001_LPC and shared clock splitters.



- A A clock
- B B clock
- C C clock
- D Data
- E E clock
- I Scan-in
- L2 +L2 output (in phase with respect to input)

D-FF Operation

Input						Output
A	I	C	E	D	B	L2
0	X	1	R	X	1	D
0	X	1	F	X	1	NC

LSSD Latch L1 Truth Table

Inputs					L1 State
A	I	C	E	D	
0	X	0	X	X	NC
1	X	0	X	X	I
0	X	1	0	X	D
0	X	1	1	X	NC



LSSD Latch L2 Truth Table

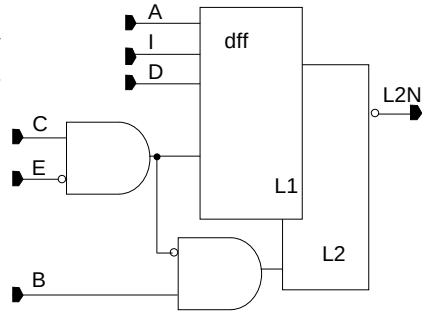
Inputs			Output
E	B	C	L2
X	0	X	NC
0	1	1	NC
X	1	0	L1
1	1	X	L1

Cell: F_LPH0002

Function: D Latch Pseudocell, -L2 Output

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the proper C and B clocks for L1 and L2, respectively. The B and C inputs must be held high during normal system operation. This cell is replaced by real technology cell LPH0002 and shared clock splitters.



A A clock
B B clock
C C clock
D Data
E E clock
I Scan-in
L2N -L2 output (out of phase with respect to input)

D-FF Operation

Input						Output
A	I	C	E	D	B	L2N
0	X	1	R	X	1	$\bar{D}$
0	X	1	F	X	1	NC

LSSD Latch L1 Truth Table

Inputs					L1 State
A	I	C	E	D	
0	X	0	X	X	NC
1	X	0	X	X	I
0	X	1	0	X	D
0	X	1	1	X	NC



LSSD Latch L2 Truth Table

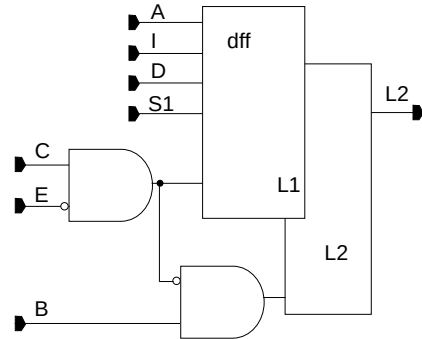
Inputs			Output
E	B	C	L2N
X	0	X	NC
0	1	1	NC
X	1	0	$\overline{L1}$
1	1	X	$\overline{L1}$

Cell: F_LPH1001_LPC

Function: D Latch Pseudocell, +L2 Output, +Asyn Set L1, Low Power

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the proper C and B clocks for L1 and L2, respectively. The B and C inputs must be held high during normal system operation. For asynchronous set operation, the C and S1 inputs must be forced to 0 and 1, respectively. (See D_F_LPH2021_LPC.) This cell is replaced by real technology cell LPH1001_LPC and shared clock splitters.



- A A clock
- B B clock
- C C clock
- D Data
- E E clock
- I Scan-in
- S1 Direct reset (positive active)
- L2 +L2 output (in phase with respect to input)

D-FF Operation

Inputs							Output
S1	A	I	C	E	D	B	L2
0	0	X	1	R	X	1	D
0	0	X	1	1, F, 0	X	1	NC
1	X	X	0	X	X	1	1
1	X	X	X	1	X	1	1
1	X	X	1	0	X	1	NC
other input conditions							X



LSSD Latch L1 Truth Table

Inputs						L1 State
S1	A	I	C	E	D	
0	0	X	0	X	X	NC
1	X	X	X	X	X	1
0	1	X	0	X	X	I
0	0	X	1	0	X	D
0	0	X	X	1	X	NC

LSSD Latch L2 Truth Table

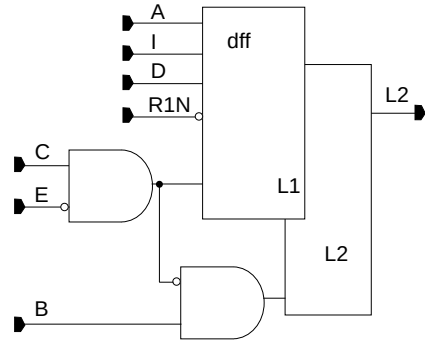
Inputs			Output
E	C	B	L2
X	X	0	NC
0	1	1	NC
X	0	1	L1
1	X	1	L1

Cell: F_LPH4001_LPC

Function: D Latch Pseudocell, +L2 Output, -Asyn Reset L1, Low Power

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the proper C and B clocks for L1 and L2, respectively. The B and C inputs must be held high during normal system operation. For asynchronous reset operation, the C and R1N inputs must both be forced to 0. (See D_F_LPH4041_LPC.) This cell is replaced by real technology cell LPH4001_LPC and shared clock splitters.



- A A clock
- B B clock
- C C clock
- D Data
- E E clock
- I Scan-in
- R1N Direct reset (negative active)
- L2 +L2 output (in phase with respect to input)

D-FF Operation

Inputs							Output
R1N	A	I	C	E	D	B	L2
1	0	X	1	R	X	1	D
1	0	X	1	1, F, 0	X	1	NC
0	X	X	0	X	X	1	0
0	X	X	X	1	X	1	0
0	X	X	1	0	X	1	NC
other input conditions							X



LSSD Latch L1 Truth Table

Inputs						L1 State
R1N	A	I	C	E	D	
1	0	X	0	X	X	NC
0	X	X	X	X	X	0
1	1	X	0	X	X	I
1	0	X	1	0	X	D
1	0	X	X	1	X	NC

LSSD Latch L2 Truth Table

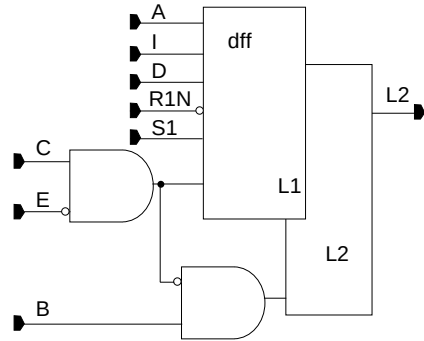
Inputs			Output
E	C	B	L2
X	X	0	NC
0	1	1	NC
X	0	1	L1
1	X	1	L1

Cell: F_LPH6001

Function: D Latch Pseudocell, +L2 Output, -Asyn Reset L1, +Asyn Set L1

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the proper C and B clocks for L1 and L2, respectively. The B and C inputs must be held high during normal system operation. For asynchronous set or reset operation, the C input must be forced to 0 while the S1 or R1N input is activated. (See D_F_LPH8081.) This cell is replaced by real technology cell LPH6001 and shared clock splitters.



- A A clock
- B B clock
- C C clock
- D Data
- E E clock
- I Scan-in
- R1N Direct reset (negative active)
- S1 Direct set (positive active)
- L2 +L2 output (in phase with respect to input)

D-FF Operation

Inputs								Output
S1	R1N	A	I	C	E	D	B	L2
0	1	0	X	1	R	X	1	D
0	1	0	X	1	1, F, 0	X	1	NC
0	0	X	X	0	X	X	1	0
0	0	X	X	X	1	X	1	0
1	X	X	X	0	X	X	1	1
1	X	X	X	X	1	X	1	1
0	0	X	X	1	0	X	1	NC
1	X	X	X	1	0	X	1	NC
other input conditions								X



LSSD Latch L1 Truth Table

Inputs							L1 State
R1N	S1	A	I	C	E	D	
1	0	0	X	0	X	X	NC
X	1	X	X	X	X	X	1
0	0	X	X	X	X	X	0
1	0	1	X	0	X	X	I
1	0	0	X	1	0	X	D
1	0	0	X	X	1	X	NC

LSSD Latch L2 Truth Table

Inputs			Output
E	C	B	L2
X	X	0	NC
0	1	1	NC
X	0	1	L1
1	X	1	L1

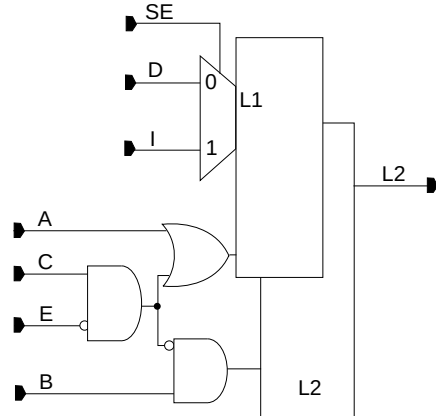
Cell: F_MPH0001_LPC

Function: LSSD MUX-Scan D-FF Pseudocell, +L2 Output, Low Power

Description:

This is a positive edge-triggered D-FF that contains a scan path multiplexer and a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the clocks for the internal L1 and L2 level-sensitive latches. For normal D-FF operation, inputs B and C must be held high and input A must be held low. Input SE controls whether scan data (I) or system data (D) is captured. This cell gets replaced by real technology cell MPH0001_LPC and shared clock splitter CLKSP1.

A	A clock
B	B clock
C	C clock
D	Data input
E	Positive edge clock
SE	Scan enable
I	Scan data input
L2	+L2 output



D-FF Operation

Inputs							Output
A	I	C	E	D	B	SE	L2
0	X	1	R	X	1	0	D
0	X	1	R	X	1	1	I
0	X	1	F	X	1	X	NC

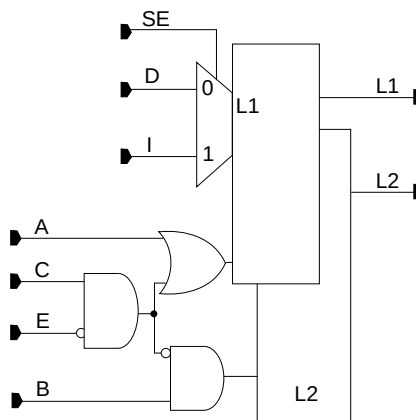
Cell: F_MPH0101_LPC

Function: LSSD MUX-Scan D-FF Pseudocell, +L1, +L2 Output, Low Power

Description:

This is a positive edge-triggered D-FF that contains a scan path multiplexer and a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the clocks for the internal L1 and L2 level-sensitive latches. For normal D-FF operation, inputs B and C must be held high and input A must be held low. Input SE controls whether scan data (I) or system data (D) is captured. This cell gets replaced by real technology cell MPH0101_LPC and shared clock splitter CLKSP1.

- A A clock
- B B clock
- C C clock
- D Data input
- E Positive edge clock
- SE Scan enable
- I Scan data input
- L1 +L1 output
- L2 +L2 output



D-FF Operation

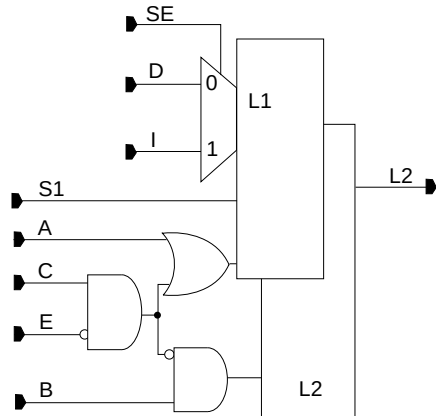
Inputs							Output
A	I	C	E	D	B	SE	L2
0	X	1	R	X	1	0	D
0	X	1	R	X	1	1	I
0	X	1	F	X	1	X	NC

Cell: F_MPH1001_LPC

Function: LSSD MUX-Scan D-FF Pseudocell, +L2 Output, +Asyn Set L1

Description:

This is a positive edge-triggered D-FF that contains a scan path multiplexer and a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the clocks for the internal L1 and L2 level-sensitive latches. For normal D-FF operation, inputs B and C must be held high and input A must be held low. Input SE controls whether scan data (I) or system data (D) is captured. For asynchronous set operation, the C and S1 inputs must be forced to 0 and 1, respectively. (See D_F_MPH2021_LPC.) This cell gets replaced by real technology cell MPH1001_LPC and shared clock splitter CLKSPL.



- A A clock
- B B clock
- C C clock
- D Data input
- E Positive edge clock
- SE Scan enable
- I Scan data input
- L2 +L2 output
- S1 Direct L1 set (positive active)

D-FF Operation

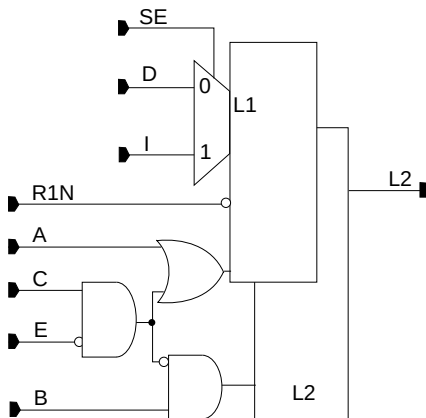
Inputs								Output
S1	A	I	C	E	D	B	SE	L2
0	0	X	1	R	X	1	0	D
0	0	X	1	R	X	1	1	I
0	0	X	1	1, F, 0	X	1	X	NC
1	X	X	0	X	X	1	X	1
1	X	X	X	1	X	1	X	1
1	X	X	1	0	X	1	X	NC
other input conditions								X

Cell: F_MPH4001_LPC

Function: LSSD MUX-Scan D-FF Pseudocell, +L2 Output, +Asyn Reset L1

Description:

This is a positive edge-triggered D-FF that contains a scan path multiplexer and a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the clocks for the internal L1 and L2 level-sensitive latches. For normal D-FF operation, inputs B and C must be held high and input A must be held low. Input SE controls whether scan data (I) or system data (D) is captured. For asynchronous reset operation, the C and R1N inputs must both be forced to 0. (See D_F_MPH4041_LPC.) This cell gets replaced by real technology cell MPH4001_LPC and shared clock splitter CLKSP1.



- A A clock
- B B clock
- C C clock
- D Data input
- E Positive edge clock
- SE Scan enable
- I Scan data input
- L2 +L2 output
- R1N Direct L1 reset (negative active)

D-FF Operation

Inputs								Output
R1N	A	I	C	E	D	B	SE	L2
1	0	X	1	R	X	1	0	D
1	0	X	1	R	X	1	1	I
1	0	X	1	1, F, 0	X	1	X	NC
0	X	X	0	X	X	1	X	0
0	X	X	X	1	X	1	X	0
0	X	X	1	0	X	1	X	NC
other input conditions								X

Cell: L_LTL0001

Function: Transparent Latch Pseudocell, +L2 Output

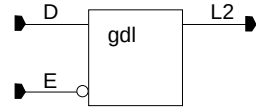
Description:

This is a level-sensitive transparent latch. It is inferred by the synthesis tools and replaced with real technology cell LTL0001.

E E clock (negative active)

D Data

L2 +L2 output (positive with respect to D)



Truth Table

Inputs		Output
E	D	L2
0	X	D
1	X	NC

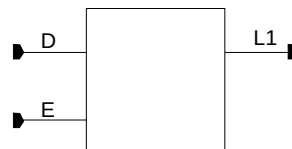
Cell: L_MPH0101_LPC

Function: Transparent Latch Pseudocell, +L1 Output

Description:

This is a level-sensitive transparent latch. It is inferred by the synthesis tools and replaced with real technology cell MPH0101_LPC and CLKSP.L.

E C clock
D Data
L1 +L1 output (positive with respect to D)



Truth Table

Inputs		Output
E	D	L1
0	X	D
1	X	NC

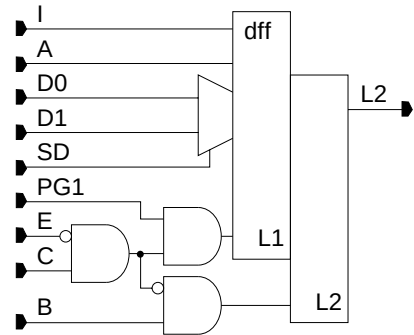
Cell: PG_LMX0001

Function: D MUX Latch Pseudocell, L1 Clock Gate, +L2 Output

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the true and complement clocks for L2 and L1, respectively. The B, C, and PG1 inputs must be held high during normal system operation. This cell is replaced by real technology cell LMX0001 and shared clock splitter CLKSPC.

- A A clock
- B B clock
- C C clock
- PG1 L1 clock gate
- D0 Data-in 0
- D1 Data-in 1
- SD Data select
- I Scan-in
- E Clock in
- L2 +L2 output (in phase with input)



D-FF Operation

Inputs									Output
SD	A	I	PG1	C	E	D0	D1	B	L2
0	0	X	1	1	R	X	X	1	D0
1	0	X	1	1	R	X	X	1	D1
X	0	X	1	1	F	X	X	1	NC



LSSD Latch L1 Truth Table

Inputs								L1 State
SD	A	I	PG1	C	E	D0	D1	
X	0	X	X	0	X	X	X	NC
X	1	X	X	0	X	X	X	I
0	0	X	1	1	0	X	X	D0
1	0	X	1	1	0	X	X	D1
X	0	X	0	1	0	X	X	NC
X	0	X	X	X	1	X	X	NC

LSSD Latch L2 Truth Table

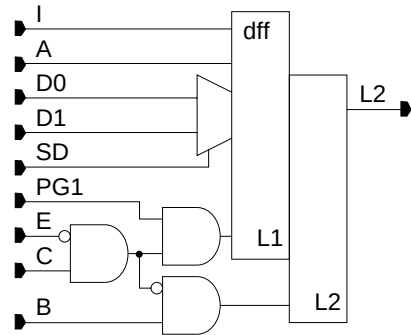
Inputs			Output	
E	B	C	L2	
X	0	X	NC	
0	1	1	NC	
X	1	0	L1	
1	1	X	L1	

Cell: PG_LMX0001_LPC

Function: D MUX Latch Pseudocell, L1 Clock Gate, +L2 Output

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the true and complement clocks for L2 and L1, respectively. The B, C, and PG1 inputs must be held high during normal system operation. This cell is replaced by real technology cell LMX0001_LPC and shared clock splitter CLKSPC.



A	A clock
B	B clock
C	C clock
PG1	L1 clock gate
D0	Data-in 0
D1	Data-in 1
SD	Data select
I	Scan-in
E	Clock in
L2	+L2 output (in phase with input)

D-FF Operation

Inputs									Output
SD	A	I	PG1	C	E	D0	D1	B	L2
0	0	X	1	1	R	X	X	1	D0
1	0	X	1	1	R	X	X	1	D1
X	0	X	1	1	F	X	X	1	NC



LSSD Latch L1 Truth Table

Inputs								L1 State
SD	A	I	PG1	C	E	D0	D1	
X	0	X	X	0	X	X	X	NC
X	1	X	X	0	X	X	X	I
0	0	X	1	1	0	X	X	D0
1	0	X	1	1	0	X	X	D1
X	0	X	0	1	0	X	X	NC
X	0	X	X	X	1	X	X	NC

LSSD Latch L2 Truth Table

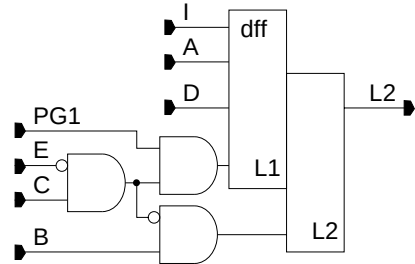
Inputs			Output
E	B	C	
X	0	X	NC
0	1	1	NC
X	1	0	L1
1	1	X	L1

Cell: PG_LPH0001

Function: D Latch Pseudocell, L1 Clock Gate, +L2 Output

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the true and complement clocks for L2 and L1, respectively. The B, C, and PG1 inputs must be held high during normal system operation. This cell is replaced by real technology cell LPH0001 and shared clock splitter CLKSPC.



A	A clock
B	B clock
C	C clock
PG1	L1 clock gate
D	Data
E	E clock
I	Scan-in
L2	+L2 output (in phase with respect to input)

D-FF Operation

Input							Output
A	I	PG1	C	E	D	B	L2
0	X	1	1	R	X	1	D
0	X	1	1	F	X	1	NC

LSSD Latch L1 Truth Table

Inputs						L1 State
A	I	PG1	C	E	D	
0	X	X	0	X	X	NC
1	X	X	0	X	X	I
0	X	1	1	0	X	D
0	X	0	1	0	X	NC
0	X	X	1	1	X	NC



LSSD Latch L2 Truth Table

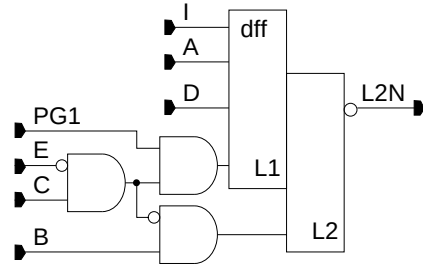
Inputs			Output
E	B	C	L2
X	0	X	NC
0	1	1	NC
X	1	0	L1
1	1	X	L1

Cell: PG_LPH0002

Function: D Latch Pseudocell, L1 Clock Gate, L2N Output

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the true and complement clocks for L2 and L1, respectively. The B, C, and PG1 inputs must be held high during normal system operation. This cell is replaced by real technology cell LPH0002 and shared clock splitter CLKSPC.



A A clock

B B clock

C C clock

PG1 L1 clock gate

D Data

E E clock

I Scan-in

L2N L2N output (out of phase with respect to input)

D-FF Operation

Input							Output
A	I	PG1	C	E	D	B	L2N
0	X	1	1	R	X	1	$\bar{D}$
0	X	1	1	F	X	1	NC

LSSD Latch L1 Truth Table

Inputs						L1 State
A	I	PG1	C	E	D	
0	X	X	0	X	X	NC
1	X	X	0	X	X	I
0	X	1	1	0	X	D
0	X	0	1	0	X	NC
0	X	X	1	1	X	NC



LSSD Latch L2 Truth Table

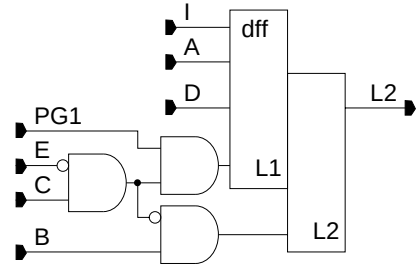
Inputs			Output
E	B	C	L2N
X	0	X	NC
0	1	1	NC
X	1	0	$\overline{L1}$
1	1	X	$\overline{L1}$

Cell: PG_LPH0001_LPC

Function: D Latch Pseudocell, L1 Clock Gate, +L2 Output

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the true and complement clocks for L2 and L1, respectively. The B, C, and PG1 inputs must be held high during normal system operation. This cell is replaced by real technology cell LPH0001_LPC and shared clock splitter CLKSPC.



A	A clock
B	B clock
C	C clock
PG1	L1 clock gate
D	Data
E	E clock
I	Scan-in
L2	+L2 output (in phase with respect to input)

D-FF Operation

Input							Output
A	I	PG1	C	E	D	B	L2
0	X	1	1	R	X	1	D
0	X	1	1	F	X	1	NC

LSSD Latch L1 Truth Table

Inputs						L1 State
A	I	PG1	C	E	D	
0	X	X	0	X	X	NC
1	X	X	0	X	X	I
0	X	1	1	0	X	D
0	X	0	1	0	X	NC
0	X	X	1	1	X	NC



LSSD Latch L2 Truth Table

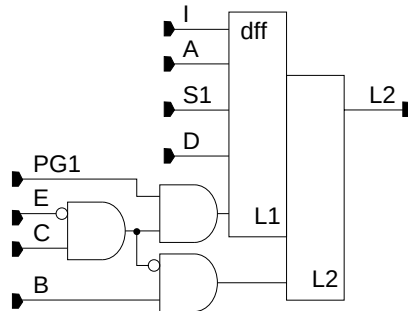
Inputs			Output
E	B	C	L2
X	0	X	NC
0	1	1	NC
X	1	0	L1
1	1	X	L1

Cell: PG_LPH1001_LPC

Function: D Latch Pseudocell, L1 Clock Gate, +L2 Output, +Asyn Set L1

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the true and complement clocks for L2 and L1, respectively. The B, C, and PG1 inputs must be held high during normal system operation. This cell is replaced by real technology cell LPH1001_LPC and shared clock splitter CLKSPC.



- A A clock
- B B clock
- C C clock
- PG1 L1 clock gate
- D Data
- E E clock
- I Scan-in
- S1 Direct reset (positive active)
- L2 +L2 output (in phase with respect to input)

D-FF Operation

Inputs								Output
S1	A	I	PG1	C	E	D	B	L2
1	X	X	X	X	X	X	X	1
0	0	X	1	1	R	X	1	D
0	0	X	1	1	F	X	1	NC



LSSD Latch L1 Truth Table

Inputs							L1 State
S1	A	I	PG1	C	E	D	
0	0	X	X	0	X	X	NC
1	X	X	X	X	X	X	1
0	1	X	X	0	X	X	I
0	0	X	1	1	0	X	D
0	0	X	0	1	0	X	NC
0	0	X	X	X	1	X	NC

LSSD Latch L2 Truth Table

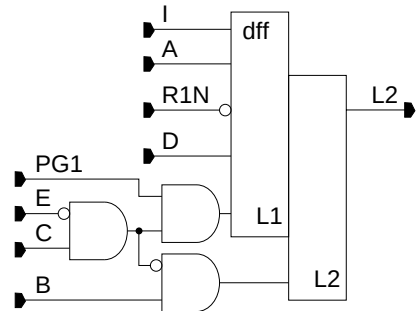
Inputs			Output
E	C	B	L2
X	X	0	NC
0	1	1	NC
X	0	1	L1
1	X	1	L1

Cell: PG_LPH4001_LPC

Function: D Latch Pseudocell, L1 Clock Gate, +L2 Output, -Asyn Reset L1

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the true and complement clocks for L2 and L1, respectively. The B, C, and PG1 inputs must be held high during normal system operation. This cell is replaced by real technology cell LPH4001_LPC and shared clock splitter CLKSPC.



- A A clock
- B B clock
- C C clock
- PG1 L1 clock gate
- D Data
- E E clock
- I Scan-in
- R1N Direct reset (negative active)
- L2 +L2 output (in phase with respect to input)

D-FF Operation

Inputs								Output
R1N	A	I	PG1	C	E	D	B	L2
0	X	X	X	X	X	X	X	0
1	0	X	1	1	R	X	1	D
1	0	X	1	1	F	X	1	NC



LSSD Latch L1 Truth Table

Inputs							L1 State
R1N	A	I	PG1	C	E	D	
1	0	X	X	0	X	X	NC
0	X	X	X	X	X	X	0
1	1	X	X	0	X	X	I
1	0	X	1	1	0	X	D
1	0	X	0	1	0	X	NC
1	0	X	X	X	1	X	NC

LSSD Latch L2 Truth Table

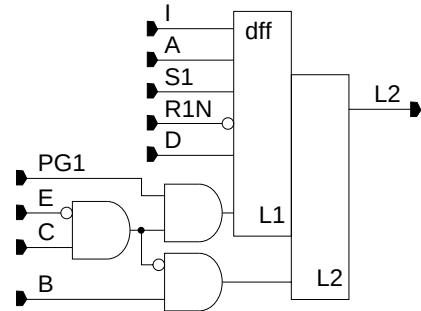
Inputs			Output
E	C	B	
X	X	0	NC
0	1	1	NC
X	0	1	L1
1	X	1	L1

Cell: PG_LPH6001

Function: D Latch Pseudocell, L1 Clock Gate, +L2 Output, -Asyn Reset L1/+Asyn Set L1

Description:

This is a positive edge-triggered D-FF that contains a clock splitter. The E clock (positive edge clock) is the input to the built-in clock splitter that generates the true and complement clocks for L2 and L1, respectively. The B, C, and PG1 inputs must be held high during normal system operation. This cell is replaced by real technology cell LPH6001 and shared clock splitter CLKSPC.



A	A clock
B	B clock
C	C clock
PG1	L1 clock gate
D	Data
E	E clock
I	Scan-in
R1N	Direct reset (negative active)
S1	Direct set (positive active)
L2	+L2 output (in phase with respect to input)

D-FF Operation

Inputs									Output
R1N	S1	A	I	PG1	C	E	D	B	L2
X	1	X	X	X	X	X	X	X	1
0	0	X	X	X	X	X	X	X	0
1	0	0	X	1	1	R	X	1	D
1	0	0	X	1	1	F	X	1	NC



LSSD Latch L1 Truth Table

Inputs								L1 State
R1N	S1	A	I	PG1	C	E	D	
1	0	0	X	X	0	X	X	NC
X	1	X	X	X	X	X	X	1
0	0	X	X	X	X	X	X	0
1	0	1	X	X	0	X	X	I
1	0	0	X	1	1	0	X	D
1	0	0	X	0	X	X	X	NC
1	0	0	X	X	X	1	X	NC

LSSD Latch L2 Truth Table

Inputs			Output
E	C	B	L2
X	X	0	NC
0	1	1	NC
X	0	1	L1
1	X	1	L1

Cell: TW_ONE_A

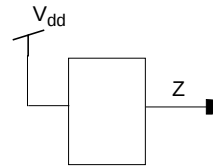
Function: Placeholder, Hold Test Wrapper Signal to 1

Boolean Expression: $Z = 1$

Description:

This pseudocell is instantiated in test wrappers for RAMs, RAs, ROMs and/or cores as a placeholder source for a test signal that needs to be held high for normal operation. Front-end processing software will replace this pseudocell with the real source of the test signal, specified by switchbox connection.

Z Output tied high



Cell: TW_ZERO_A

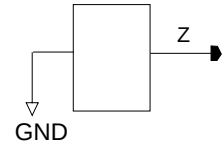
Function: Placeholder, Hold Test Wrapper Signal to 0

Boolean Expression: $Z = 0$

Description:

This pseudocell is instantiated in test wrappers for RAMs, RAs, ROMs and/or cores as a placeholder source for a test signal that needs to be held low for normal operation. Front-end processing software will replace this pseudocell with the real source of the test signal, specified by switchbox connection.

Z Output tied low





Standard Cell Nontest I/O

Refer to "DC or Limited-Function Test I/Os" on page 90 for more information on using DC test I/Os.

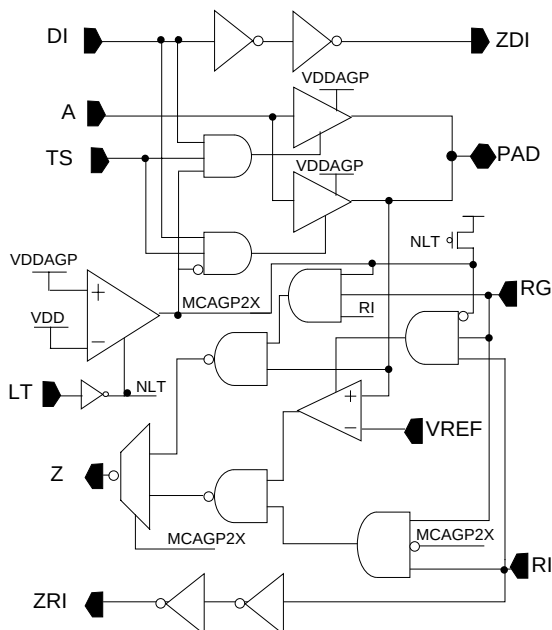
Cell: BAGP2X4X, BAGP2X4X_PM

Function: AGP 2X/4X Dual Mode Nontest CIO

Description:

Noninverting three-state driver/receiver for 3.3V AGP (accelerated graphics port) 2X operation or 1.5V 4X operation. This I/O requires two power supplies: V_{dd} and V_{DAGP} . The voltage on the second power supply (V_{DAGP}) determines the I/O's mode of operation. These are bidirectional I/Os. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} . The 4X receiver requires an (off-chip) input reference (0.75V).

A	Driver data input
TS	Driver three-state control
LT	DC current gate (I_{dd} test) input
DI	Driver inhibit input (DI in)
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
PAD	Driver output/receiver input
VREF	Voltage reference input
Z	Receiver output
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A ¹	DI

1. If $VDDAGP = 1.5V \pm 0.1V$, the driver operates in AGP4X mode. Output logical "1" = $VDDAGP = 1.5V$. If $VDDAGP = 3.3V \pm 0.3V$, the driver operates in AGP2X mode. Output logical "1" = $VDDAGP = 3.3V$.
2. During I_{ddq} test, when $LT="1"$, the I/O will be forced to 2X operation and $VDDAGP$ must be set to 3.3V.

2x/4X Receiver Truth Table

Inputs					Outputs		Comments
PAD	RI	RG	LT	VREF ¹	Z	ZRI	
_ ²	1	1	1 ²	-	PAD	RI	Test mode
-	0	-	-	-	0	RI	Test mode
-	-	0	-	-	0	RI	Test mode/functional mode
0 ³	1	1	0	-	0	RI	Functional mode
1 ²	1	1	0	-	1	RI	Functional mode
Hi-Z	1	1	0	-	X	RI	

1. A reference voltage of $VDDAGP/2$ is required for AGP4X operation.
2. During I_{ddq} test, when $LT="1"$, the I/O is forced to 2X operation and $VDDAGP$ must be set to 3.3V.
3. Receiver mode is selected by the voltage on $VDDAGP$. If $VDDAGP = 1.5 \pm 0.1V$, the receiver operates in AGP4X mode. If $VDDAGP = 3.3 \pm 0.3V$, the receiver operates in AGP2X mode. The PAD input requires signaling level "1", which corresponds to the I/O's current mode of operation. AGP2X mode requires $3.3V \pm 0.3V$. AGP4X mode requires $1.5V \pm 0.1V$. Both modes require 0V for "low" signaling.



AGP 4X Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V VDDAGP = 1.4V T _j = 125°C Process = Slow	V _{dd} = 1.8V VDDAGP = 1.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V VDDAGP = 1.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	0.756 + 0.035D _{std}	0.472 + 0.027D _{std}	0.306 + 0.021D _{std}
		t _{PHL}	0.960 + 0.038D _{std}	0.609 + 0.028D _{std}	0.436 + 0.022D _{std}

AGP 2X Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V VDDAGP = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V VDDAGP = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V VDDAGP = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	2.151 + 0.044D _{std}	1.356 + 0.032D _{std}	0.980 + 0.025D _{std}
		t _{PHL}	2.154 + 0.052D _{std}	1.449 + 0.034D _{std}	1.042 + 0.027D _{std}

AGP 4X Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V VDDAGP = 1.4V T _j = 125°C Process = Slow	V _{dd} = 1.8V VDDAGP = 1.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V VDDAGP = 1.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	1.018 + 0.003N _{std}	0.477 + 0.001N _{std}	0.296 + 0.001N _{std}
		t _{PHL}	0.861 + 0.003N _{std}	0.600 + 0.002N _{std}	0.440 + 0.001N _{std}

AGP 2X Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V VDDAGP = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V VDDAGP = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V VDDAGP = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.620 + 0.002N _{std}	0.433 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.534 + 0.002N _{std}	0.394 + 0.001N _{std}	0.318 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	23.683
DI	12.461
LT	11.336
PAD (Receiver Input)	666.167
RG	9.721
RI	10.426
TS	7.981
VREF	115.883
Internal	720.00
Cell Units	2 cells

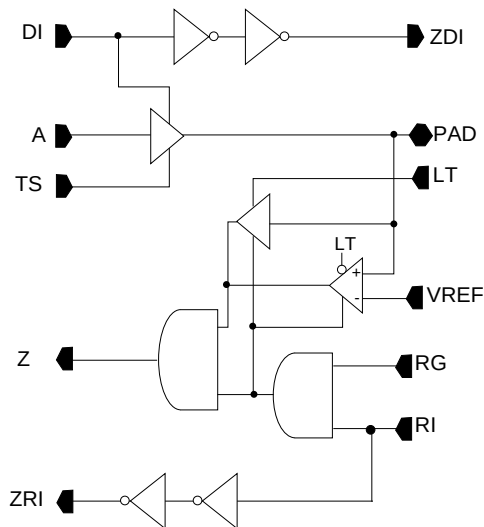
Cell: BAGP4X, BAGP4X_PM

Function: 1.5V AGP 4X Nontest 3-State CIO

Description:

Noninverting three-state driver/receiver for 1.5V AGP (accelerated graphics port) 4X interface. This is a bidirectional I/O. A, TS, RG, and Z must have a boundary-scan structure. If RG is not used it should be tied to V_{dd} . Output di/dt and performance are chosen by performance level selection. Receiver requires (off-chip) input reference ($V_{ddq}/2$).

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- LT DC current gate (I_{dd} test) input
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- VREF Voltage reference input
- PAD Driver output/receiver input
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)
- Z Receiver output



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	0	-	Hi-Z	DI
-	-	0	Hi-Z	DI
1	1	1	1 ¹	DI
0	1	1	0	DI

¹. Logical "1" = $V_{ddq} = V_{dd150} = 1.5V$.

Receiver Truth Table

Inputs					Outputs	
PAD	LT	RI	RG	VREF	Z	ZRI
-	-	-	0	-	0	RI
-	-	0	-	-	0	RI
1 ¹	0	1	1	-	1	RI
0 ²	0	1	1	-	0	RI
1 ³	1	1	1	-	1	RI
0 ⁴	1	1	1	-	0	RI

1. PAD input requires AGP4X level "high." AGP4X "high" is V_{ddq} .

2. PAD input requires AGP4X level "low." AGP4X "low" is 0.

3. PAD input requires CMOS level "high." CMOS "high" is V_{dd} .

4. PAD input requires CMOS level "low." CMOS "low" is 0.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd150} = 1.4V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd150} = 1.5V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd150} = 1.6V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$0.788 + 0.035D_{std}$	$0.527 + 0.026D_{std}$	$0.390 + 0.021D_{std}$
		t_{PHL}	$0.759 + 0.036D_{std}$	$0.514 + 0.025D_{std}$	$0.381 + 0.021D_{std}$
	B	t_{PLH}	$0.615 + 0.034D_{std}$	$0.438 + 0.025D_{std}$	$0.347 + 0.021D_{std}$
		t_{PHL}	$0.622 + 0.035D_{std}$	$0.456 + 0.025D_{std}$	$0.362 + 0.020D_{std}$
	C	t_{PLH}	$0.500 + 0.034D_{std}$	$0.360 + 0.025D_{std}$	$0.291 + 0.021D_{std}$
		t_{PHL}	$0.525 + 0.034D_{std}$	$0.390 + 0.024D_{std}$	$0.315 + 0.020D_{std}$



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.386 + 0.001N _{std}	0.251 + 0.001N _{std}	0.169 + 0.001N _{std}
		t _{PHL}	0.382 + 0.001N _{std}	0.255 + 0.001N _{std}	0.174 + 0.001N _{std}
	B	t _{PLH}	0.384 + 0.001N _{std}	0.254 + 0.001N _{std}	0.172 + 0.001N _{std}
		t _{PHL}	0.382 + 0.001N _{std}	0.256 + 0.001N _{std}	0.174 + 0.001N _{std}
	C	t _{PLH}	0.384 + 0.001N _{std}	0.254 + 0.001N _{std}	0.172 + 0.001N _{std}
		t _{PHL}	0.382 + 0.001N _{std}	0.256 + 0.001N _{std}	0.174 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	24.804	26.829	29.358
DI	3.937	3.937	3.945
LT	4.015	4.015	4.015
PAD (Receiver Input)	370.708	370.708	370.708
RG	7.420	7.420	7.420
RI	6.312	6.312	6.312
TS	3.098	3.096	3.095
VREF	110.667	110.667	110.667
Internal	345.166	350.679	357.236
Cell Units	1 cell	1 cell	1 cell

Cell: VAGP4XR1, VAGP4XR1_PM

Function: Voltage Reference Receiver

Description:

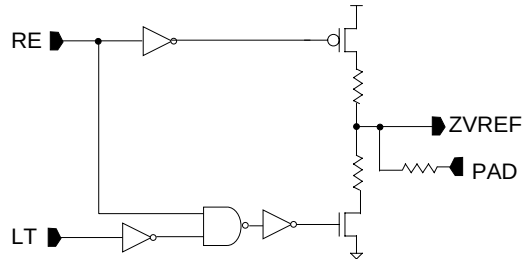
This cell generates a precision on-chip reference voltage ($V_{dd150}/2$). At system mode, the reference may be disabled ($RE = 0$) to apply an external reference voltage through the PAD pin, or the on-chip reference generator may remain enabled ($RE = 1$). When enabled, the reference generator requires 1.0 mA of current.

RE Reference enable input

LT DC current gate (I_{dd} test) input

PAD Connection to package pin

ZVREF Reference voltage



Driver Truth Table

Inputs			Output	Comments
PAD	LT	RE	ZVREF	
-	0	1	X	$ZVREF = 0.5 \cdot V_{dd150}$; used during wafer test
-	1	1	X	$ZVREF = V_{dd150}$
-	-	0	X	Reference generator is Hi-Z; used during packaged device test

Notes:

- Resistance between PAD and VREF is negligible.
- This cell is NOT ALLOWED in 64 test pin locations.

Cell: VAGP4XR2, VAGP4XR2_PM

Function: Supplemental AGP4X Voltage Reference Pin (VREF Driver)

Description:

This cell provides additional PAD for external reference voltage. Additional pads are required to stabilize reference voltage due to noise. A minimum of one is recommended.



VREF Reference voltage

PAD Off-chip supplied reference voltage

Driver Truth Table

Inputs	Outputs	Comments
VREF	PAD	
-	X	Supplemental external VREF pin

Notes:

- a. This cell is NOT ALLOWED in 64 test pin locations.
- b. PAD is electrically hard-wired to VREF. It is used as a supplementary external VREF pin. The customer can provide as many pins on the chip as required.



Cell: BATAUDMA, BATAUDMA_PM

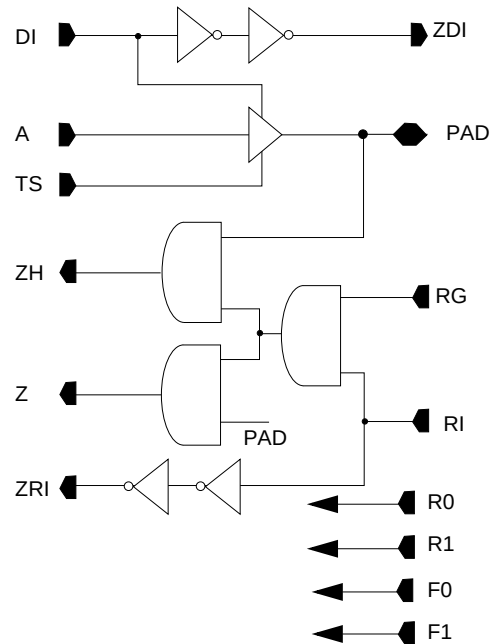
Function: 3.3V (5V Protected) Nontest UDMA 33/66/100 Data and Strobe 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with UDMA 33, 66, and 100 Mb/s off-chip bidirectional data buses. Performance level C is used for data; performance level D is used for strobe. R0, R1, F0, and F1 are input control pins to change the output slew rate. R0 and R1 are for rising slew rate; F0 and F1 are for falling. The slew rate inputs need to be observable in a latch or latches so that the logic circuits and wires for the slew rate controls can be tested. The different slew rates cannot be measured during I/O test. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
PAD	Driver output/receiver input
Z	Non-hysteresis receiver output
ZH	Hysteresis receiver output
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)
R0	Rising slew rate control input 1
R1	Rising slew rate control input 2
F0	Falling slew rate control input 1
F1	Falling slew rate control input 2

Pin Group: (Z, ZH): (1, 2)





Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Slew Rate Control Truth Table

Slew Rate Control (rising)		Slew Rate Control (falling)		Outputs (PAD)	
R0	R1	F0	F1	Rise (Mb/s)	Fall (Mb/s)
0	0	X	X	33 slow	-
0	1	X	X	33 fast	-
1	0	X	X	66	-
1	1	X	X	100	-
X	X	0	0	-	33 slow
X	X	0	1	-	33 fast
X	X	1	0	-	66
X	X	1	1	-	100

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	C	t_{PLH}	$4.342 + 0.062D_{std}$	$2.860 + 0.043D_{std}$	$2.097 + 0.034D_{std}$
		t_{PHL}	$6.096 + 0.045D_{std}$	$4.126 + 0.030D_{std}$	$2.979 + 0.023D_{std}$
	D	t_{PLH}	$4.461 + 0.060D_{std}$	$2.957 + 0.042D_{std}$	$2.187 + 0.032D_{std}$
		t_{PHL}	$6.274 + 0.044D_{std}$	$4.327 + 0.028D_{std}$	$3.158 + 0.021D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	C	t _{PLH}	0.822 + 0.003N _{std}	0.552 + 0.002N _{std}	0.419 + 0.002N _{std}
		t _{PHL}	1.143 + 0.001N _{std}	0.899 + 0.001N _{std}	0.754 + 0.001N _{std}
PAD-ZH		t _{PLH}	5.640 + 0.003N _{std}	3.336 + 0.002N _{std}	2.218 + 0.002N _{std}
		t _{PHL}	4.650 + 0.003N _{std}	3.424 + 0.002N _{std}	2.713 + 0.001N _{std}
PAD-Z	D	t _{PLH}	0.831 + 0.003N _{std}	0.547 + 0.002N _{std}	0.407 + 0.002N _{std}
		t _{PHL}	1.155 + 0.001N _{std}	0.907 + 0.001N _{std}	0.756 + 0.001N _{std}
PAD-ZH		t _{PLH}	5.727 + 0.003N _{std}	3.318 + 0.002N _{std}	2.221 + 0.001N _{std}
		t _{PHL}	4.643 + 0.003N _{std}	3.424 + 0.002N _{std}	2.712 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	C	D
A	4.002	3.986
DI	2.628	2.622
F0	4.543	4.543
F1	4.358	4.358
PAD (Receiver Input)	530.833	530.917
R0	4.474	4.474
R1	4.503	4.503
RG	1.121	1.120
RI	2.836	2.832
TS	2.290	2.285
Internal	959.000	959.000
Cell Units	1 cell	1 cell

Cell: BC1820, BC1820_PM

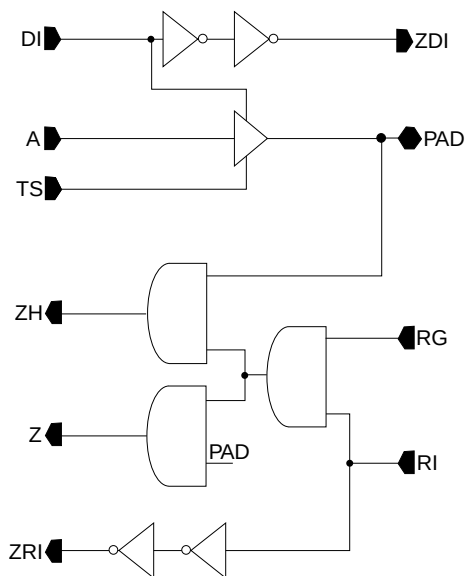
Function: 1.8V CMOS Nontest 20 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.529 + 0.033D _{std}	1.120 + 0.024D _{std}	0.829 + 0.019D _{std}
		t _{PHL}	1.375 + 0.032D _{std}	0.998 + 0.022D _{std}	0.751 + 0.017D _{std}
	B	t _{PLH}	1.320 + 0.030D _{std}	0.976 + 0.022D _{std}	0.735 + 0.017D _{std}
		t _{PHL}	1.214 + 0.030D _{std}	0.881 + 0.020D _{std}	0.671 + 0.015D _{std}
	C	t _{PLH}	1.000 + 0.028D _{std}	0.718 + 0.020D _{std}	0.539 + 0.016D _{std}
		t _{PHL}	0.941 + 0.028D _{std}	0.664 + 0.019D _{std}	0.500 + 0.014D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.264 + 0.000N _{std}	0.189 + 0.000N _{std}	0.146 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.205 + 0.000N _{std}	0.164 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.460 + 0.000N _{std}	0.337 + 0.000N _{std}	0.276 + 0.000N _{std}
		t _{PHL}	0.404 + 0.001N _{std}	0.330 + 0.000N _{std}	0.270 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.265 + 0.000N _{std}	0.185 + 0.000N _{std}	0.139 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.203 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.266 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.265 + 0.000N _{std}	0.185 + 0.000N _{std}	0.139 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.203 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.266 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.604	15.495	15.798
DI	3.737	3.747	3.757
PAD (Receiver Input)	501.042	501.042	501.042
RG	1.918	1.918	1.918
RI	4.122	4.122	4.122
TS	3.016	3.019	3.019
Internal	664.972	682.934	698.807
Cell Units	1 cell	1 cell	1 cell

Cell: BC1835, BC1835_PM

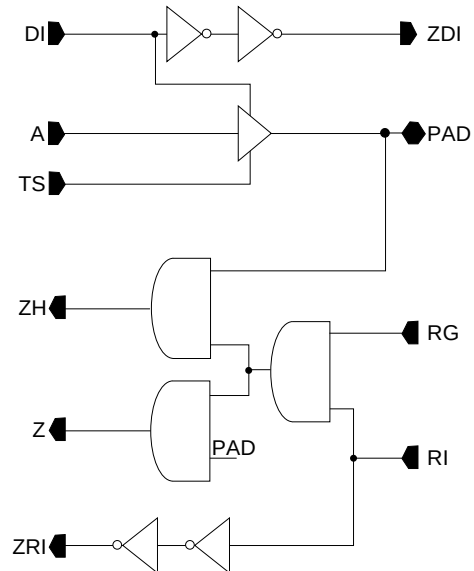
Function: 1.8V CMOS Nontest 35 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
PAD	Driver output/receiver input
ZH	Hysteresis receiver output
Z	Non-hysteresis receiver output
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.466 + 0.046D _{std}	1.077 + 0.035D _{std}	0.808 + 0.029D _{std}
		t _{PHL}	1.336 + 0.046D _{std}	0.975 + 0.033D _{std}	0.742 + 0.027D _{std}
	B	t _{PLH}	1.192 + 0.043D _{std}	0.891 + 0.032D _{std}	0.682 + 0.026D _{std}
		t _{PHL}	1.058 + 0.044D _{std}	0.786 + 0.031D _{std}	0.614 + 0.025D _{std}
	C	t _{PLH}	0.893 + 0.042D _{std}	0.654 + 0.031D _{std}	0.506 + 0.026D _{std}
		t _{PHL}	0.826 + 0.043D _{std}	0.608 + 0.030D _{std}	0.477 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.264 + 0.000N _{std}	0.189 + 0.000N _{std}	0.146 + 0.000N _{std}
PAD-ZH		t _{PHL}	0.252 + 0.001N _{std}	0.205 + 0.000N _{std}	0.165 + 0.000N _{std}
		t _{PLH}	0.461 + 0.000N _{std}	0.337 + 0.000N _{std}	0.277 + 0.000N _{std}
		t _{PHL}	0.404 + 0.001N _{std}	0.331 + 0.000N _{std}	0.270 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.139 + 0.000N _{std}
PAD-ZH		t _{PHL}	0.252 + 0.001N _{std}	0.203 + 0.000N _{std}	0.161 + 0.000N _{std}
		t _{PLH}	0.464 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.266 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.139 + 0.000N _{std}
PAD-ZH		t _{PHL}	0.252 + 0.001N _{std}	0.203 + 0.000N _{std}	0.161 + 0.000N _{std}
		t _{PLH}	0.464 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.266 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.690	15.221	15.616
DI	3.723	3.723	3.722
PAD (Receiver Input)	457.500	457.500	457.500
RG	1.910	1.910	1.910
RI	4.100	4.100	4.100
TS	3.010	3.008	3.008
Internal	652.338	667.676	683.208
Cell Units	1 cell	1 cell	1 cell

Cell: BC1850, BC1850_PM

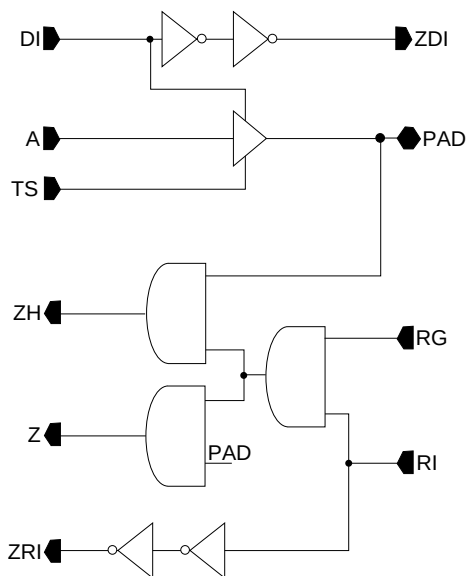
Function: 1.8V CMOS Nontest 50 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.332 + 0.063D _{std}	0.987 + 0.048D _{std}	0.742 + 0.040D _{std}
		t _{PHL}	1.201 + 0.064D _{std}	0.883 + 0.046D _{std}	0.674 + 0.039D _{std}
	B	t _{PLH}	1.045 + 0.060D _{std}	0.776 + 0.045D _{std}	0.601 + 0.038D _{std}
		t _{PHL}	0.895 + 0.062D _{std}	0.680 + 0.045D _{std}	0.539 + 0.037D _{std}
	C	t _{PLH}	0.811 + 0.060D _{std}	0.624 + 0.045D _{std}	0.499 + 0.038D _{std}
		t _{PHL}	0.736 + 0.062D _{std}	0.563 + 0.045D _{std}	0.460 + 0.037D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.264 + 0.000N _{std}	0.189 + 0.000N _{std}	0.146 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.205 + 0.000N _{std}	0.164 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.461 + 0.000N _{std}	0.337 + 0.000N _{std}	0.276 + 0.000N _{std}
		t _{PHL}	0.404 + 0.001N _{std}	0.331 + 0.000N _{std}	0.270 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.140 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.204 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.267 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.140 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.204 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.267 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.643	14.579	15.646
DI	3.748	3.748	3.757
PAD (Receiver Input)	407.792	407.792	407.792
RG	1.918	1.918	1.918
RI	4.122	4.122	4.122
TS	3.015	3.020	3.021
Internal	559.008	562.492	573.638
Cell Units	1 cell	1 cell	1 cell

Cell: BC1865, BC1865_PM

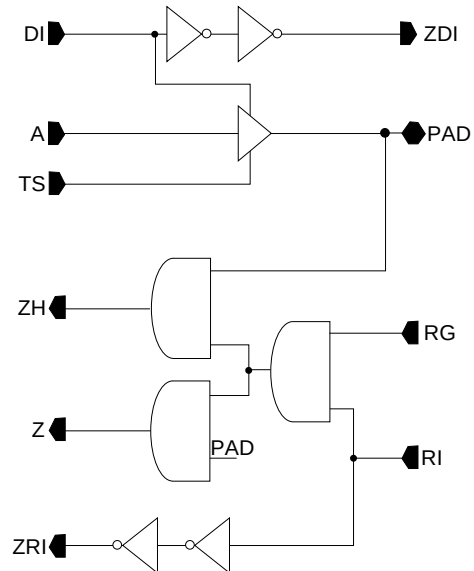
Function: 1.8V CMOS Nontest 65 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
PAD	Driver output/receiver input
ZH	Hysteresis receiver output
Z	Non-hysteresis receiver output
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.174 + 0.081D _{std}	0.875 + 0.061D _{std}	0.661 + 0.051D _{std}
		t _{PHL}	1.052 + 0.083D _{std}	0.771 + 0.060D _{std}	0.588 + 0.049D _{std}
	B	t _{PLH}	0.897 + 0.079D _{std}	0.691 + 0.059D _{std}	0.558 + 0.049D _{std}
		t _{PHL}	0.795 + 0.081D _{std}	0.619 + 0.058D _{std}	0.503 + 0.048D _{std}
	C	t _{PLH}	0.666 + 0.078D _{std}	0.536 + 0.059D _{std}	0.448 + 0.049D _{std}
		t _{PHL}	0.645 + 0.081D _{std}	0.515 + 0.058D _{std}	0.430 + 0.048D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.264 + 0.000N _{std}	0.189 + 0.000N _{std}	0.146 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.205 + 0.000N _{std}	0.165 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.461 + 0.000N _{std}	0.337 + 0.000N _{std}	0.276 + 0.000N _{std}
		t _{PHL}	0.404 + 0.001N _{std}	0.331 + 0.000N _{std}	0.270 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.140 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.204 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.267 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.140 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.204 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.267 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.676	14.630	15.710
DI	3.748	3.751	3.757
PAD (Receiver Input)	368.667	368.708	368.708
RG	1.918	1.918	1.918
RI	4.122	4.122	4.122
TS	3.025	3.025	3.019
Internal	459.655	461.564	470.249
Cell Units	1 cell	1 cell	1 cell

Cell: BC1890, BC1890_PM

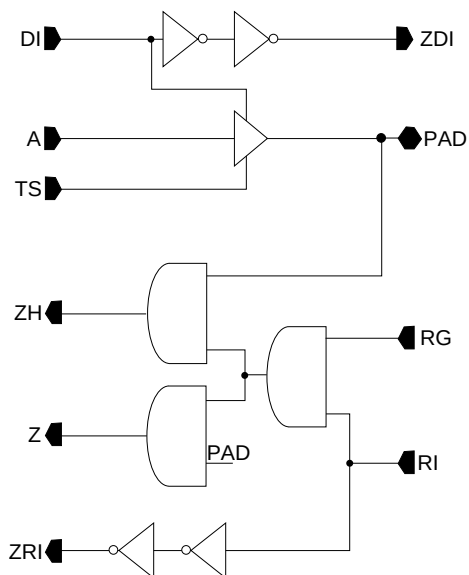
Function: 1.8V CMOS Nontest 90 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	0.995 + 0.112D _{std}	0.743 + 0.084D _{std}	0.567 + 0.071D _{std}
		t _{PHL}	0.921 + 0.113D _{std}	0.673 + 0.082D _{std}	0.514 + 0.069D _{std}
	B	t _{PLH}	0.780 + 0.110D _{std}	0.606 + 0.083D _{std}	0.437 + 0.071D _{std}
		t _{PHL}	0.726 + 0.111D _{std}	0.600 + 0.081D _{std}	0.504 + 0.068D _{std}
	C	t _{PLH}	0.555 + 0.109D _{std}	0.418 + 0.084D _{std}	0.318 + 0.071D _{std}
		t _{PHL}	0.562 + 0.111D _{std}	0.488 + 0.081D _{std}	0.414 + 0.068D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.264 + 0.000N _{std}	0.189 + 0.000N _{std}	0.146 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.205 + 0.000N _{std}	0.165 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.461 + 0.000N _{std}	0.337 + 0.000N _{std}	0.277 + 0.000N _{std}
		t _{PHL}	0.404 + 0.001N _{std}	0.331 + 0.000N _{std}	0.270 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.140 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.204 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.274 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.267 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.140 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.204 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.274 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.267 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.677	14.751	16.312
DI	3.752	3.758	3.757
PAD (Receiver Input)	341.000	341.042	341.042
RG	1.918	1.918	1.918
RI	4.122	4.122	4.122
TS	3.025	3.023	3.022
Internal	400.738	402.284	412.296
Cell Units	1 cell	1 cell	1 cell

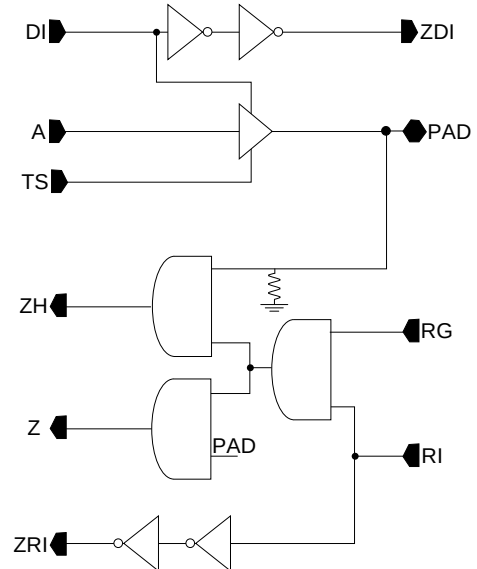
Cell: BC1820PD, BC1820PD_PM

Function: 1.8V CMOS Nontest 20 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
L	1	1	0	0	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.533 + 0.033D _{std}	1.126 + 0.024D _{std}	0.837 + 0.019D _{std}
		t _{PHL}	1.366 + 0.032D _{std}	0.991 + 0.022D _{std}	0.743 + 0.017D _{std}
	B	t _{PLH}	1.324 + 0.030D _{std}	0.981 + 0.022D _{std}	0.738 + 0.017D _{std}
		t _{PHL}	1.209 + 0.030D _{std}	0.876 + 0.020D _{std}	0.667 + 0.015D _{std}
	C	t _{PLH}	1.002 + 0.028D _{std}	0.721 + 0.020D _{std}	0.541 + 0.016D _{std}
		t _{PHL}	0.938 + 0.028D _{std}	0.661 + 0.019D _{std}	0.498 + 0.014D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.288 + 0.000N _{std}	0.215 + 0.000N _{std}	0.172 + 0.000N _{std}
		t _{PHL}	0.257 + 0.001N _{std}	0.200 + 0.000N _{std}	0.156 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.485 + 0.000N _{std}	0.363 + 0.000N _{std}	0.303 + 0.000N _{std}
		t _{PHL}	0.411 + 0.001N _{std}	0.328 + 0.000N _{std}	0.263 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.355 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.399 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.355 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.399 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.594	15.483	15.791
DI	3.738	3.748	3.757
PAD (Receiver Input)	482.625	502.042	502.042
RG	1.918	1.918	1.918
RI	4.127	4.127	4.127
TS	3.018	3.022	3.022
Internal	509.376	521.281	528.133
Cell Units	1 cell	1 cell	1 cell

Cell: BC1835PD, BC1835PD_PM

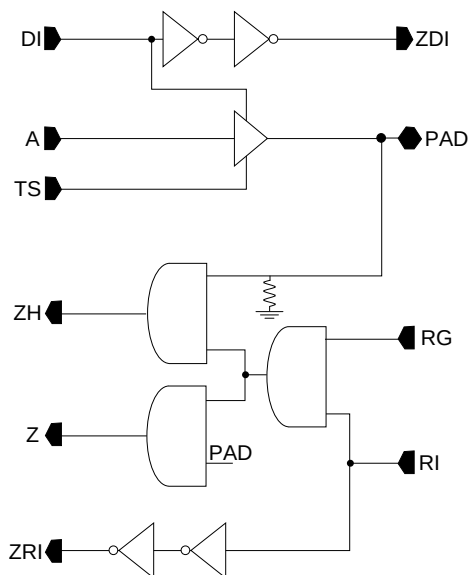
Function: 1.8V CMOS Nontest 35 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
L	1	1	0	0	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.472 + 0.046D _{std}	1.086 + 0.035D _{std}	0.818 + 0.029D _{std}
		t _{PHL}	1.327 + 0.046D _{std}	0.969 + 0.033D _{std}	0.735 + 0.027D _{std}
	B	t _{PLH}	1.201 + 0.043D _{std}	0.897 + 0.032D _{std}	0.690 + 0.027D _{std}
		t _{PHL}	1.057 + 0.043D _{std}	0.783 + 0.031D _{std}	0.610 + 0.025D _{std}
	C	t _{PLH}	0.897 + 0.042D _{std}	0.658 + 0.031D _{std}	0.510 + 0.026D _{std}
		t _{PHL}	0.824 + 0.043D _{std}	0.606 + 0.030D _{std}	0.476 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.276 + 0.000N _{std}	0.206 + 0.000N _{std}	0.165 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.191 + 0.000N _{std}	0.149 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.473 + 0.000N _{std}	0.355 + 0.000N _{std}	0.296 + 0.000N _{std}
		t _{PHL}	0.398 + 0.001N _{std}	0.319 + 0.000N _{std}	0.256 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.694	15.232	15.615
DI	3.737	3.737	3.748
PAD (Receiver Input)	458.500	458.542	458.750
RG	1.918	1.918	1.918
RI	4.122	4.122	4.127
TS	3.023	3.021	3.022
Internal	547.324	556.745	563.024
Cell Units	1 cell	1 cell	1 cell

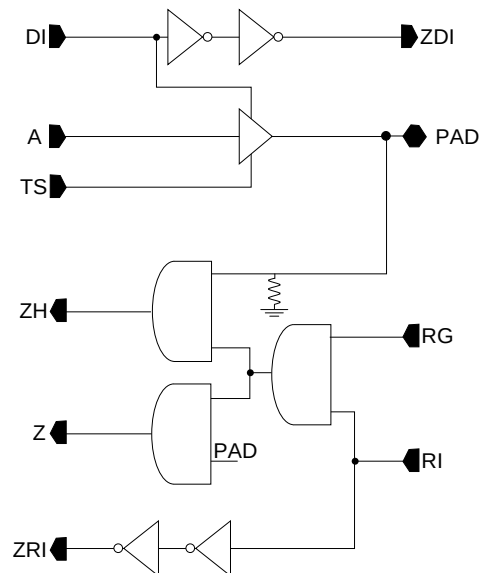
Cell: BC1850PD, BC1850PD_PM

Function: 1.8V CMOS Nontest 50 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
L	1	1	0	0	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.338 + 0.063D _{std}	0.993 + 0.048D _{std}	0.748 + 0.040D _{std}
		t _{PHL}	1.192 + 0.063D _{std}	0.874 + 0.046D _{std}	0.666 + 0.038D _{std}
	B	t _{PLH}	1.048 + 0.060D _{std}	0.781 + 0.046D _{std}	0.607 + 0.038D _{std}
		t _{PHL}	0.891 + 0.061D _{std}	0.676 + 0.044D _{std}	0.535 + 0.037D _{std}
	C	t _{PLH}	0.813 + 0.060D _{std}	0.627 + 0.045D _{std}	0.502 + 0.038D _{std}
		t _{PHL}	0.734 + 0.061D _{std}	0.560 + 0.044D _{std}	0.457 + 0.036D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.276 + 0.000N _{std}	0.206 + 0.000N _{std}	0.165 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.191 + 0.000N _{std}	0.149 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.473 + 0.000N _{std}	0.355 + 0.000N _{std}	0.296 + 0.000N _{std}
		t _{PHL}	0.399 + 0.001N _{std}	0.319 + 0.000N _{std}	0.256 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.246 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.246 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.640	14.645	15.653
DI	3.734	3.745	3.754
PAD (Receiver Input)	409.167	409.208	409.208
RG	1.918	1.918	1.918
RI	4.127	4.127	4.127
TS	3.015	3.020	3.022
Internal	536.861	536.449	544.010
Cell Units	1 cell	1 cell	1 cell

Cell: BC1865PD, BC1865PD_PM

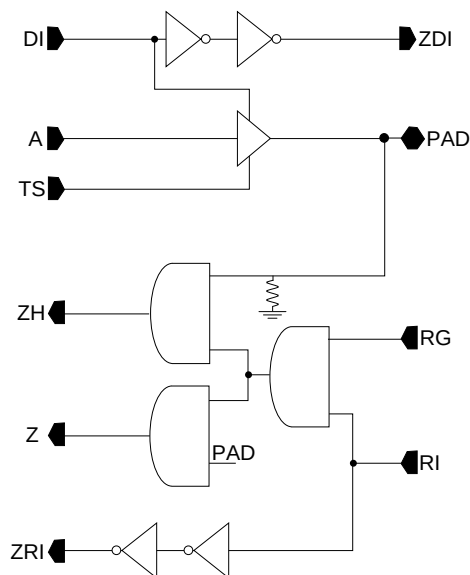
Function: 1.8V CMOS Nontest 65 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
L	1	1	0	0	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.179 + 0.082D _{std}	0.881 + 0.062D _{std}	0.667 + 0.052D _{std}
		t _{PHL}	1.044 + 0.081D _{std}	0.762 + 0.058D _{std}	0.581 + 0.048D _{std}
	B	t _{PLH}	0.902 + 0.079D _{std}	0.695 + 0.060D _{std}	0.564 + 0.050D _{std}
		t _{PHL}	0.789 + 0.080D _{std}	0.616 + 0.057D _{std}	0.499 + 0.047D _{std}
	C	t _{PLH}	0.668 + 0.079D _{std}	0.541 + 0.059D _{std}	0.450 + 0.050D _{std}
		t _{PHL}	0.639 + 0.079D _{std}	0.506 + 0.057D _{std}	0.412 + 0.047D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.276 + 0.000N _{std}	0.206 + 0.000N _{std}	0.165 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.191 + 0.000N _{std}	0.149 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.473 + 0.000N _{std}	0.355 + 0.000N _{std}	0.296 + 0.000N _{std}
		t _{PHL}	0.399 + 0.001N _{std}	0.319 + 0.000N _{std}	0.256 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.246 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.246 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.680	14.688	15.692
DI	3.740	3.740	3.755
PAD (Receiver Input)	370.167	370.167	370.167
RG	1.918	1.918	1.918
RI	4.127	4.127	4.127
TS	3.025	3.025	3.021
Internal	524.013	524.764	531.112
Cell Units	1 cell	1 cell	1 cell

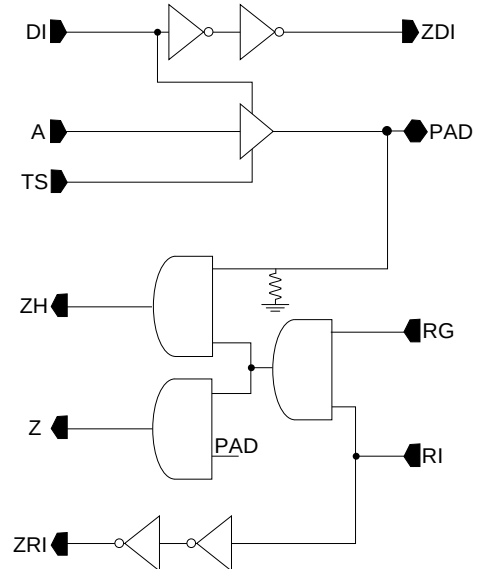
Cell: BC1890PD, BC1890PD_PM

Function: 1.8V CMOS Nontest 90 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
RI Receiver inhibit input (RI in)
RG Receiver gate control
PAD Driver output/receiver input
ZH Hysteresis receiver output
Z Non-hysteresis receiver output
ZDI Driver inhibit output (DI out)
ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
L	1	1	0	0	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.000 + 0.113D _{std}	0.749 + 0.086D _{std}	0.574 + 0.072D _{std}
		t _{PHL}	0.912 + 0.111D _{std}	0.664 + 0.080D _{std}	0.506 + 0.067D _{std}
	B	t _{PLH}	0.786 + 0.111D _{std}	0.576 + 0.085D _{std}	0.457 + 0.072D _{std}
		t _{PHL}	0.722 + 0.109D _{std}	0.592 + 0.079D _{std}	0.491 + 0.066D _{std}
	C	t _{PLH}	0.555 + 0.111D _{std}	0.457 + 0.085D _{std}	0.361 + 0.072D _{std}
		t _{PHL}	0.555 + 0.109D _{std}	0.475 + 0.079D _{std}	0.414 + 0.065D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.276 + 0.000N _{std}	0.206 + 0.000N _{std}	0.165 + 0.000N _{std}
PAD-ZH		t _{PHL}	0.245 + 0.001N _{std}	0.192 + 0.000N _{std}	0.149 + 0.000N _{std}
		t _{PLH}	0.473 + 0.000N _{std}	0.355 + 0.000N _{std}	0.296 + 0.000N _{std}
		t _{PHL}	0.399 + 0.001N _{std}	0.319 + 0.000N _{std}	0.256 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.278 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
PAD-ZH		t _{PHL}	0.245 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.278 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
PAD-ZH		t _{PHL}	0.245 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.740	14.740	16.318
DI	3.742	3.749	3.755
PAD (Receiver Input)	342.375	342.375	342.375
RG	1.918	1.918	1.918
RI	4.122	4.122	4.122
TS	3.026	3.024	3.025
Internal	569.566	570.365	579.155
Cell Units	1 cell	1 cell	1 cell

Cell: BC1820PU, BC1820PU_PM

Function: 1.8V CMOS Nontest 20 Ohm 3-State CIO w/Pull-Up

Description:

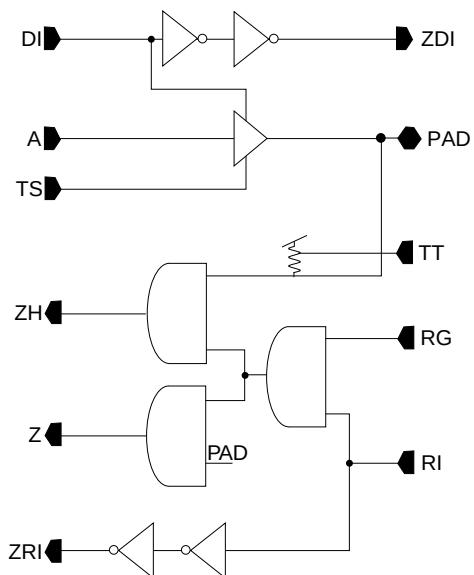
Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (1.8V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
TT	Termination test input
PAD	Driver output/receiver input
ZH	Hysteresis receiver output
Z	Non-hysteresis receiver output
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1,H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.518 + 0.032D_{std}$	$1.111 + 0.024D_{std}$	$0.823 + 0.019D_{std}$
		t_{PHL}	$1.380 + 0.032D_{std}$	$1.002 + 0.022D_{std}$	$0.754 + 0.017D_{std}$
	B	t_{PLH}	$1.312 + 0.030D_{std}$	$0.970 + 0.021D_{std}$	$0.730 + 0.017D_{std}$
		t_{PHL}	$1.219 + 0.030D_{std}$	$0.884 + 0.020D_{std}$	$0.673 + 0.015D_{std}$
	C	t_{PLH}	$0.995 + 0.027D_{std}$	$0.715 + 0.020D_{std}$	$0.536 + 0.015D_{std}$
		t_{PHL}	$0.944 + 0.028D_{std}$	$0.666 + 0.019D_{std}$	$0.501 + 0.014D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.253 + 0.000N_{std}$	$0.176 + 0.000N_{std}$	$0.132 + 0.000N_{std}$
		t_{PHL}	$0.266 + 0.001N_{std}$	$0.220 + 0.000N_{std}$	$0.181 + 0.000N_{std}$
PAD-ZH		t_{PLH}	$0.451 + 0.000N_{std}$	$0.325 + 0.000N_{std}$	$0.263 + 0.000N_{std}$
		t_{PHL}	$0.419 + 0.001N_{std}$	$0.347 + 0.000N_{std}$	$0.287 + 0.000N_{std}$



Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.220 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.285 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.220 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.285 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.601	15.483	15.791
DI	3.738	3.738	3.752
PAD (Receiver Input)	502.458	502.333	501.875
RG	1.918	1.918	1.918
RI	4.140	4.140	4.140
TS	3.033	3.034	3.043
TT	1.393	1.393	1.393
Internal	356.921	348.585	341.513
Cell Units	1 cell	1 cell	1 cell

Cell: BC1835PU, BC1835PU_PM

Function: 1.8V CMOS Nontest 35 Ohm 3-State CIO w/Pull-Up

Description:

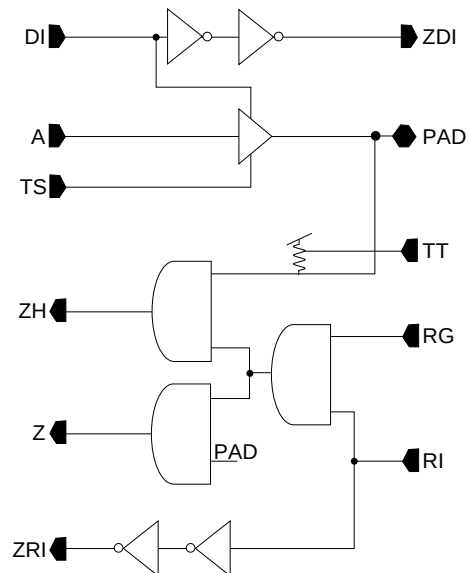
Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (1.8V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled





Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1,H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.452 + 0.046D _{std}	1.068 + 0.035D _{std}	0.803 + 0.029D _{std}
		t _{PHL}	1.342 + 0.046D _{std}	0.983 + 0.033D _{std}	0.747 + 0.027D _{std}
	B	t _{PLH}	1.190 + 0.042D _{std}	0.887 + 0.032D _{std}	0.679 + 0.026D _{std}
		t _{PHL}	1.065 + 0.044D _{std}	0.791 + 0.031D _{std}	0.617 + 0.025D _{std}
	C	t _{PLH}	0.891 + 0.041D _{std}	0.652 + 0.031D _{std}	0.505 + 0.026D _{std}
		t _{PHL}	0.829 + 0.043D _{std}	0.610 + 0.031D _{std}	0.480 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.254 + 0.000N _{std}	0.176 + 0.000N _{std}	0.131 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.220 + 0.000N _{std}	0.181 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.452 + 0.000N _{std}	0.325 + 0.000N _{std}	0.264 + 0.000N _{std}
		t _{PHL}	0.419 + 0.001N _{std}	0.347 + 0.000N _{std}	0.287 + 0.000N _{std}

Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.221 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.286 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.267 + 0.001N _{std}	0.221 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.286 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.680	15.232	15.615
DI	3.738	3.738	3.749
PAD (Receiver Input)	458.708	458.708	458.708
RG	1.918	1.918	1.918
RI	4.140	4.140	4.140
TS	3.037	3.034	3.040
TT	1.393	1.393	1.393
Internal	356.000	348.000	341.000
Cell Units	1 cell	1 cell	1 cell

Cell: BC1850PU, BC1850PU_PM

Function: 1.8V CMOS Nontest 50 Ohm 3-State CIO w/Pull-Up

Description:

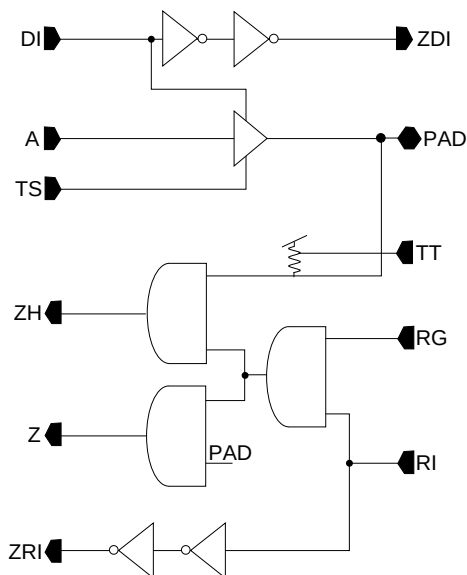
Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (1.8V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
TT	Termination test input
PAD	Driver output/receiver input
ZH	Hysteresis receiver output
Z	Non-hysteresis receiver output
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1,H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.319 + 0.062D _{std}	0.976 + 0.047D _{std}	0.734 + 0.039D _{std}
		t _{PHL}	1.206 + 0.064D _{std}	0.887 + 0.047D _{std}	0.678 + 0.039D _{std}
	B	t _{PLH}	1.037 + 0.059D _{std}	0.771 + 0.045D _{std}	0.600 + 0.037D _{std}
		t _{PHL}	0.897 + 0.063D _{std}	0.682 + 0.045D _{std}	0.541 + 0.037D _{std}
	C	t _{PLH}	0.803 + 0.059D _{std}	0.620 + 0.044D _{std}	0.495 + 0.037D _{std}
		t _{PHL}	0.737 + 0.062D _{std}	0.565 + 0.045D _{std}	0.458 + 0.037D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.254 + 0.000N _{std}	0.176 + 0.000N _{std}	0.131 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.220 + 0.000N _{std}	0.181 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.452 + 0.000N _{std}	0.325 + 0.000N _{std}	0.263 + 0.000N _{std}
		t _{PHL}	0.419 + 0.001N _{std}	0.348 + 0.000N _{std}	0.288 + 0.000N _{std}



Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.267 + 0.001N _{std}	0.221 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.286 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.267 + 0.001N _{std}	0.221 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.286 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.640	14.572	15.654
DI	3.738	3.750	3.749
PAD (Receiver Input)	409.125	409.167	409.167
RG	1.918	1.918	1.918
RI	4.140	4.140	4.140
TS	3.040	3.042	3.041
TT	1.393	1.393	1.393
Internal	412.504	406.252	403.243
Cell Units	1 cell	1 cell	1 cell

Cell: BC1865PU, BC1865PU_PM

Function: 1.8V CMOS Nontest 65 Ohm 3-State CIO w/Pull-Up

Description:

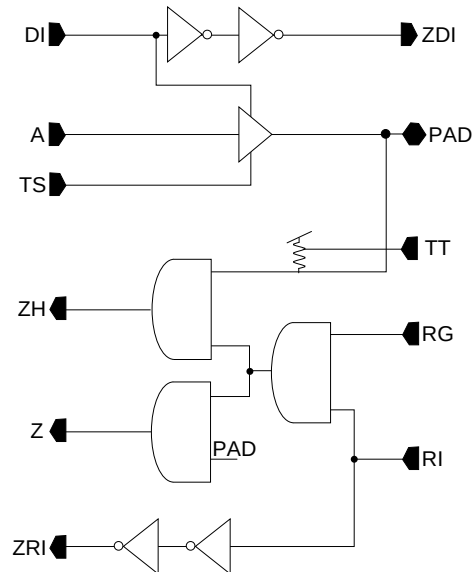
Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (1.8V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
TT	Termination test input
PAD	Driver output/receiver input
ZH	Hysteresis receiver output
Z	Non-hysteresis receiver output
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled





Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1,H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.161 + 0.080D _{std}	0.863 + 0.060D _{std}	0.653 + 0.050D _{std}
		t _{PHL}	1.056 + 0.083D _{std}	0.775 + 0.060D _{std}	0.591 + 0.050D _{std}
	B	t _{PLH}	0.893 + 0.077D _{std}	0.688 + 0.058D _{std}	0.549 + 0.049D _{std}
		t _{PHL}	0.796 + 0.082D _{std}	0.621 + 0.059D _{std}	0.509 + 0.049D _{std}
	C	t _{PLH}	0.662 + 0.077D _{std}	0.526 + 0.058D _{std}	0.434 + 0.049D _{std}
		t _{PHL}	0.648 + 0.081D _{std}	0.508 + 0.059D _{std}	0.432 + 0.049D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.254 + 0.000N _{std}	0.176 + 0.000N _{std}	0.131 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.220 + 0.000N _{std}	0.181 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.452 + 0.000N _{std}	0.325 + 0.000N _{std}	0.263 + 0.000N _{std}
		t _{PHL}	0.419 + 0.001N _{std}	0.348 + 0.000N _{std}	0.288 + 0.000N _{std}

Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.221 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.286 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.221 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.286 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.680	14.688	15.695
DI	3.738	3.759	3.752
PAD (Receiver Input)	370.042	370.083	370.083
RG	1.918	1.918	1.918
RI	4.140	4.140	4.140
TS	3.045	3.042	3.043
TT	1.393	1.393	1.393
Internal	397.242	408.436	392.889
Cell Units	1 cell	1 cell	1 cell

Cell: BC1890PU, BC1890PU_PM

Function: 1.8V CMOS Nontest 90 Ohm 3-State CIO w/Pull-Up

Description:

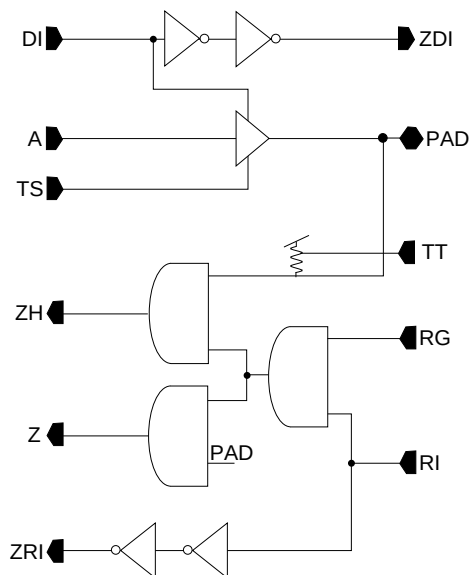
Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (1.8V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
TT	Termination test input
PAD	Driver output/receiver input
ZH	Hysteresis receiver output
Z	Non-hysteresis receiver output
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1,H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	0.981 + 0.109D _{std}	0.732 + 0.082D _{std}	0.558 + 0.069D _{std}
		t _{PHL}	0.923 + 0.115D _{std}	0.675 + 0.084D _{std}	0.516 + 0.070D _{std}
	B	t _{PLH}	0.770 + 0.107D _{std}	0.602 + 0.081D _{std}	0.433 + 0.069D _{std}
		t _{PHL}	0.722 + 0.113D _{std}	0.595 + 0.082D _{std}	0.506 + 0.068D _{std}
	C	t _{PLH}	0.591 + 0.106D _{std}	0.410 + 0.082D _{std}	0.349 + 0.069D _{std}
		t _{PHL}	0.557 + 0.113D _{std}	0.482 + 0.082D _{std}	0.419 + 0.069D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.254 + 0.000N _{std}	0.176 + 0.000N _{std}	0.131 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.220 + 0.000N _{std}	0.181 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.452 + 0.000N _{std}	0.325 + 0.000N _{std}	0.263 + 0.000N _{std}
		t _{PHL}	0.419 + 0.001N _{std}	0.348 + 0.000N _{std}	0.288 + 0.000N _{std}



Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.267 + 0.001N _{std}	0.221 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.421 + 0.001N _{std}	0.349 + 0.000N _{std}	0.286 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.267 + 0.001N _{std}	0.221 + 0.000N _{std}	0.180 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.421 + 0.001N _{std}	0.349 + 0.000N _{std}	0.286 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.722	14.726	16.305
DI	3.750	3.760	3.759
PAD (Receiver Input)	342.500	342.542	342.542
RG	1.918	1.918	1.918
RI	4.145	4.140	4.140
TS	3.046	3.046	3.045
TT	1.393	1.393	1.393
Internal	412.000	406.000	396.000
Cell Units	1 cell	1 cell	1 cell

Cell: BC2520, BC2520_PM

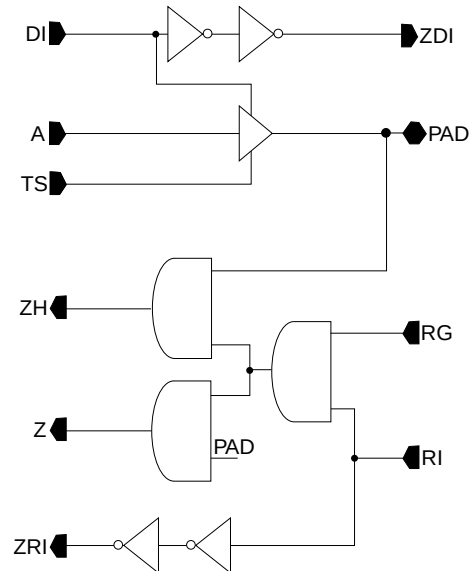
Function: 2.5V CMOS Nontest 20 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.647 + 0.021D _{std}	1.192 + 0.016D _{std}	0.880 + 0.013D _{std}
		t _{PHL}	1.625 + 0.023D _{std}	1.182 + 0.016D _{std}	0.878 + 0.013D _{std}
	B	t _{PLH}	1.526 + 0.019D _{std}	1.084 + 0.014D _{std}	0.800 + 0.011D _{std}
		t _{PHL}	1.497 + 0.021D _{std}	1.071 + 0.015D _{std}	0.800 + 0.012D _{std}
	C	t _{PLH}	1.351 + 0.018D _{std}	0.933 + 0.013D _{std}	0.683 + 0.010D _{std}
		t _{PHL}	1.336 + 0.020D _{std}	0.937 + 0.014D _{std}	0.690 + 0.011D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.291 + 0.001N _{std}	0.220 + 0.001N _{std}
		t _{PHL}	0.391 + 0.002N _{std}	0.309 + 0.001N _{std}	0.250 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.432 + 0.001N _{std}	0.345 + 0.001N _{std}
		t _{PHL}	0.548 + 0.002N _{std}	0.450 + 0.001N _{std}	0.373 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.430 + 0.002N _{std}	0.288 + 0.001N _{std}	0.214 + 0.001N _{std}
		t _{PHL}	0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.433 + 0.001N _{std}	0.344 + 0.001N _{std}
		t _{PHL}	0.555 + 0.002N _{std}	0.456 + 0.001N _{std}	0.375 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.430 + 0.002N _{std}	0.288 + 0.001N _{std}	0.214 + 0.001N _{std}
		t _{PHL}	0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.433 + 0.001N _{std}	0.344 + 0.001N _{std}
		t _{PHL}	0.555 + 0.002N _{std}	0.456 + 0.001N _{std}	0.375 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	10.679	10.680	10.679
DI	7.150	7.150	7.150
PAD (Receiver Input)	501.417	501.417	501.417
RG	1.933	1.933	1.933
RI	3.427	3.427	3.427
TS	6.163	6.163	6.167
Internal	474.863	466.104	464.575
Cell Units	1 cell	1 cell	1 cell

Cell: BC2535, BC2535_PM

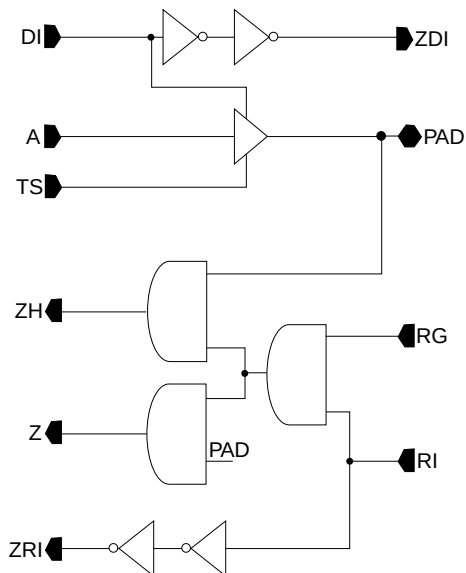
Function: 2.5V CMOS Nontest 35 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.617 + 0.031D _{std}	1.175 + 0.023D _{std}	0.870 + 0.019D _{std}
		t _{PHL}	1.590 + 0.032D _{std}	1.160 + 0.023D _{std}	0.862 + 0.019D _{std}
	B	t _{PLH}	1.473 + 0.029D _{std}	1.065 + 0.022D _{std}	0.801 + 0.018D _{std}
		t _{PHL}	1.439 + 0.030D _{std}	1.049 + 0.022D _{std}	0.793 + 0.018D _{std}
	C	t _{PLH}	1.292 + 0.029D _{std}	0.911 + 0.021D _{std}	0.682 + 0.018D _{std}
		t _{PHL}	1.273 + 0.030D _{std}	0.909 + 0.021D _{std}	0.683 + 0.018D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.291 + 0.001N _{std}	0.220 + 0.001N _{std}
		t _{PHL}	0.391 + 0.002N _{std}	0.310 + 0.001N _{std}	0.251 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.432 + 0.001N _{std}	0.345 + 0.001N _{std}
t _{PHL}		0.548 + 0.002N _{std}	0.451 + 0.001N _{std}	0.373 + 0.001N _{std}	
PAD-Z	B	t _{PLH}	0.431 + 0.002N _{std}	0.288 + 0.001N _{std}	0.215 + 0.001N _{std}
		t _{PHL}	0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.433 + 0.001N _{std}	0.344 + 0.001N _{std}
		t _{PHL}	0.555 + 0.002N _{std}	0.456 + 0.001N _{std}	0.375 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.431 + 0.002N _{std}	0.288 + 0.001N _{std}	0.215 + 0.001N _{std}
		t _{PHL}	0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.433 + 0.001N _{std}	0.344 + 0.001N _{std}
		t _{PHL}	0.555 + 0.002N _{std}	0.456 + 0.001N _{std}	0.375 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	10.675	10.680	10.652
DI	7.151	7.151	7.179
PAD (Receiver Input)	459.583	459.583	459.583
RG	1.933	1.933	1.933
RI	3.427	3.427	3.427
TS	6.167	6.167	6.167
Internal	604.630	603.172	601.628
Cell Units	1 cell	1 cell	1 cell

Cell: BC2550, BC2550_PM

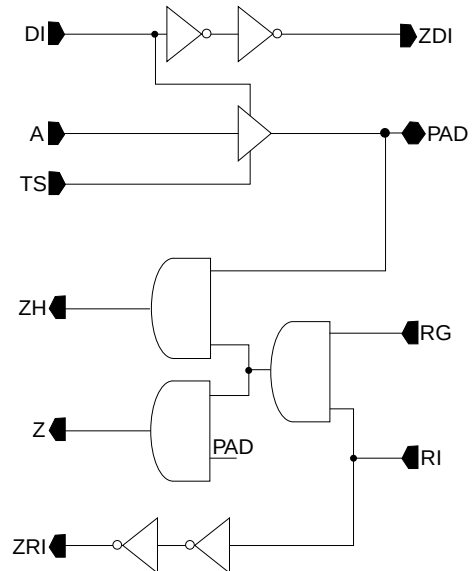
Function: 2.5V CMOS Nontest 50 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.581 + 0.041D _{std}	1.158 + 0.032D _{std}	0.863 + 0.026D _{std}
		t _{PHL}	1.550 + 0.042D _{std}	1.137 + 0.031D _{std}	0.849 + 0.026D _{std}
	B	t _{PLH}	1.421 + 0.040D _{std}	1.051 + 0.030D _{std}	0.805 + 0.025D _{std}
		t _{PHL}	1.386 + 0.041D _{std}	1.032 + 0.030D _{std}	0.795 + 0.025D _{std}
	C	t _{PLH}	1.239 + 0.040D _{std}	0.896 + 0.030D _{std}	0.690 + 0.025D _{std}
		t _{PHL}	1.217 + 0.041D _{std}	0.892 + 0.030D _{std}	0.684 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.291 + 0.001N _{std}	0.220 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.310 + 0.001N _{std}	0.251 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.432 + 0.001N _{std}	0.345 + 0.001N _{std}
		t _{PHL}	0.548 + 0.002N _{std}	0.451 + 0.001N _{std}	0.373 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.431 + 0.002N _{std}	0.288 + 0.001N _{std}	0.215 + 0.001N _{std}
		t _{PHL}	0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.433 + 0.001N _{std}	0.344 + 0.001N _{std}
		t _{PHL}	0.555 + 0.002N _{std}	0.456 + 0.001N _{std}	0.375 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.431 + 0.002N _{std}	0.288 + 0.001N _{std}	0.215 + 0.001N _{std}
		t _{PHL}	0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.433 + 0.001N _{std}	0.344 + 0.001N _{std}
		t _{PHL}	0.555 + 0.002N _{std}	0.456 + 0.001N _{std}	0.375 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	10.688	10.687	10.679
DI	7.151	7.151	7.179
PAD (Receiver Input)	437.833	437.833	437.833
RG	1.933	1.933	1.933
RI	3.427	3.427	3.427
TS	6.167	6.167	6.167
Internal	730.244	730.706	731.427
Cell Units	1 cell	1 cell	1 cell

Cell: BC2565, BC2565_PM

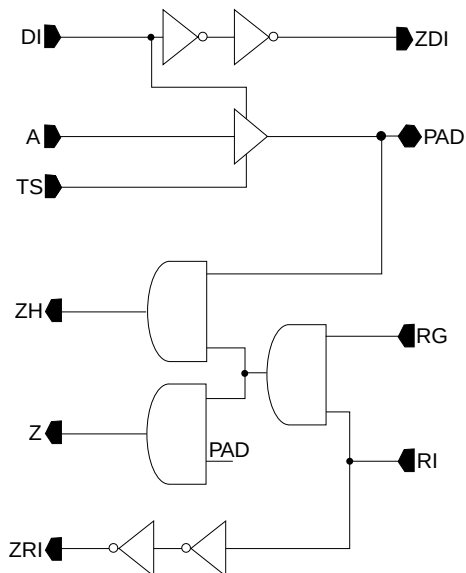
Function: 2.5V CMOS Nontest 65 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.562 + 0.052D _{std}	1.148 + 0.040D _{std}	0.862 + 0.034D _{std}
		t _{PHL}	1.539 + 0.052D _{std}	1.123 + 0.040D _{std}	0.842 + 0.034D _{std}
	B	t _{PLH}	1.380 + 0.051D _{std}	1.045 + 0.039D _{std}	0.811 + 0.034D _{std}
		t _{PHL}	1.350 + 0.051D _{std}	1.028 + 0.039D _{std}	0.807 + 0.033D _{std}
	C	t _{PLH}	1.199 + 0.051D _{std}	0.882 + 0.039D _{std}	0.691 + 0.034D _{std}
		t _{PHL}	1.181 + 0.051D _{std}	0.881 + 0.038D _{std}	0.689 + 0.033D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.291 + 0.001N _{std}	0.220 + 0.001N _{std}
		t _{PHL}	0.391 + 0.002N _{std}	0.310 + 0.001N _{std}	0.251 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.432 + 0.001N _{std}	0.345 + 0.001N _{std}
t _{PHL}		0.548 + 0.002N _{std}	0.451 + 0.001N _{std}	0.373 + 0.001N _{std}	
PAD-Z	B	t _{PLH}	0.431 + 0.002N _{std}	0.288 + 0.001N _{std}	0.215 + 0.001N _{std}
t _{PHL}		0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}	
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.434 + 0.001N _{std}	0.344 + 0.001N _{std}
		t _{PHL}	0.556 + 0.002N _{std}	0.456 + 0.001N _{std}	0.375 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.431 + 0.002N _{std}	0.288 + 0.001N _{std}	0.215 + 0.001N _{std}
t _{PHL}		0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}	
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.434 + 0.001N _{std}	0.344 + 0.001N _{std}
		t _{PHL}	0.556 + 0.002N _{std}	0.456 + 0.001N _{std}	0.375 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	10.688	10.687	10.687
DI	7.151	7.151	7.152
PAD (Receiver Input)	430.583	430.583	430.583
RG	1.933	1.933	1.933
RI	3.427	3.427	3.427
TS	6.167	6.167	6.167
Internal	814.544	845.729	865.455
Cell Units	1 cell	1 cell	1 cell

Cell: BC2590, BC2590_PM

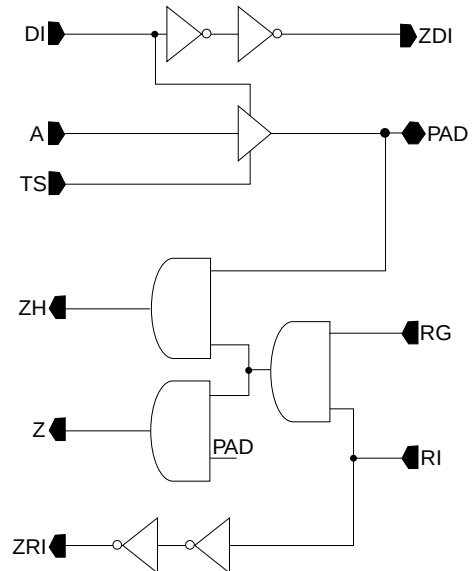
Function: 2.5V CMOS Nontest 90 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.353 + 0.074D _{std}	0.982 + 0.056D _{std}	0.733 + 0.047D _{std}
		t _{PHL}	1.374 + 0.075D _{std}	1.015 + 0.055D _{std}	0.756 + 0.047D _{std}
	B	t _{PLH}	1.209 + 0.073D _{std}	0.924 + 0.056D _{std}	0.731 + 0.047D _{std}
		t _{PHL}	1.311 + 0.073D _{std}	1.018 + 0.054D _{std}	0.806 + 0.045D _{std}
	C	t _{PLH}	1.043 + 0.073D _{std}	0.763 + 0.056D _{std}	0.611 + 0.047D _{std}
		t _{PHL}	1.121 + 0.073D _{std}	0.863 + 0.054D _{std}	0.685 + 0.045D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.291 + 0.001N _{std}	0.220 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.310 + 0.001N _{std}	0.251 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.432 + 0.001N _{std}	0.345 + 0.001N _{std}
		t _{PHL}	0.548 + 0.002N _{std}	0.451 + 0.001N _{std}	0.373 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.431 + 0.002N _{std}	0.288 + 0.001N _{std}	0.215 + 0.001N _{std}
		t _{PHL}	0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.434 + 0.001N _{std}	0.344 + 0.001N _{std}
		t _{PHL}	0.556 + 0.002N _{std}	0.456 + 0.001N _{std}	0.376 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.431 + 0.002N _{std}	0.288 + 0.001N _{std}	0.215 + 0.001N _{std}
		t _{PHL}	0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.434 + 0.001N _{std}	0.344 + 0.001N _{std}
		t _{PHL}	0.556 + 0.002N _{std}	0.456 + 0.001N _{std}	0.376 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	10.686	10.686	10.685
DI	7.151	7.151	7.178
PAD (Receiver Input)	326.625	326.625	326.625
RG	1.933	1.933	1.933
RI	3.427	3.427	3.427
TS	6.167	6.167	6.166
Internal	832.000	844.000	836.000
Cell Units	1 cell	1 cell	1 cell

Cell: BC2520PD, BC2520PD_PM

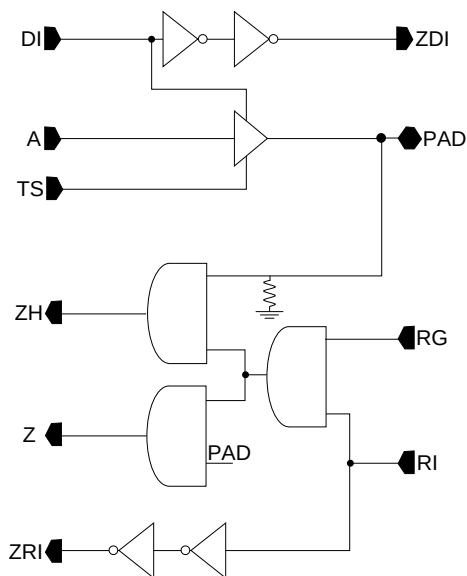
Function: 2.5V CMOS Nontest 20 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
L	1	1	0	0	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.649 + 0.021D _{std}	1.194 + 0.016D _{std}	0.879 + 0.013D _{std}
		t _{PHL}	1.623 + 0.023D _{std}	1.177 + 0.016D _{std}	0.871 + 0.013D _{std}
	B	t _{PLH}	1.528 + 0.019D _{std}	1.084 + 0.014D _{std}	0.796 + 0.011D _{std}
		t _{PHL}	1.492 + 0.021D _{std}	1.065 + 0.015D _{std}	0.791 + 0.011D _{std}
	C	t _{PLH}	1.351 + 0.018D _{std}	0.933 + 0.013D _{std}	0.681 + 0.010D _{std}
		t _{PHL}	1.335 + 0.020D _{std}	0.934 + 0.014D _{std}	0.685 + 0.011D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.435 + 0.002N _{std}	0.306 + 0.001N _{std}	0.237 + 0.001N _{std}
		t _{PHL}	0.388 + 0.002N _{std}	0.299 + 0.001N _{std}	0.236 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.620 + 0.002N _{std}	0.448 + 0.001N _{std}	0.363 + 0.001N _{std}
		t _{PHL}	0.546 + 0.002N _{std}	0.442 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.440 + 0.002N _{std}	0.305 + 0.001N _{std}	0.233 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.625 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.440 + 0.002N _{std}	0.305 + 0.001N _{std}	0.233 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.625 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.243	11.243	11.243
DI	7.651	7.652	7.650
PAD (Receiver Input)	538.083	538.083	538.083
RG	2.002	2.002	2.002
RI	3.524	3.524	3.524
TS	6.499	6.499	6.499
Internal	426.353	417.656	416.099
Cell Units	1 cell	1 cell	1 cell

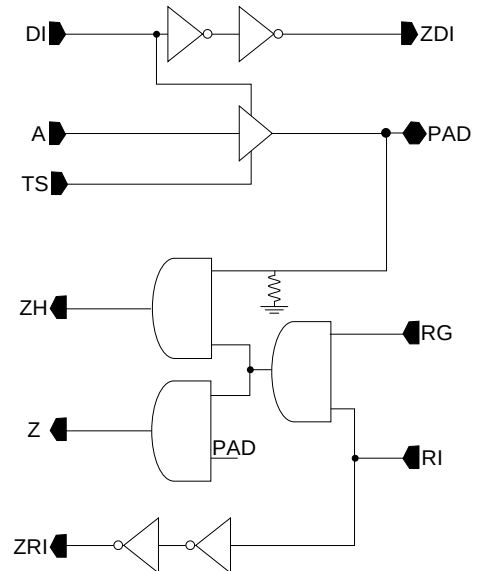
Cell: BC2535PD, BC2535PD_PM

Function: 2.5V CMOS Nontest 35 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
L	1	1	0	0	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.619 + 0.031D _{std}	1.176 + 0.023D _{std}	0.867 + 0.019D _{std}
		t _{PHL}	1.584 + 0.032D _{std}	1.150 + 0.023D _{std}	0.852 + 0.019D _{std}
	B	t _{PLH}	1.475 + 0.029D _{std}	1.064 + 0.022D _{std}	0.798 + 0.018D _{std}
		t _{PHL}	1.436 + 0.030D _{std}	1.041 + 0.022D _{std}	0.784 + 0.018D _{std}
	C	t _{PLH}	1.293 + 0.029D _{std}	0.909 + 0.022D _{std}	0.678 + 0.018D _{std}
		t _{PHL}	1.273 + 0.030D _{std}	0.906 + 0.021D _{std}	0.676 + 0.017D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.436 + 0.002N _{std}	0.307 + 0.001N _{std}	0.237 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.388 + 0.002N _{std}	0.299 + 0.001N _{std}	0.237 + 0.001N _{std}
		t _{PLH}	0.620 + 0.002N _{std}	0.449 + 0.001N _{std}	0.363 + 0.001N _{std}
		t _{PHL}	0.547 + 0.002N _{std}	0.442 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PLH}	0.625 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PLH}	0.625 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.230	11.244	11.243
DI	7.651	7.652	7.661
PAD (Receiver Input)	491.625	491.625	491.625
RG	2.002	2.002	2.002
RI	3.525	3.525	3.524
TS	6.499	6.499	6.499
Internal	539.602	539.594	538.313
Cell Units	1 cell	1 cell	1 cell

Cell: BC2550PD, BC2550PD_PM

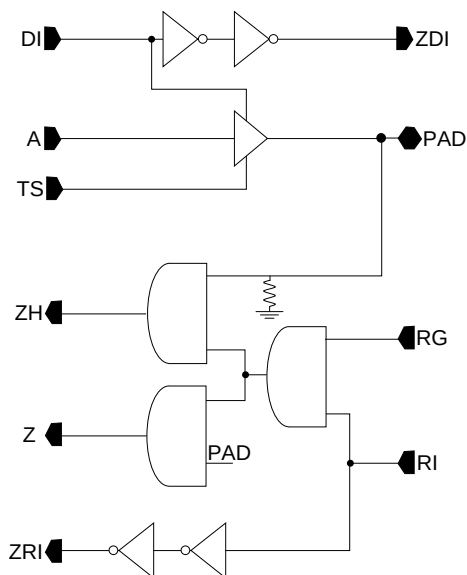
Function: 2.5V CMOS Nontest 50 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
L	1	1	0	0	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.583 + 0.041D _{std}	1.158 + 0.032D _{std}	0.860 + 0.027D _{std}
		t _{PHL}	1.548 + 0.042D _{std}	1.126 + 0.031D _{std}	0.837 + 0.026D _{std}
	B	t _{PLH}	1.422 + 0.040D _{std}	1.050 + 0.031D _{std}	0.801 + 0.026D _{std}
		t _{PHL}	1.383 + 0.041D _{std}	1.023 + 0.030D _{std}	0.784 + 0.025D _{std}
	C	t _{PLH}	1.238 + 0.040D _{std}	0.892 + 0.030D _{std}	0.683 + 0.026D _{std}
		t _{PHL}	1.217 + 0.040D _{std}	0.886 + 0.029D _{std}	0.675 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.436 + 0.002N _{std}	0.307 + 0.001N _{std}	0.237 + 0.001N _{std}
		t _{PHL}	0.388 + 0.002N _{std}	0.299 + 0.001N _{std}	0.237 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.620 + 0.002N _{std}	0.449 + 0.001N _{std}	0.363 + 0.001N _{std}
t _{PHL}		0.547 + 0.002N _{std}	0.442 + 0.001N _{std}	0.362 + 0.001N _{std}	
PAD-Z	B	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.626 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.626 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.243	11.243	11.243
DI	7.651	7.652	7.661
PAD (Receiver Input)	464.083	464.125	464.083
RG	2.002	2.002	2.002
RI	3.525	3.525	3.525
TS	6.499	6.499	6.499
Internal	643.393	645.345	646.491
Cell Units	1 cell	1 cell	1 cell

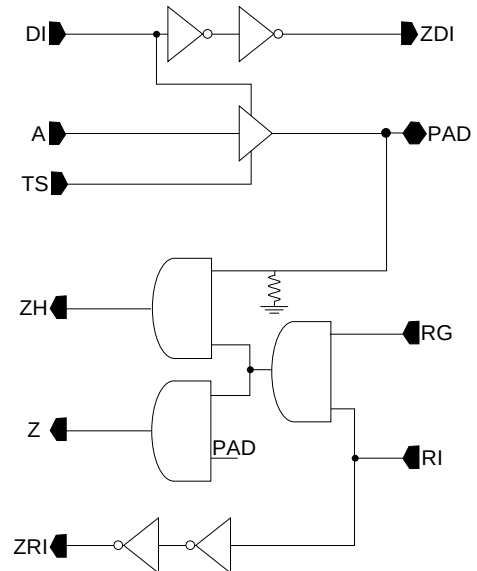
Cell: BC2565PD, BC2565PD_PM

Function: 2.5V CMOS Nontest 65 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
L	1	1	0	0	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.564 + 0.052D _{std}	1.148 + 0.040D _{std}	0.858 + 0.034D _{std}
		t _{PHL}	1.538 + 0.051D _{std}	1.113 + 0.039D _{std}	0.830 + 0.033D _{std}
	B	t _{PLH}	1.380 + 0.051D _{std}	1.044 + 0.039D _{std}	0.807 + 0.034D _{std}
		t _{PHL}	1.348 + 0.051D _{std}	1.018 + 0.038D _{std}	0.793 + 0.032D _{std}
	C	t _{PLH}	1.198 + 0.051D _{std}	0.885 + 0.039D _{std}	0.687 + 0.034D _{std}
		t _{PHL}	1.182 + 0.050D _{std}	0.875 + 0.038D _{std}	0.678 + 0.032D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.436 + 0.002N _{std}	0.307 + 0.001N _{std}	0.237 + 0.001N _{std}
		t _{PHL}	0.388 + 0.002N _{std}	0.299 + 0.001N _{std}	0.237 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.620 + 0.002N _{std}	0.449 + 0.001N _{std}	0.363 + 0.001N _{std}
		t _{PHL}	0.547 + 0.002N _{std}	0.443 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.625 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.625 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.243	11.243	11.244
DI	7.651	7.652	7.661
PAD (Receiver Input)	452.625	452.625	452.625
RG	2.002	2.002	2.002
RI	3.524	3.524	3.524
TS	6.499	6.499	6.499
Internal	739.221	741.969	741.656
Cell Units	1 cell	1 cell	1 cell

Cell: BC2590PD, BC2590PD_PM

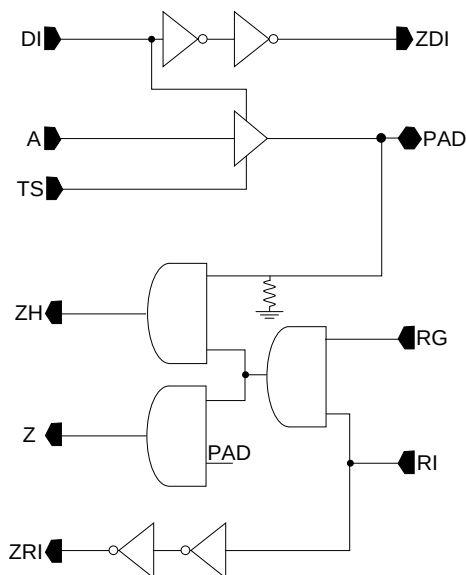
Function: 2.5V CMOS Nontest 90 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
L	1	1	0	0	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.357 + 0.074D _{std}	0.980 + 0.057D _{std}	0.729 + 0.048D _{std}
		t _{PHL}	1.377 + 0.073D _{std}	1.000 + 0.054D _{std}	0.739 + 0.045D _{std}
	B	t _{PLH}	1.210 + 0.074D _{std}	0.923 + 0.056D _{std}	0.721 + 0.048D _{std}
		t _{PHL}	1.305 + 0.071D _{std}	1.002 + 0.052D _{std}	0.782 + 0.044D _{std}
	C	t _{PLH}	1.039 + 0.074D _{std}	0.776 + 0.056D _{std}	0.612 + 0.047D _{std}
		t _{PHL}	1.114 + 0.071D _{std}	0.848 + 0.052D _{std}	0.663 + 0.044D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.436 + 0.002N _{std}	0.307 + 0.001N _{std}	0.237 + 0.001N _{std}
		t _{PHL}	0.388 + 0.002N _{std}	0.299 + 0.001N _{std}	0.237 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.620 + 0.002N _{std}	0.449 + 0.001N _{std}	0.363 + 0.001N _{std}
t _{PHL}		0.547 + 0.002N _{std}	0.442 + 0.001N _{std}	0.362 + 0.001N _{std}	
PAD-Z	B	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.625 + 0.002N _{std}	0.451 + 0.001N _{std}	0.365 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.625 + 0.002N _{std}	0.451 + 0.001N _{std}	0.365 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.243	11.242	11.242
DI	7.652	7.661	7.661
PAD (Receiver Input)	343.875	343.875	343.875
RG	2.002	2.002	2.002
RI	3.525	3.525	3.524
TS	6.499	6.500	6.499
Internal	832.000	844.000	836.000
Cell Units	1 cell	1 cell	1 cell

Cell: BC2520PU, BC2520PU_PM

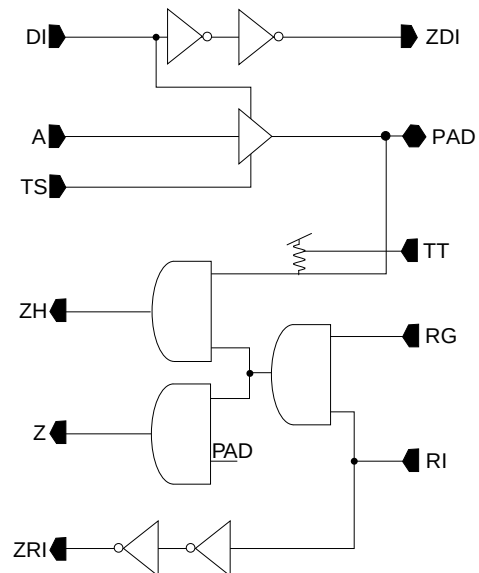
Function: 2.5V CMOS Nontest 20 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (2.5V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1,H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.642 + 0.021D_{std}$	$1.185 + 0.016D_{std}$	$0.873 + 0.013D_{std}$
		t_{PHL}	$1.630 + 0.023D_{std}$	$1.183 + 0.016D_{std}$	$0.876 + 0.013D_{std}$
	B	t_{PLH}	$1.522 + 0.019D_{std}$	$1.079 + 0.014D_{std}$	$0.792 + 0.011D_{std}$
		t_{PHL}	$1.498 + 0.021D_{std}$	$1.071 + 0.015D_{std}$	$0.796 + 0.012D_{std}$
	C	t_{PLH}	$1.348 + 0.018D_{std}$	$0.930 + 0.013D_{std}$	$0.679 + 0.010D_{std}$
		t_{PHL}	$1.339 + 0.020D_{std}$	$0.937 + 0.014D_{std}$	$0.687 + 0.011D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.419 + 0.002N _{std}	0.283 + 0.001N _{std}	0.210 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.403 + 0.002N _{std}	0.322 + 0.001N _{std}	0.263 + 0.001N _{std}
		t _{PLH}	0.604 + 0.002N _{std}	0.425 + 0.001N _{std}	0.336 + 0.001N _{std}
		t _{PHL}	0.561 + 0.002N _{std}	0.465 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.422 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
		t _{PLH}	0.613 + 0.002N _{std}	0.425 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.568 + 0.002N _{std}	0.471 + 0.001N _{std}	0.391 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.422 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
		t _{PLH}	0.613 + 0.002N _{std}	0.425 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.568 + 0.002N _{std}	0.471 + 0.001N _{std}	0.391 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	10.680	11.243	11.243
DI	7.150	7.652	7.653
PAD (Receiver Input)	537.625	537.625	537.625
RG	1.934	1.934	1.934
RI	3.426	3.426	3.426
TS	6.122	6.500	6.500
TT	4.117	4.302	4.302
Internal	310.829	308.482	309.045
Cell Units	1 cell	1 cell	1 cell

Cell: BC2535PU, BC2535PU_PM

Function: 2.5V CMOS Nontest 35 Ohm 3-State CIO w/Pull-Up

Description:

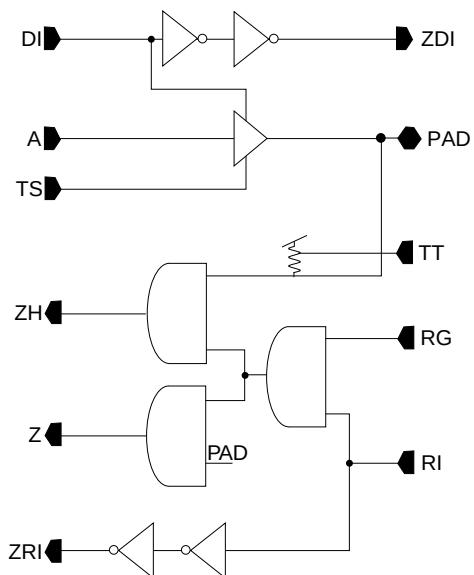
Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (2.5V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1,H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.611 + 0.031D _{std}	1.168 + 0.023D _{std}	0.861 + 0.019D _{std}
		t _{PHL}	1.593 + 0.032D _{std}	1.159 + 0.023D _{std}	0.859 + 0.019D _{std}
	B	t _{PLH}	1.469 + 0.029D _{std}	1.058 + 0.022D _{std}	0.793 + 0.018D _{std}
		t _{PHL}	1.441 + 0.031D _{std}	1.048 + 0.022D _{std}	0.789 + 0.018D _{std}
	C	t _{PLH}	1.290 + 0.028D _{std}	0.906 + 0.021D _{std}	0.675 + 0.018D _{std}
		t _{PHL}	1.275 + 0.030D _{std}	0.910 + 0.021D _{std}	0.680 + 0.018D _{std}



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.420 + 0.002N _{std}	0.283 + 0.001N _{std}	0.210 + 0.001N _{std}
		t _{PHL}	0.403 + 0.002N _{std}	0.322 + 0.001N _{std}	0.263 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.604 + 0.002N _{std}	0.425 + 0.001N _{std}	0.336 + 0.001N _{std}
		t _{PHL}	0.561 + 0.002N _{std}	0.465 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.425 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.425 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.471 + 0.001N _{std}	0.391 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.425 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.425 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.471 + 0.001N _{std}	0.391 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.230	11.244	11.230
DI	7.376	7.652	7.652
PAD (Receiver Input)	491.417	491.417	491.417
RG	2.002	2.002	2.002
RI	3.525	3.525	3.525
TS	6.329	6.504	6.504
TT	4.281	4.281	4.281
Internal	350.407	353.335	352.995
Cell Units	1 cell	1 cell	1 cell

Cell: BC2550PU, BC2550PU_PM

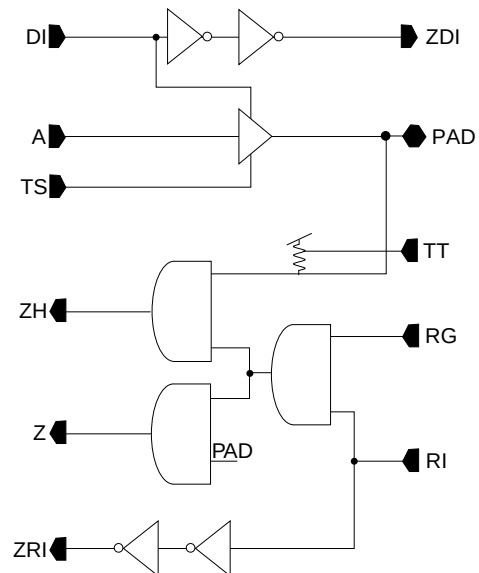
Function: 2.5V CMOS Nontest 50 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (2.5V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1,H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.575 + 0.041D_{std}$	$1.150 + 0.031D_{std}$	$0.853 + 0.026D_{std}$
		t_{PHL}	$1.553 + 0.042D_{std}$	$1.136 + 0.031D_{std}$	$0.844 + 0.026D_{std}$
	B	t_{PLH}	$1.417 + 0.040D_{std}$	$1.044 + 0.030D_{std}$	$0.795 + 0.025D_{std}$
		t_{PHL}	$1.387 + 0.041D_{std}$	$1.030 + 0.030D_{std}$	$0.791 + 0.025D_{std}$
	C	t_{PLH}	$1.237 + 0.039D_{std}$	$0.891 + 0.030D_{std}$	$0.674 + 0.025D_{std}$
		t_{PHL}	$1.220 + 0.041D_{std}$	$0.891 + 0.030D_{std}$	$0.680 + 0.025D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.420 + 0.002N _{std}	0.283 + 0.001N _{std}	0.210 + 0.001N _{std}
		t _{PHL}	0.403 + 0.002N _{std}	0.322 + 0.001N _{std}	0.263 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.604 + 0.002N _{std}	0.425 + 0.001N _{std}	0.336 + 0.001N _{std}
		t _{PHL}	0.561 + 0.002N _{std}	0.465 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.422 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.425 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.472 + 0.001N _{std}	0.391 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.422 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.425 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.471 + 0.001N _{std}	0.391 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.243	11.243	11.242
DI	7.651	7.652	7.651
PAD (Receiver Input)	463.833	463.792	463.833
RG	2.003	2.003	2.003
RI	3.525	3.524	3.524
TS	6.502	6.502	6.502
TT	4.302	4.302	4.302
Internal	387.510	390.957	392.701
Cell Units	1 cell	1 cell	1 cell

Cell: BC2565PU, BC2565PU_PM

Function: 2.5V CMOS Nontest 65 Ohm 3-State CIO w/Pull-Up

Description:

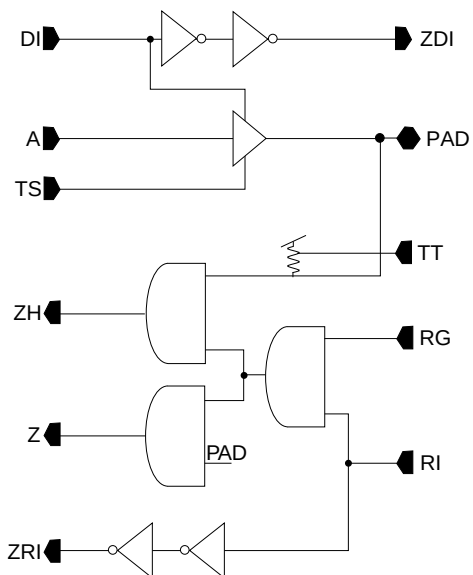
Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (2.5V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1,H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.556 + 0.051D _{std}	1.139 + 0.039D _{std}	0.850 + 0.033D _{std}
		t _{PHL}	1.546 + 0.052D _{std}	1.121 + 0.040D _{std}	0.838 + 0.034D _{std}
	B	t _{PLH}	1.377 + 0.050D _{std}	1.037 + 0.039D _{std}	0.808 + 0.033D _{std}
		t _{PHL}	1.351 + 0.051D _{std}	1.026 + 0.039D _{std}	0.803 + 0.033D _{std}
	C	t _{PLH}	1.196 + 0.050D _{std}	0.875 + 0.039D _{std}	0.679 + 0.033D _{std}
		t _{PHL}	1.182 + 0.051D _{std}	0.879 + 0.039D _{std}	0.684 + 0.033D _{std}



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.420 + 0.002N _{std}	0.283 + 0.001N _{std}	0.210 + 0.001N _{std}
		t _{PHL}	0.403 + 0.002N _{std}	0.322 + 0.001N _{std}	0.263 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.604 + 0.002N _{std}	0.425 + 0.001N _{std}	0.336 + 0.001N _{std}
		t _{PHL}	0.562 + 0.002N _{std}	0.465 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.423 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.426 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.472 + 0.001N _{std}	0.391 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.423 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.426 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.472 + 0.001N _{std}	0.391 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.244	11.243	11.243
DI	7.651	7.652	7.661
PAD (Receiver Input)	452.292	452.333	452.333
RG	2.003	2.003	2.003
RI	3.524	3.524	3.524
TS	6.502	6.502	6.502
TT	4.302	4.302	4.302
Internal	415.172	418.989	418.855
Cell Units	1 cell	1 cell	1 cell

Cell: BC2590PU, BC2590PU_PM

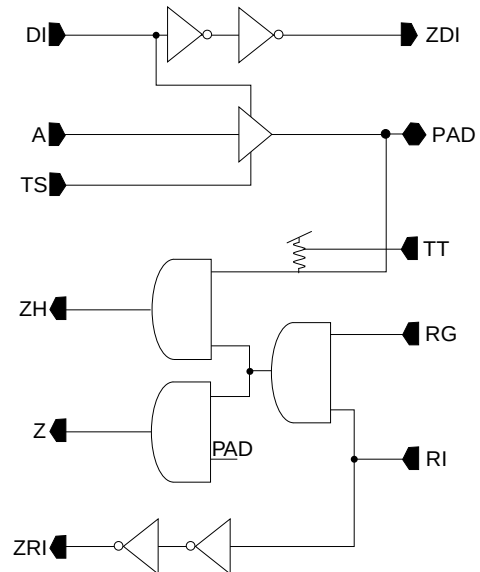
Function: 2.5V CMOS Nontest 90 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (2.5V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1,H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.344 + 0.072D_{std}$	$0.971 + 0.055D_{std}$	$0.721 + 0.046D_{std}$
		t_{PHL}	$1.388 + 0.075D_{std}$	$1.012 + 0.056D_{std}$	$0.751 + 0.047D_{std}$
	B	t_{PLH}	$1.206 + 0.072D_{std}$	$0.914 + 0.055D_{std}$	$0.712 + 0.046D_{std}$
		t_{PHL}	$1.308 + 0.074D_{std}$	$1.011 + 0.054D_{std}$	$0.799 + 0.046D_{std}$
	C	t_{PLH}	$1.040 + 0.072D_{std}$	$0.771 + 0.055D_{std}$	$0.604 + 0.046D_{std}$
		t_{PHL}	$1.115 + 0.073D_{std}$	$0.858 + 0.054D_{std}$	$0.674 + 0.046D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.420 + 0.002N _{std}	0.283 + 0.001N _{std}	0.210 + 0.001N _{std}
		t _{PHL}	0.403 + 0.002N _{std}	0.323 + 0.001N _{std}	0.263 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.604 + 0.002N _{std}	0.425 + 0.001N _{std}	0.336 + 0.001N _{std}
		t _{PHL}	0.562 + 0.002N _{std}	0.465 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.425 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.426 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.472 + 0.001N _{std}	0.391 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.425 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.426 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.472 + 0.001N _{std}	0.391 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.243	11.243	11.242
DI	7.661	7.661	7.661
PAD (Receiver Input)	343.750	343.750	343.750
RG	2.003	2.003	2.003
RI	3.524	3.524	3.525
TS	6.500	6.500	6.500
TT	4.302	4.302	4.302
Internal	832.000	844.000	836.000
Cell Units	1 cell	1 cell	1 cell

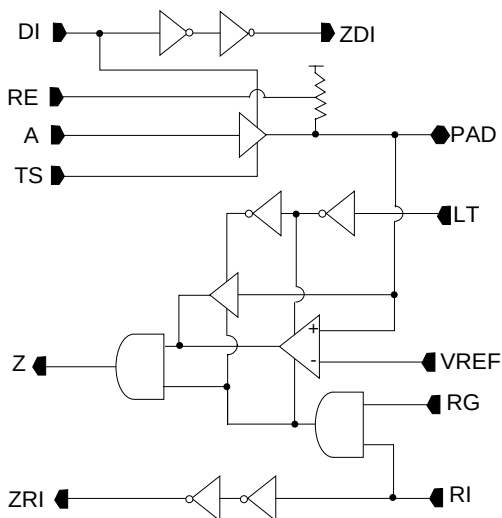
Cell: BGTLD, BGTLD_PM

Function: Nontest GTL CIO for Double Termination

Description:

Noninverting bidirectional driver/receiver with three-state control. Output di/dt and performance are chosen by performance level selection. Off-chip termination requires 25Ω to 1.2V or 1.5V (V_{TT}). On-chip termination is provided only for chip testing. Receiver requires (off chip) input reference ($2/3 \cdot V_{TT}$). RG and RI disable differential circuit within receiver to reduce power consumption. A, TS, and Z must be wired to latches for boundary scan. If RG is not used it should be tied to Vdd.

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RE	Reference enable input
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
LT	DC current gate (I_{dd} test) input
VREF	Voltage reference input
PAD	Driver output/receiver input
Z	Non-hysteresis receiver output
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)



Driver Truth Table

Inputs				Outputs	
A	TS	DI	RE	PAD	ZDI
-	0	-	-	Hi-Z ¹	DI
-	-	0	-	Hi-Z ¹	DI
1	1	1	0	Hi-Z ¹	DI
0	1	1	0	0	DI
1	1	1	1	1	DI
0	1	1	1	0	DI

¹. PAD is Hi-Z if driver is not externally terminated.

Notes:

- RE = 1 enables on-chip terminator (to V_{dd}).
- Timing model will be based on driver terminated off-chip (25Ω to V_{TT}).
- $V_{TT} = 1.2V$ (GTL); $V_{TT} = 1.5V$ (GTL+).

Receiver Truth Table

Inputs				Outputs		Comments
PAD	LT	RI	RG	Z	ZRI	
-	-	0	-	0	RI	Test mode
-	-	-	0	0	RI	Functional mode (user inhibit)
0 ¹	0	1	1	0	RI	Functional mode
1 ¹	0	1	1	1	RI	Functional mode
0 ²	1	1	1	0	RI	CMOS bypass
1 ²	1	1	1	1	RI	CMOS bypass

¹. PAD input requires GTL/GTL+ levels.

². PAD input requires CMOS levels.



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.111 + 0.020D _{std}	1.336 + 0.019D _{std}	1.247 + 0.020D _{std}
		t _{PHL}	1.527 + 0.010D _{std}	0.929 + 0.007D _{std}	0.603 + 0.005D _{std}
	B	t _{PLH}	0.674 + 0.018D _{std}	0.595 + 0.020D _{std}	0.531 + 0.020D _{std}
		t _{PHL}	1.056 + 0.008D _{std}	0.641 + 0.005D _{std}	0.414 + 0.004D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.574 + 0.001N _{std}	0.298 + 0.001N _{std}	0.193 + 0.001N _{std}
		t _{PHL}	0.624 + 0.001N _{std}	0.315 + 0.001N _{std}	0.206 + 0.001N _{std}
	B	t _{PLH}	0.586 + 0.001N _{std}	0.294 + 0.001N _{std}	0.187 + 0.001N _{std}
		t _{PHL}	0.626 + 0.001N _{std}	0.314 + 0.001N _{std}	0.203 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	8.484	15.978
DI	3.697	3.696
LT	2.909	2.909
PAD (Receiver Input)	371.000	373.083
RE	1.981	1.976
RG	4.374	4.374
RI	5.767	5.767
TS	2.656	2.657
VREF	218.425	218.425
Internal	431.664	440.428
Cell Units	1 cell	1 cell

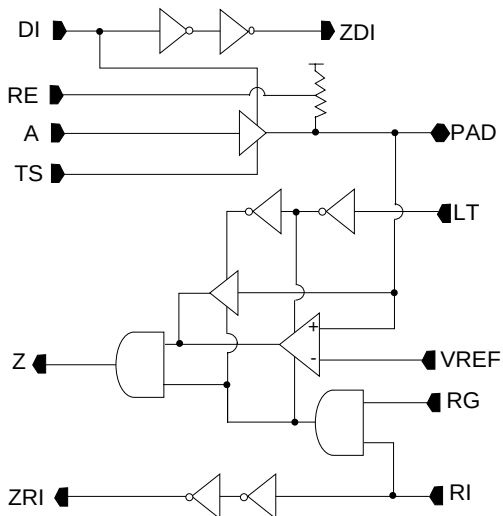
Cell: BGTLS, BGTLS_PM

Function: Nontest GTL CIO for Single Termination

Description:

Noninverting bidirectional driver/receiver with three-state control. Output di/dt and performance are chosen by performance level selection. Off-chip termination requires 50Ω to 1.2V or 1.5V (V_{TT}). On-chip termination is provided only for chip testing. Receiver requires (off chip) input reference ($2/3 \cdot V_{TT}$). RG and RI disable differential circuit within receiver to reduce power consumption. A, TS, and Z must be wired to latches for boundary scan. If RG is not used it should be tied to Vdd.

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RE	Reference enable input
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
LT	DC current gate (I_{dd} test) input
VREF	Voltage reference input
PAD	Driver output/receiver input
Z	Non-hysteresis receiver output
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)



Driver Truth Table

Inputs				Outputs	
A	TS	DI	RE	PAD	ZDI
-	0	-	-	Hi-Z ¹	DI
-	-	0	-	Hi-Z ¹	DI
1	1	1	0	Hi-Z ¹	DI
0	1	1	0	0	DI
1	1	1	1	1	DI
0	1	1	1	0	DI

¹. PAD is Hi-Z if driver is not externally terminated.

Notes:

- RE = 1 enables on-chip terminator (to V_{dd}).
- Timing model will be based on driver terminated off-chip (50Ω to V_{TT}).
- $V_{TT} = 1.2V$ (GTL); $V_{TT} = 1.5V$ (GTL+).

Receiver Truth Table

Inputs				Outputs		Comments
PAD	LT	RI	RG	Z	ZRI	
-	-	0	-	0	RI	Test mode
-	-	-	0	0	RI	Functional mode (user inhibit)
0 ¹	0	1	1	0	RI	Functional mode
1 ¹	0	1	1	1	RI	Functional mode
0 ²	1	1	1	0	RI	CMOS bypass
1 ²	1	1	1	1	RI	CMOS bypass

¹. PAD input requires GTL/GTL+ levels.

². PAD input requires CMOS levels.



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$0.514 + 0.038D_{std}$	$0.462 + 0.042D_{std}$	$0.407 + 0.043D_{std}$
		t_{PHL}	$0.967 + 0.013D_{std}$	$0.632 + 0.009D_{std}$	$0.432 + 0.007D_{std}$
	B	t_{PLH}	$0.439 + 0.038D_{std}$	$0.352 + 0.043D_{std}$	$0.380 + 0.044D_{std}$
		t_{PHL}	$0.730 + 0.011D_{std}$	$0.470 + 0.007D_{std}$	$0.317 + 0.005D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.574 + 0.001N_{std}$	$0.300 + 0.001N_{std}$	$0.192 + 0.001N_{std}$
		t_{PHL}	$0.625 + 0.001N_{std}$	$0.315 + 0.001N_{std}$	$0.209 + 0.001N_{std}$
	B	t_{PLH}	$0.585 + 0.001N_{std}$	$0.294 + 0.001N_{std}$	$0.187 + 0.001N_{std}$
		t_{PHL}	$0.626 + 0.001N_{std}$	$0.314 + 0.001N_{std}$	$0.203 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

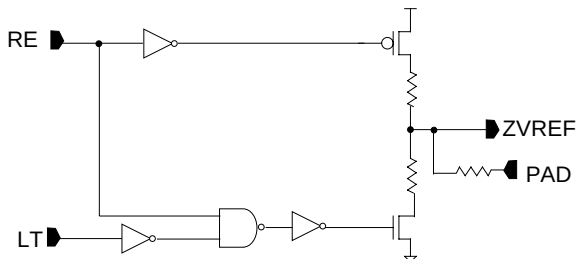
Input Pins	Performance Level	
	A	B
A	14.642	14.049
DI	3.703	3.704
LT	2.909	2.909
PAD (Receiver Input)	441.083	440.750
RE	1.982	1.983
RG	4.374	4.374
RI	5.767	5.767
TS	2.657	2.657
VREF	218.425	218.425
Internal	453.626	465.903
Cell Units	1 cell	1 cell

Cell: VGTLR1, VGTLR1_PM

Function: GTL Voltage Reference Receiver

Description:

This cell generates an on-chip reference voltage, VREF ($2 \cdot V_{TT}/3$, where $V_{TT} = 1.5V$) to the input of GTL receivers during test. At system mode, the reference is disabled ($RE = 0$) to apply an external reference voltage through the PAD pin.



RE Reference enable input

LT DC current gate (I_{dd} test) input

PAD Connection to package pin for off-chip supplied VREF

ZVREF Reference voltage (out)

Driver Truth Table

Inputs			Output	Comments
PAD	LT	RE	ZVREF	
-	0	1	X	ZVREF = Internal reference voltage used during wafer test
-	1	1	X	ZVREF = Internal V_{dd}
-	-	0	X	ZVREF = External reference voltage

Notes:

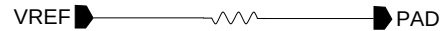
- PAD is hard-wired to VREF. Resistance between PAD and VREF is negligible. External reference voltage can be applied to PAD only when $RE = 0$.
- This cell is NOT ALLOWED in 64 test pin locations.

Cell: VGTLR2, VGTLR2_PM

Function: Supplemental GTL+ Voltage Reference Pin (VREF Driver)

Description:

This cell provides additional PAD for external reference voltage. Additional pads are required to stabilize reference voltage due to noise. A minimum of one is recommended.



VREF Reference voltage

PAD Off-chip supplied reference voltage

Driver Truth Table

Input	Output	Comments
VREF	PAD	
-	X	Supplemental external VREF pin

Notes:

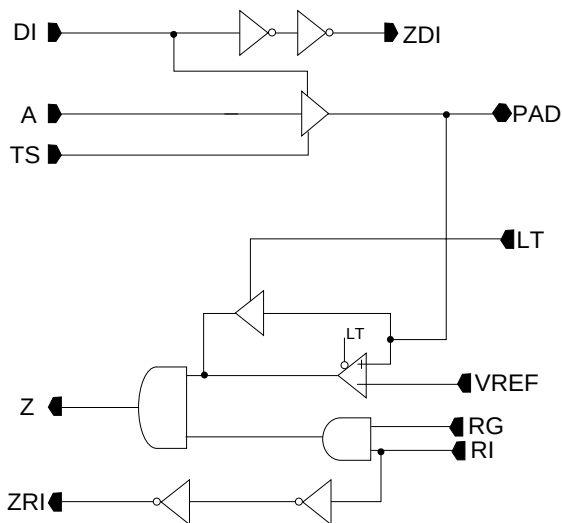
- a. This cell is NOT ALLOWED in 64 test pin locations.
- b. PAD is electrically hard-wired to VREF. It is used as a supplementary external VREF pin. Customer can provide as many pins on the chip as required.

Cell: BHSTL18C1, BHSTL18C1_PM
Function: HSTL 1.8V Class 1 Nontest CIO

Description:

Noninverting bidirectional driver/receiver.
Off-chip termination requires 50 ohms to $V_{ddq}/2$, where $V_{ddq} = V_{dd}$. Receiver requires (off-chip) input reference ($V_{ddq}/2$).

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
LT DC current gate (I_{dd} test) input
RI Receiver inhibit input (RI in)
RG Receiver gate control
VREF Voltage reference input
PAD Driver output/receiver input
ZDI Driver inhibit output (DI out)
ZRI Receiver inhibit output (RI out)
Z Receiver output



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	0	-	Hi-Z ¹	DI
-	-	0	Hi-Z ¹	DI
-	1	1	A	DI

¹. PAD is Hi-Z if driver is not externally terminated. PAD is at " $V_{ddq}/2$ " if driver is terminated (off-chip).

Notes:

- Logical "1" = $V_{ddq} = V_{dd} = 1.8V$.
- Timing model will be based on driver terminated off-chip.

Receiver Truth Table

Inputs					Outputs		Comments
PAD	LT	RI	RG	VREF	Z	ZRI	
-	-	-	0	-	0	RI	Test mode
-	-	0	-	-	0	RI	Test mode
1 ¹	0	1	1	-	1	RI	Functional mode
0 ²	0	1	1	-	0	RI	Functional mode
1 ³	1	1	1	-	1	RI	Bypass mode
0 ⁴	1	1	1	-	0	RI	Bypass mode

1. PAD input requires HSTL level "high" and $V_{ddq} < V_{dd}$.
2. PAD input requires HSTL level "low."
3. PAD input requires CMOS level "high" and $V_{ddq} = V_{dd}$.
4. PAD input requires CMOS level "low."

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$0.564 + 0.020D_{std}$	$0.449 + 0.016D_{std}$	$0.357 + 0.014D_{std}$
		t_{PHL}	$0.525 + 0.020D_{std}$	$0.408 + 0.015D_{std}$	$0.323 + 0.013D_{std}$
	B	t_{PLH}	$0.473 + 0.018D_{std}$	$0.376 + 0.015D_{std}$	$0.305 + 0.013D_{std}$
		t_{PHL}	$0.430 + 0.019D_{std}$	$0.339 + 0.015D_{std}$	$0.278 + 0.013D_{std}$



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.397 + 0.001N _{std}	0.266 + 0.001N _{std}	0.192 + 0.000N _{std}
		t _{PHL}	0.413 + 0.001N _{std}	0.266 + 0.001N _{std}	0.174 + 0.000N _{std}
	B	t _{PLH}	0.393 + 0.001N _{std}	0.267 + 0.001N _{std}	0.196 + 0.000N _{std}
		t _{PHL}	0.404 + 0.001N _{std}	0.265 + 0.001N _{std}	0.176 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	24.883	24.908
DI	3.542	3.541
LT	3.081	3.093
PAD (Receiver Input)	355.917	354.917
RG	6.690	6.690
RI	5.678	5.678
TS	2.988	2.988
VREF	109.442	109.442
Internal	206.276	210.959
Cell Units	1 cell	1 cell

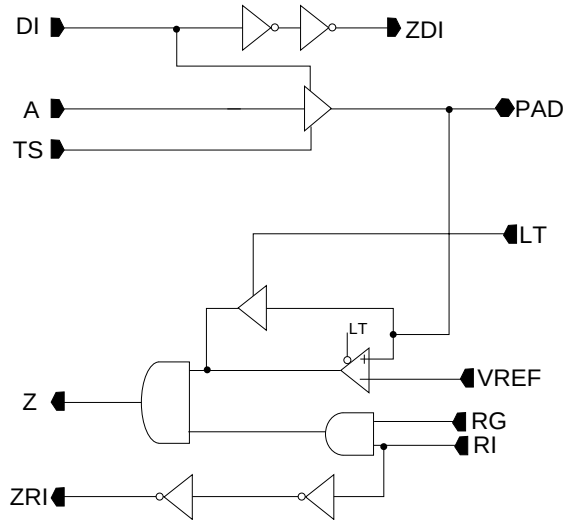
Cell: BHSTL18C2, BHSTL18C2_PM

Function: HSTL 1.8V Class 2 Nontest CIO

Description:

Noninverting bidirectional driver/receiver. Off-chip termination requires 25 ohms to $V_{ddq}/2$, where $V_{ddq} = V_{dd}$. Receiver requires (off-chip) input reference ($V_{ddq}/2$).

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
LT	DC current gate (I_{dd} test) input
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
VREF	Voltage reference input
PAD	Driver output/receiver input
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)
Z	Receiver output



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	0	-	Hi-Z ¹	DI
-	-	0	Hi-Z ¹	DI
-	1	1	A	DI

¹. PAD is Hi-Z if driver is not externally terminated. PAD is at " $V_{ddq}/2$ " if driver is terminated (off-chip).

Notes:

- Logical "1" = $V_{ddq} = V_{dd} = 1.8V$.
- Timing model will be based on driver terminated off-chip.



Receiver Truth Table

Inputs					Outputs		Comments
PAD	LT	RI	RG	VREF	Z	ZRI	
-	-	-	0	-	0	RI	Test mode
-	-	0	-	-	0	RI	Test mode
1 ¹	0	1	1	-	1	RI	Functional mode
0 ²	0	1	1	-	0	RI	Functional mode
1 ³	1	1	1	-	1	RI	Bypass mode
0 ⁴	1	1	1	-	0	RI	Bypass mode

1. PAD input requires HSTL level "high" and $V_{ddq} < V_{dd}$.

2. PAD input requires HSTL level "low."

3. PAD input requires CMOS level "high" and $V_{ddq} = V_{dd}$.

4. PAD input requires CMOS level "low."

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$0.571 + 0.013D_{std}$	$0.466 + 0.011D_{std}$	$0.373 + 0.009D_{std}$
		t_{PHL}	$0.627 + 0.013D_{std}$	$0.462 + 0.010D_{std}$	$0.349 + 0.008D_{std}$
	B	t_{PLH}	$0.524 + 0.011D_{std}$	$0.420 + 0.009D_{std}$	$0.340 + 0.008D_{std}$
		t_{PHL}	$0.505 + 0.012D_{std}$	$0.389 + 0.009D_{std}$	$0.309 + 0.008D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.397 + 0.001N_{std}$	$0.266 + 0.001N_{std}$	$0.192 + 0.000N_{std}$
		t_{PHL}	$0.413 + 0.001N_{std}$	$0.266 + 0.001N_{std}$	$0.174 + 0.000N_{std}$
	B	t_{PLH}	$0.393 + 0.001N_{std}$	$0.267 + 0.001N_{std}$	$0.195 + 0.000N_{std}$
		t_{PHL}	$0.404 + 0.001N_{std}$	$0.265 + 0.001N_{std}$	$0.176 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

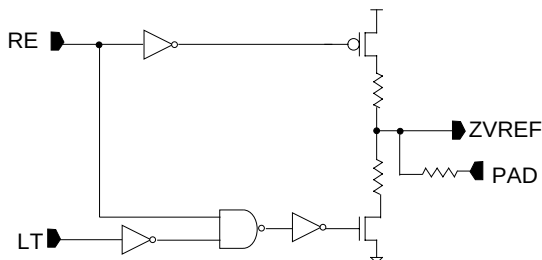
Input Pins	Performance Level	
	A	B
A	19.148	21.023
DI	3.551	3.549
LT	3.121	3.121
PAD (Receiver Input)	399.833	399.875
RG	6.691	6.691
RI	5.678	5.678
TS	2.992	2.989
VREF	109.450	109.450
Internal	200.395	220.741
Cell Units	1 cell	1 cell

Cell: VHSTL18R1, VHSTL18R1_PM
Function: Voltage Reference Receiver

Description:

This cell generates a precision on-chip reference voltage ($V_{dd}/2$). At system mode, the reference may be disabled ($RE = 0$) to apply an external reference voltage through the PAD pin, or the on-chip reference generator may remain enabled ($RE = 1$). When enabled, the reference generator requires 1.0 mA of current.

RE Reference enable input
LT DC current gate (I_{dd} test) input
PAD Connection to package pin
ZVREF Reference voltage



Driver Truth Table

Inputs			Output	Comments
PAD	LT	RE	ZVREF	
-	0	1	X	ZVREF = $0.5 * V_{dd}$; used during wafer test
-	1	1	X	ZVREF = V_{dd}
-	-	0	X	Reference generator is Hi-Z; used during packaged device test

Notes:

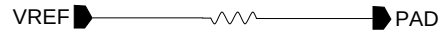
- Resistance between PAD and VREF is negligible.
- This cell is NOT ALLOWED in 64 test pin locations.

Cell: VHSTL18R2, VHSTL18R2_PM

Function: Supplemental 1.8V HSTL Voltage Reference Pin (VREF Driver)

Description:

This cell provides additional PAD for external reference voltage. Additional pads are required to stabilize reference voltage due to noise. A minimum of one is recommended.



VREF Reference voltage

PAD Off-chip supplied reference voltage

Driver Truth Table

Input	Output	Comments
VREF	PAD	
-	X	Supplemental external VREF pin

Notes:

- This cell is NOT ALLOWED in 64 test pin locations.
- PAD is electrically hard-wired to VREF. It is used as a supplementary external VREF pin. The customer can provide as many pins on the chip as required.

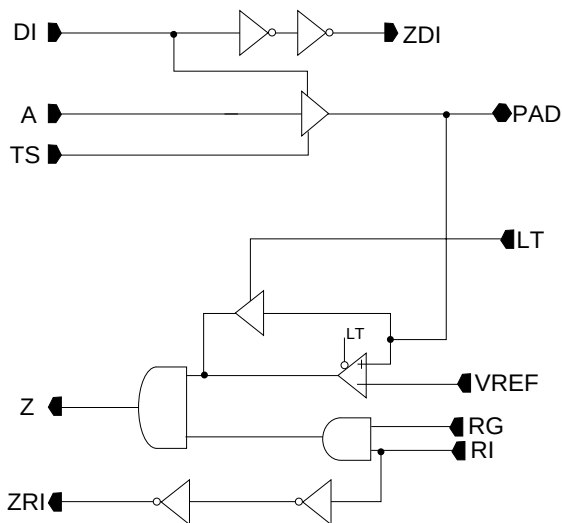
Cell: BHSTLC1, BHSTLC1_PM

Function: HSTL 1.5V Class 1 Nontest CIO

Description:

Noninverting bidirectional driver/receiver.
Off-chip termination requires 50 ohms to $V_{ddq}/2$, where $V_{ddq} = 1.5$. Receiver requires (off-chip) input reference ($V_{ddq}/2$).

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
LT DC current gate (I_{dd} test) input
RI Receiver inhibit input (RI in)
RG Receiver gate control
VREF Voltage reference input
PAD Driver output/receiver input
ZDI Driver inhibit output (DI out)
ZRI Receiver inhibit output (RI out)
Z Receiver output



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	0	-	Hi-Z ¹	DI
-	-	0	Hi-Z ¹	DI
-	1	1	A	DI

¹. PAD is Hi-Z if driver is not externally terminated. PAD is at " $V_{ddq}/2$ " if driver is terminated (off-chip).

Notes:

- Logical "1" = $V_{ddq} = 1.5V$.
- Timing model will be based on driver terminated off-chip.

Receiver Truth Table

Inputs					Outputs		Comments
PAD	LT	RI	RG	VREF	Z	ZRI	
-	-	-	0	-	0	RI	Test mode
-	-	0	-	-	0	RI	Test mode
1 ¹	0	1	1	-	1	RI	Functional mode
0 ²	0	1	1	-	0	RI	Functional mode
1 ³	1	1	1	-	1	RI	Bypass mode
0 ⁴	1	1	1	-	0	RI	Bypass mode

1. PAD input requires HSTL level "high" and $V_{ddq} < V_{dd}$.
2. PAD input requires HSTL level "low."
3. PAD input requires CMOS level "high" and $V_{ddq} = V_{dd}$.
4. PAD input requires CMOS level "low."

Note: A VREF signal of 0.75V must be applied through the VHSTLR1_A and VHSTLR2_A cells.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd150} = 1.4V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd150} = 1.5V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd150} = 1.6V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$0.535 + 0.019D_{std}$	$0.430 + 0.016D_{std}$	$0.345 + 0.014D_{std}$
		t_{PHL}	$0.496 + 0.019D_{std}$	$0.382 + 0.015D_{std}$	$0.299 + 0.013D_{std}$
	B	t_{PLH}	$0.449 + 0.018D_{std}$	$0.360 + 0.015D_{std}$	$0.295 + 0.013D_{std}$
		t_{PHL}	$0.410 + 0.018D_{std}$	$0.320 + 0.015D_{std}$	$0.261 + 0.013D_{std}$



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.405 + 0.001N _{std}	0.265 + 0.001N _{std}	0.172 + 0.000N _{std}
		t _{PHL}	0.491 + 0.001N _{std}	0.318 + 0.001N _{std}	0.221 + 0.000N _{std}
	B	t _{PLH}	0.406 + 0.001N _{std}	0.266 + 0.001N _{std}	0.171 + 0.000N _{std}
		t _{PHL}	0.488 + 0.001N _{std}	0.324 + 0.001N _{std}	0.227 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	30.062	29.854
DI	3.734	3.734
LT	3.226	3.227
PAD (Receiver Input)	371.542	371.750
RG	7.115	7.115
RI	5.978	5.978
TS	3.124	3.124
VREF	111.975	111.975
Internal	226.611	229.132
Cell Units	1 cell	1 cell

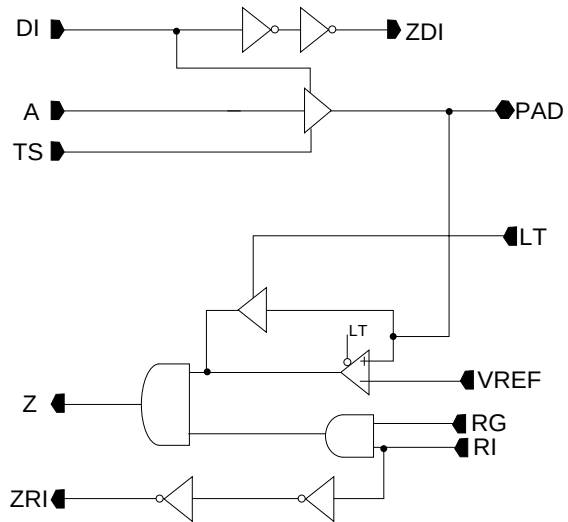
Cell: BHSTLC2, BHSTLC2_PM

Function: HSTL 1.5V Class 2 Nontest CIO

Description:

Noninverting bidirectional driver/receiver.
Off-chip termination requires 25 ohms to $V_{ddq}/2$, where $V_{ddq} = 1.5$. Receiver requires (off-chip) input reference ($V_{ddq}/2$).

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
LT DC current gate (I_{dd} test) input
RI Receiver inhibit input (RI in)
RG Receiver gate control
VREF Voltage reference input
PAD Driver output/receiver input
ZDI Driver inhibit output (DI out)
ZRI Receiver inhibit output (RI out)
Z Receiver output



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	0	-	Hi-Z ¹	DI
-	-	0	Hi-Z ¹	DI
-	1	1	A	DI

¹. PAD is Hi-Z if driver is not externally terminated. PAD is at " $V_{ddq}/2$ " if driver is terminated (off-chip).

Notes:

- Logical "1" = $V_{ddq} = 1.5V$.
- Timing model will be based on driver terminated off-chip.



Receiver Truth Table

Inputs					Outputs		Comments
PAD	LT	RI	RG	VREF	Z	ZRI	
-	-	-	0	-	0	RI	Test mode
-	-	0	-	-	0	RI	Test mode
1 ¹	0	1	1	-	1	RI	Functional mode
0 ²	0	1	1	-	0	RI	Functional mode
1 ³	1	1	1	-	1	RI	Bypass mode
0 ⁴	1	1	1	-	0	RI	Bypass mode

1. PAD input requires HSTL level "high" and $V_{ddq} < V_{dd}$.

2. PAD input requires HSTL level "low."

3. PAD input requires CMOS level "high" and $V_{ddq} = V_{dd}$.

4. PAD input requires CMOS level "low."

Note: A VREF signal of 0.75V must be applied through the VHSTLR1_A and VHSTLR2_A cells.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd150} = 1.4V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd150} = 1.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd150} = 1.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.225 + 0.014D_{std}$	$0.841 + 0.013D_{std}$	$0.645 + 0.011D_{std}$
		t_{PHL}	$1.026 + 0.011D_{std}$	$0.706 + 0.008D_{std}$	$0.511 + 0.007D_{std}$
	B	t_{PLH}	$1.009 + 0.011D_{std}$	$0.702 + 0.010D_{std}$	$0.538 + 0.009D_{std}$
		t_{PHL}	$0.902 + 0.010D_{std}$	$0.633 + 0.008D_{std}$	$0.472 + 0.007D_{std}$



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.405 + 0.001N_{std}$	$0.265 + 0.001N_{std}$	$0.172 + 0.000N_{std}$
		t_{PHL}	$0.491 + 0.001N_{std}$	$0.318 + 0.001N_{std}$	$0.221 + 0.000N_{std}$
	B	t_{PLH}	$0.406 + 0.001N_{std}$	$0.266 + 0.001N_{std}$	$0.171 + 0.000N_{std}$
		t_{PHL}	$0.488 + 0.001N_{std}$	$0.324 + 0.001N_{std}$	$0.227 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

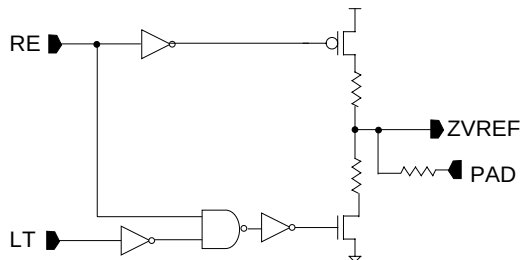
Input Pins	Performance Level	
	A	B
A	11.298	13.837
DI	3.742	3.742
LT	3.227	3.217
PAD (Receiver Input)	416.583	416.583
RG	7.097	7.115
RI	5.978	5.978
TS	3.129	3.128
VREF	111.975	111.975
Internal	302.186	377.388
Cell Units	1 cell	1 cell

Cell: VHSTLR1, VHSTLR1_PM

Function: Voltage Reference Receiver

Description:

This cell generates a precision on-chip reference voltage ($V_{dd}/2$). At system mode, the reference may be disabled ($RE = 0$) to apply an external reference voltage through the PAD pin, or the on-chip reference generator may remain enabled ($RE = 1$). When enabled, the reference generator requires 1.0 mA of current.



RE Reference enable input

LT DC current gate (I_{dd} test) input

PAD Connection to package pin

ZVREF Reference voltage

Driver Truth Table

Inputs			Output	Comments
PAD	LT	RE	ZVREF	
-	0	1	X	$ZVREF = 0.5 * V_{dd}$; used during wafer test
-	1	1	X	$ZVREF = V_{dd}$
-	-	0	X	Reference generator is Hi-Z; used during packaged device test

Notes:

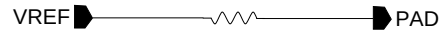
- Resistance between PAD and VREF is negligible.
- This cell is NOT ALLOWED in 64 test pin locations.

Cell: VHSTLR2, VHSTLR2_PM

Function: Supplemental 1.5V HSTL Voltage Reference Pin (VREF Driver)

Description:

This cell provides additional PAD for external reference voltage. Additional pads are required to stabilize reference voltage due to noise. A minimum of one is recommended.



VREF Reference voltage

PAD Off-chip supplied reference voltage

Driver Truth Table

Input	Output	Comments
VREF	PAD	
-	X	Supplemental external VREF pin

Notes:

- This cell is NOT ALLOWED in 64 test pin locations.
- PAD is electrically hard-wired to VREF. It is used as a supplementary external VREF pin. The customer can provide as many pins on the chip as required.

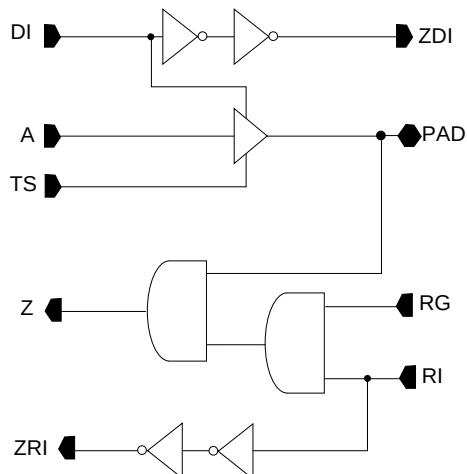
Cell: BI2C25, BI2C25_PM

Function: 2.5V Nontest I²C CIO

Description:

Noninverting driver/hysteresis receiver that interfaces 1.8V internal functions with I²C bus voltages not greater than 2.7V. Minimum off-chip termination of 767Ω to 2.5V is required for I²C bus application. For I²C applications, the driver is used as an open drain driver by holding the A input low and using the TS input to let the output be pulled high when TS is logical 0 and to drive the output low when TS is a logical 1. This I/O is intended for standard and fast mode I²C applications and will not meet high speed mode requirements. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd}.

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
PAD	Driver output/receiver input
Z	Hysteresis receiver output
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z ¹	DI
-	0	-	Hi-Z ¹	DI
0	1	1	0	DI
1	1	1	1	DI

¹. For I²C applications in which PAD is externally terminated with a pull-up resistor, PAD will be pulled to the termination voltage. Timing models will be based on off-chip driver termination of 767Ω to 2.5V. Timing for other pull-up applications must be determined using HSPICE or equivalent.

Receiver Truth Table

Inputs			Outputs	
PAD	RI	RG	Z	ZRI
-	0	-	0	RI
-	-	0	0	RI
0	1	1	0	RI
1	1	1	1	RI
Hi-Z	1	1	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	3.219 + 0.058D _{std}	2.167 + 0.044D _{std}	1.559 + 0.035D _{std}
		t _{PHL}	95.623 + 0.163D _{std}	64.680 + 0.088D _{std}	42.160 + 0.049D _{std}



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	3.054 + 0.002N _{std}	2.257 + 0.001N _{std}	1.997 + 0.001N _{std}
		t _{PHL}	3.717 + 0.002N _{std}	3.881 + 0.001N _{std}	3.528 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

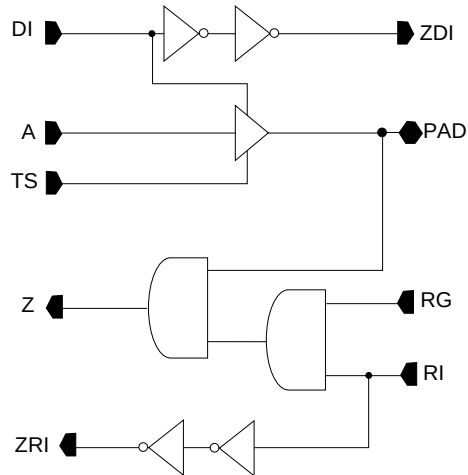
Input Pins	Performance Level
	A
A	11.461
DI	7.678
PAD (Receiver Input)	708.542
RG	2.005
RI	3.556
TS	6.655
Internal	1193.915
Cell Units	1 cell

Cell: BI2C33, BI2C33_PM
Function: 3.3V Nontest I²C CIO

Description:

Noninverting driver/hysteresis receiver that interfaces 1.8V internal functions with I²C bus voltages not greater than 3.6V. Minimum off chip termination of 1067Ω to 3.3V is required for I²C bus application. For I²C applications, the driver is used as an open drain driver by holding the A input low and using the TS input to let the output be pulled high when TS is a logical 1. This I/O is intended for standard and fast mode I²C applications and will not meet high speed mode requirements. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd}.

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
PAD	Driver output/receiver input
Z	Hysteresis receiver output
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)





Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z ¹	DI
-	0	-	Hi-Z ¹	DI
0	1	1	0	DI
1	1	1	1	DI

¹. For I²C applications in which PAD is externally terminated with a pull-up resistor, PAD will be pulled to the termination voltage. Timing models will be based on off-chip driver termination of 1067Ω to 3.3V. Timing for other pull-up applications must be determined using HSPICE or equivalent.

Receiver Truth Table

Inputs			Outputs	
PAD	RI	RG	Z	ZRI
-	0	-	0	RI
-	-	0	0	RI
0	1	1	0	RI
1	1	1	1	RI
Hi-Z	1	1	X	RI

Driver Propagation Delays

Path (Input to Output)	Perfor- mance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	3.191 + 0.062D _{std}	2.190 + 0.046D _{std}	1.671 + 0.038D _{std}
		t _{PHL}	117.072 + 0.167D _{std}	77.470 + 0.098D _{std}	53.462 + 0.057D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.243 + 0.002N _{std}	-0.474 + 0.001N _{std}	-0.865 + 0.001N _{std}
		t _{PHL}	4.229 + -0.001N _{std}	3.842 + -0.000N _{std}	4.124 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	12.763
DI	5.694
PAD (Receiver Input)	787.500
RG	2.052
RI	3.257
TS	4.368
Internal	1425.500
Cell Units	1 cell

Cell: BP2520, BP2520_PM

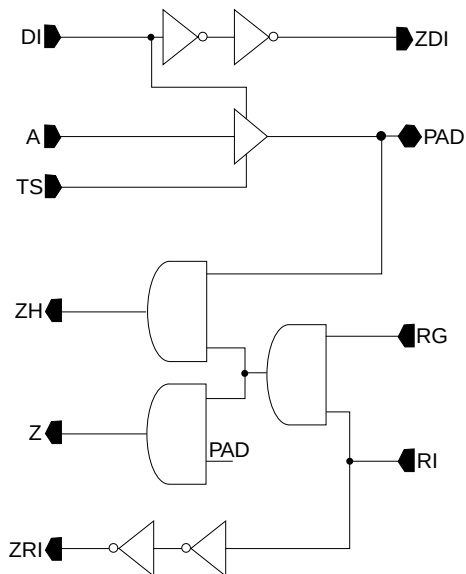
Function: 2.5V (3.3V Tolerant) CMOS Nontest 20 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses and is tolerant of 3.3V LVTTTL levels. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.519 + 0.021D _{std}	1.047 + 0.015D _{std}	0.760 + 0.012D _{std}
		t _{PHL}	1.557 + 0.026D _{std}	1.116 + 0.018D _{std}	0.838 + 0.014D _{std}
	B	t _{PLH}	1.308 + 0.019D _{std}	0.870 + 0.014D _{std}	0.631 + 0.011D _{std}
		t _{PHL}	1.261 + 0.023D _{std}	0.864 + 0.015D _{std}	0.635 + 0.012D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.291 + 0.001N _{std}	0.220 + 0.001N _{std}
		t _{PHL}	0.391 + 0.002N _{std}	0.309 + 0.001N _{std}	0.250 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.432 + 0.001N _{std}	0.345 + 0.001N _{std}
		t _{PHL}	0.548 + 0.002N _{std}	0.450 + 0.001N _{std}	0.373 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.430 + 0.002N _{std}	0.288 + 0.001N _{std}	0.214 + 0.001N _{std}
		t _{PHL}	0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.433 + 0.001N _{std}	0.344 + 0.001N _{std}
		t _{PHL}	0.555 + 0.002N _{std}	0.456 + 0.001N _{std}	0.375 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	10.626	10.536
DI	7.167	7.180
PAD (Receiver Input)	501.417	501.417
RG	1.933	1.933
RI	3.427	3.427
TS	6.174	6.172
Internal	495.708	492.654
Cell Units	1 cell	1 cell

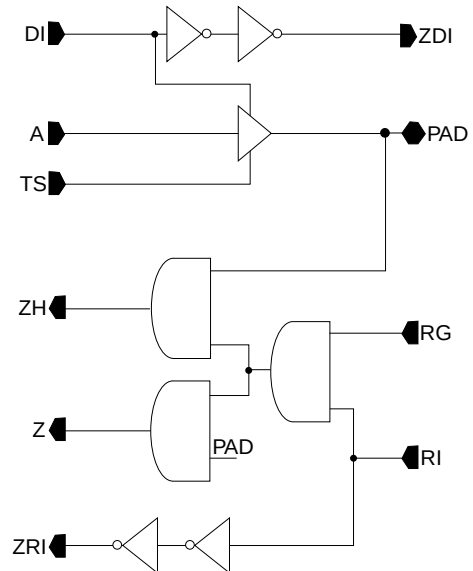
Cell: BP2535, BP2535_PM

Function: 2.5V (3.3V Tolerant) CMOS Nontest 35 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses and is tolerant of 3.3V LVTTTL levels. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.492 + 0.030D _{std}	1.033 + 0.022D _{std}	0.751 + 0.018D _{std}
		t _{PHL}	1.530 + 0.033D _{std}	1.100 + 0.024D _{std}	0.828 + 0.019D _{std}
	B	t _{PLH}	1.273 + 0.028D _{std}	0.868 + 0.021D _{std}	0.649 + 0.017D _{std}
		t _{PHL}	1.223 + 0.031D _{std}	0.862 + 0.022D _{std}	0.652 + 0.018D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{Std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{Std}	0.291 + 0.001N _{Std}	0.220 + 0.001N _{Std}
		t _{PHL}	0.391 + 0.002N _{Std}	0.310 + 0.001N _{Std}	0.251 + 0.001N _{Std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{Std}	0.432 + 0.001N _{Std}	0.345 + 0.001N _{Std}
		t _{PHL}	0.548 + 0.002N _{Std}	0.451 + 0.001N _{Std}	0.373 + 0.001N _{Std}
PAD-Z	B	t _{PLH}	0.431 + 0.002N _{Std}	0.288 + 0.001N _{Std}	0.215 + 0.001N _{Std}
		t _{PHL}	0.396 + 0.002N _{Std}	0.309 + 0.001N _{Std}	0.245 + 0.001N _{Std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{Std}	0.433 + 0.001N _{Std}	0.344 + 0.001N _{Std}
		t _{PHL}	0.555 + 0.002N _{Std}	0.456 + 0.001N _{Std}	0.375 + 0.001N _{Std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	10.590	10.485
DI	7.167	7.187
PAD (Receiver Input)	459.583	459.583
RG	1.933	1.933
RI	3.427	3.427
TS	6.174	6.172
Internal	631.672	627.812
Cell Units	1 cell	1 cell

Cell: BP2550, BP2550_PM

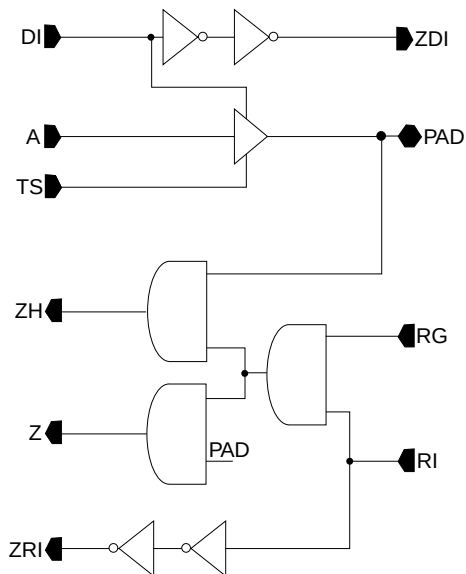
Function: 2.5V (3.3V Tolerant) CMOS Nontest 50 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses and is tolerant of 3.3V LVTTTL levels. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.457 + 0.040D _{std}	1.018 + 0.030D _{std}	0.743 + 0.025D _{std}
		t _{PHL}	1.494 + 0.043D _{std}	1.073 + 0.031D _{std}	0.811 + 0.026D _{std}
	B	t _{PLH}	1.233 + 0.039D _{std}	0.865 + 0.030D _{std}	0.664 + 0.025D _{std}
		t _{PHL}	1.177 + 0.041D _{std}	0.847 + 0.030D _{std}	0.658 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.291 + 0.001N _{std}	0.220 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.310 + 0.001N _{std}	0.251 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.432 + 0.001N _{std}	0.345 + 0.001N _{std}
		t _{PHL}	0.548 + 0.002N _{std}	0.451 + 0.001N _{std}	0.373 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.431 + 0.002N _{std}	0.288 + 0.001N _{std}	0.215 + 0.001N _{std}
		t _{PHL}	0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.433 + 0.001N _{std}	0.344 + 0.001N _{std}
		t _{PHL}	0.555 + 0.002N _{std}	0.456 + 0.001N _{std}	0.375 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	10.627	10.544
DI	7.171	7.155
PAD (Receiver Input)	437.833	437.833
RG	1.933	1.933
RI	3.427	3.427
TS	6.174	6.172
Internal	757.612	755.517
Cell Units	1 cell	1 cell

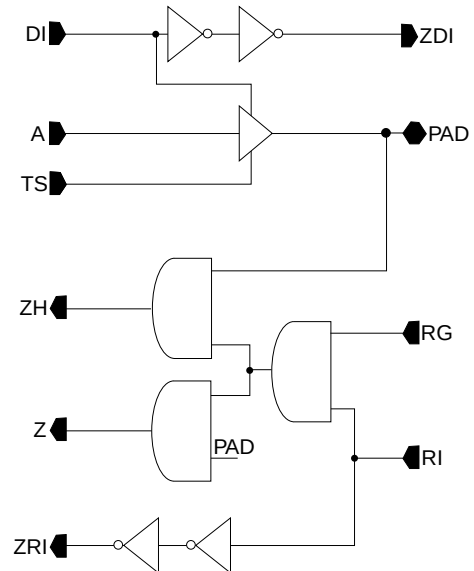
Cell: BP2565, BP2565_PM

Function: 2.5V (3.3V Tolerant) CMOS Nontest 65 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses and is tolerant of 3.3V LVTTTL levels. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.437 + 0.052D _{std}	1.003 + 0.040D _{std}	0.740 + 0.034D _{std}
		t _{PHL}	1.449 + 0.054D _{std}	1.052 + 0.041D _{std}	0.799 + 0.034D _{std}
	B	t _{PLH}	1.197 + 0.052D _{std}	0.864 + 0.040D _{std}	0.675 + 0.034D _{std}
		t _{PHL}	1.140 + 0.053D _{std}	0.848 + 0.040D _{std}	0.669 + 0.034D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.291 + 0.001N _{std}	0.220 + 0.001N _{std}
		t _{PHL}	0.391 + 0.002N _{std}	0.310 + 0.001N _{std}	0.251 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.432 + 0.001N _{std}	0.345 + 0.001N _{std}
		t _{PHL}	0.548 + 0.002N _{std}	0.451 + 0.001N _{std}	0.373 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.431 + 0.002N _{std}	0.288 + 0.001N _{std}	0.215 + 0.001N _{std}
		t _{PHL}	0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.434 + 0.001N _{std}	0.344 + 0.001N _{std}
		t _{PHL}	0.556 + 0.002N _{std}	0.456 + 0.001N _{std}	0.375 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	10.626	10.544
DI	7.168	7.159
PAD (Receiver Input)	430.583	430.583
RG	1.933	1.933
RI	3.427	3.427
TS	6.174	6.172
Internal	870.940	869.126
Cell Units	1 cell	1 cell

Cell: BP2590, BP2590_PM

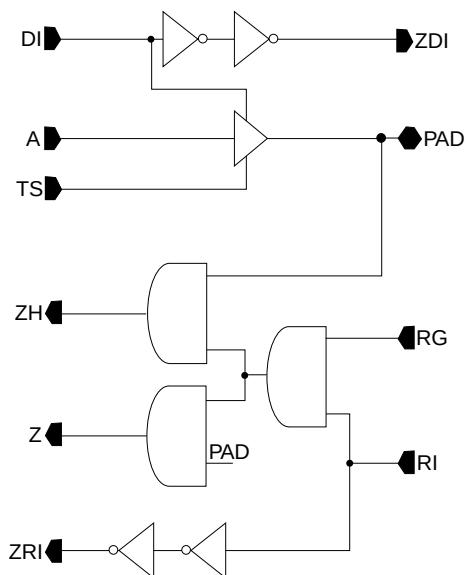
Function: 2.5V (3.3V Tolerant) CMOS Nontest 90 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses and is tolerant of 3.3V LVTTTL levels. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.128 + 0.075D _{std}	0.769 + 0.057D _{std}	0.562 + 0.048D _{std}
		t _{PHL}	1.175 + 0.076D _{std}	0.852 + 0.056D _{std}	0.639 + 0.046D _{std}
	B	t _{PLH}	1.064 + 0.075D _{std}	0.762 + 0.057D _{std}	0.605 + 0.048D _{std}
		t _{PHL}	1.181 + 0.075D _{std}	0.915 + 0.054D _{std}	0.734 + 0.045D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})			
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast	
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.291 + 0.001N _{std}	0.220 + 0.001N _{std}	
PAD-ZH		t _{PHL}	0.392 + 0.002N _{std}	0.310 + 0.001N _{std}	0.251 + 0.001N _{std}	
		t _{PLH}	0.610 + 0.002N _{std}	0.432 + 0.001N _{std}	0.345 + 0.001N _{std}	
		t _{PHL}	0.548 + 0.002N _{std}	0.451 + 0.001N _{std}	0.373 + 0.001N _{std}	
PAD-Z	B	t _{PLH}	0.431 + 0.002N _{std}	0.288 + 0.001N _{std}	0.215 + 0.001N _{std}	
PAD-ZH		t _{PHL}	0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}	
		t _{PLH}	0.619 + 0.002N _{std}	0.434 + 0.001N _{std}	0.344 + 0.001N _{std}	
		t _{PHL}	0.556 + 0.002N _{std}	0.456 + 0.001N _{std}	0.376 + 0.001N _{std}	



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	10.680	10.686
DI	7.153	7.176
PAD (Receiver Input)	326.625	326.625
RG	1.933	1.933
RI	3.427	3.427
TS	6.180	6.179
Internal	868.000	875.000
Cell Units	1 cell	1 cell

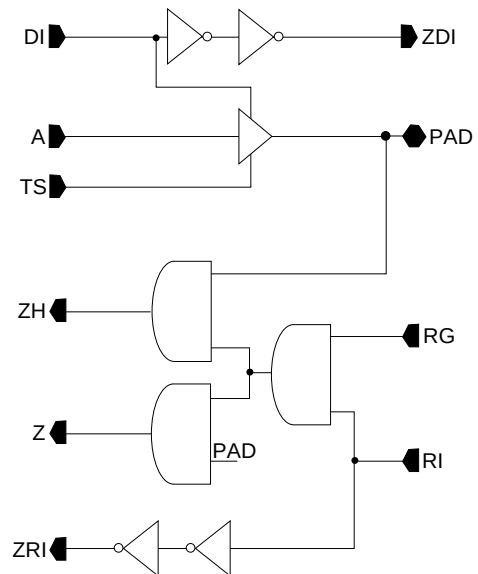
Cell: BP3320, BP3320_PM

Function: 3.3V LVTTTL (5V Protected) Nontest 20 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Receiver is 5.0V tolerant. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.771 + 0.023D _{std}	1.252 + 0.016D _{std}	0.948 + 0.013D _{std}
		t _{PHL}	1.615 + 0.023D _{std}	1.136 + 0.015D _{std}	0.871 + 0.012D _{std}
	B	t _{PLH}	1.588 + 0.022D _{std}	1.092 + 0.016D _{std}	0.823 + 0.013D _{std}
		t _{PHL}	1.424 + 0.022D _{std}	0.974 + 0.014D _{std}	0.736 + 0.011D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.416 + 0.002N _{std}	0.237 + 0.001N _{std}	0.144 + 0.001N _{std}
		t _{PHL}	0.629 + 0.001N _{std}	0.521 + 0.001N _{std}	0.456 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.355 + 0.001N _{std}	0.238 + 0.001N _{std}
		t _{PHL}	0.709 + 0.001N _{std}	0.593 + 0.001N _{std}	0.517 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.420 + 0.002N _{std}	0.227 + 0.001N _{std}	0.128 + 0.001N _{std}
		t _{PHL}	0.630 + 0.001N _{std}	0.530 + 0.001N _{std}	0.464 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.351 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PHL}	0.711 + 0.001N _{std}	0.603 + 0.001N _{std}	0.527 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	12.249	12.250
DI	5.736	5.736
PAD (Receiver Input)	545.083	544.917
RG	2.098	2.098
RI	3.366	3.366
TS	4.429	4.430
Internal	169.000	166.000
Cell Units	1 cell	1 cell

Cell: BP3335, BP3335_PM

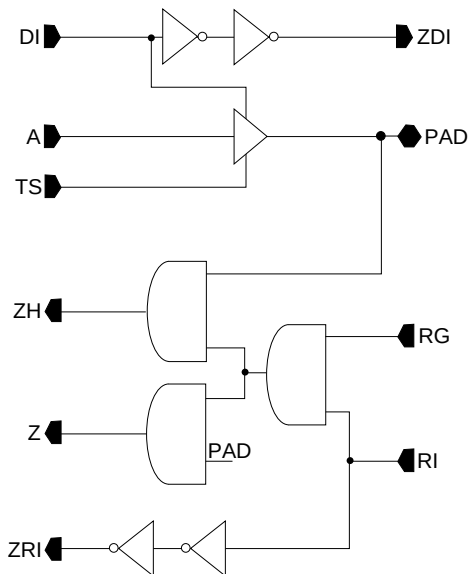
Function: 3.3V LVTTL (5V Protected) Nontest 35 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTL off-chip bidirectional data buses. Receiver is 5.0V tolerant. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.650 + 0.031D _{std}	1.154 + 0.023D _{std}	0.861 + 0.019D _{std}
		t _{PHL}	1.513 + 0.031D _{std}	1.052 + 0.022D _{std}	0.798 + 0.018D _{std}
	B	t _{PLH}	1.482 + 0.029D _{std}	1.033 + 0.022D _{std}	0.788 + 0.018D _{std}
		t _{PHL}	1.354 + 0.029D _{std}	0.938 + 0.021D _{std}	0.718 + 0.017D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.416 + 0.002N _{std}	0.237 + 0.001N _{std}	0.144 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.629 + 0.001N _{std}	0.521 + 0.001N _{std}	0.456 + 0.000N _{std}
		t _{PLH}	0.610 + 0.002N _{std}	0.355 + 0.001N _{std}	0.238 + 0.001N _{std}
		t _{PHL}	0.709 + 0.001N _{std}	0.593 + 0.001N _{std}	0.517 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.420 + 0.002N _{std}	0.227 + 0.001N _{std}	0.128 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.630 + 0.001N _{std}	0.530 + 0.001N _{std}	0.464 + 0.000N _{std}
		t _{PLH}	0.613 + 0.002N _{std}	0.351 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PHL}	0.711 + 0.001N _{std}	0.603 + 0.001N _{std}	0.527 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	12.264	12.266
DI	5.738	5.738
PAD (Receiver Input)	545.083	544.917
RG	2.098	2.098
RI	3.366	3.366
TS	4.520	4.520
Internal	221.000	219.000
Cell Units	1 cell	1 cell

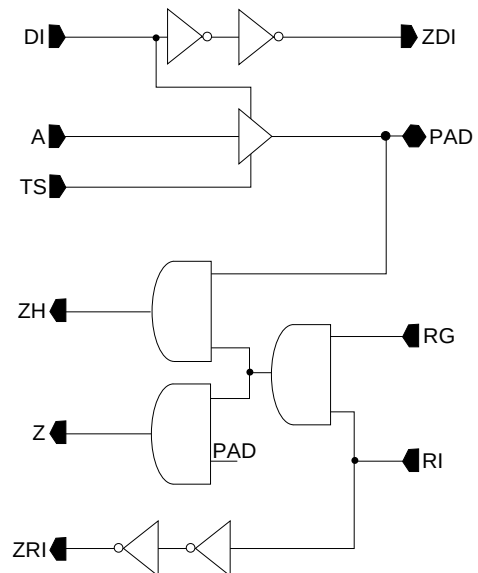
Cell: BP3350, BP3350_PM

Function: 3.3V LVTTTL (5V Protected) Nontest 50 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Receiver is 5.0V tolerant. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.549 + 0.041D _{std}	1.094 + 0.031D _{std}	0.821 + 0.026D _{std}
		t _{PHL}	1.427 + 0.042D _{std}	0.983 + 0.030D _{std}	0.741 + 0.025D _{std}
	B	t _{PLH}	1.348 + 0.040D _{std}	0.962 + 0.030D _{std}	0.750 + 0.025D _{std}
		t _{PHL}	1.203 + 0.040D _{std}	0.836 + 0.029D _{std}	0.650 + 0.024D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.416 + 0.002N _{std}	0.237 + 0.001N _{std}	0.144 + 0.001N _{std}
		t _{PHL}	0.629 + 0.001N _{std}	0.521 + 0.001N _{std}	0.456 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.355 + 0.001N _{std}	0.238 + 0.001N _{std}
		t _{PHL}	0.709 + 0.001N _{std}	0.593 + 0.001N _{std}	0.517 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.420 + 0.002N _{std}	0.227 + 0.001N _{std}	0.128 + 0.001N _{std}
		t _{PHL}	0.630 + 0.001N _{std}	0.530 + 0.001N _{std}	0.464 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.351 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PHL}	0.711 + 0.001N _{std}	0.603 + 0.001N _{std}	0.527 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	12.282	12.283
DI	5.738	5.738
PAD (Receiver Input)	545.083	544.917
RG	2.098	2.098
RI	3.366	3.366
TS	4.520	4.521
Internal	283.000	282.000
Cell Units	1 cell	1 cell

Cell: BP3365, BP3365_PM

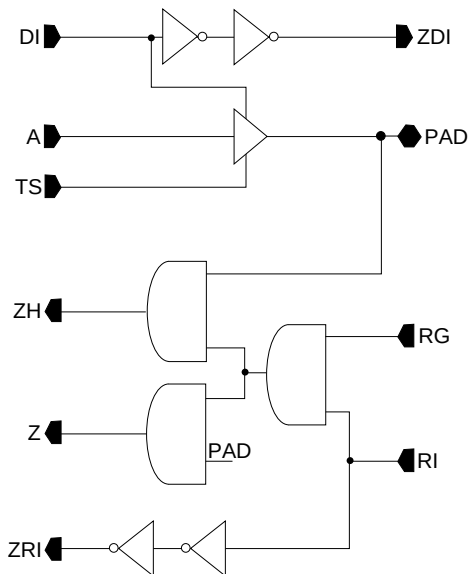
Function: 3.3V LVTTL (5V Protected) Nontest 65 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTL off-chip bidirectional data buses. Receiver is 5.0V tolerant. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.417 + 0.054D _{std}	1.012 + 0.041D _{std}	0.765 + 0.034D _{std}
		t _{PHL}	1.300 + 0.054D _{std}	0.899 + 0.039D _{std}	0.680 + 0.033D _{std}
	B	t _{PLH}	1.199 + 0.052D _{std}	0.878 + 0.039D _{std}	0.700 + 0.033D _{std}
		t _{PHL}	1.095 + 0.053D _{std}	0.783 + 0.038D _{std}	0.619 + 0.032D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.416 + 0.002N _{std}	0.237 + 0.001N _{std}	0.144 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.629 + 0.001N _{std}	0.521 + 0.001N _{std}	0.456 + 0.000N _{std}
		t _{PLH}	0.610 + 0.002N _{std}	0.355 + 0.001N _{std}	0.238 + 0.001N _{std}
		t _{PHL}	0.709 + 0.001N _{std}	0.593 + 0.001N _{std}	0.517 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.420 + 0.002N _{std}	0.227 + 0.001N _{std}	0.128 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.630 + 0.001N _{std}	0.530 + 0.001N _{std}	0.464 + 0.000N _{std}
		t _{PLH}	0.613 + 0.002N _{std}	0.351 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PHL}	0.711 + 0.001N _{std}	0.603 + 0.001N _{std}	0.527 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	12.283	12.285
DI	5.736	5.736
PAD (Receiver Input)	545.083	544.917
RG	2.098	2.098
RI	3.366	3.366
TS	4.520	4.520
Internal	347.000	347.000
Cell Units	1 cell	1 cell

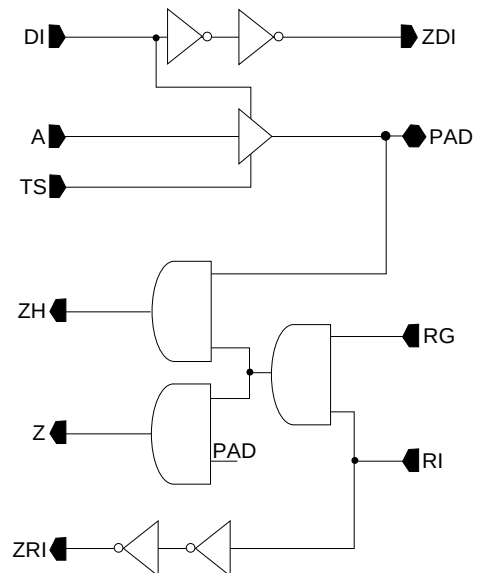
Cell: BP3390, BP3390_PM

Function: 3.3V LVTTTL (5V Protected) Nontest 90 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Receiver is 5.0V tolerant. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.250 + 0.075D _{std}	0.895 + 0.057D _{std}	0.678 + 0.048D _{std}
		t _{PHL}	1.164 + 0.072D _{std}	0.806 + 0.053D _{std}	0.607 + 0.045D _{std}
	B	t _{PLH}	1.025 + 0.074D _{std}	0.774 + 0.056D _{std}	0.635 + 0.047D _{std}
		t _{PHL}	1.028 + 0.071D _{std}	0.766 + 0.052D _{std}	0.626 + 0.044D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.416 + 0.002N _{std}	0.237 + 0.001N _{std}	0.144 + 0.001N _{std}
		t _{PHL}	0.629 + 0.001N _{std}	0.521 + 0.001N _{std}	0.456 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.355 + 0.001N _{std}	0.238 + 0.001N _{std}
		t _{PHL}	0.709 + 0.001N _{std}	0.593 + 0.001N _{std}	0.517 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.420 + 0.002N _{std}	0.227 + 0.001N _{std}	0.128 + 0.001N _{std}
		t _{PHL}	0.630 + 0.001N _{std}	0.530 + 0.001N _{std}	0.464 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.351 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PHL}	0.711 + 0.001N _{std}	0.603 + 0.001N _{std}	0.527 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	12.283	12.283
DI	5.738	5.738
PAD (Receiver Input)	545.083	544.917
RG	2.098	2.098
RI	3.366	3.366
TS	4.521	4.520
Internal	868.000	875.000
Cell Units	1 cell	1 cell

Cell: BPCIX3, BPCIX3_PM

Function: 3.3V PCI-X/PCI Nontest 3-State CIO

Description:

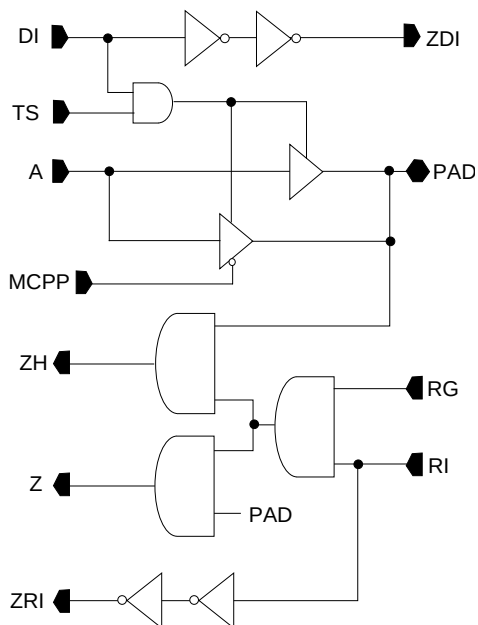
A noninverting three-state nontest driver/receiver that interfaces 1.8V internal functions with 3.3V PCI-X or PCI off-chip bidirectional data buses. Both non-hysteresis, and hysteresis receiver outputs are provided. The hysteresis output path will have improved noise immunity, but a slightly slower propagation delay. A mode control (MCP) provides a 40 ohm driver impedance for point-to-point applications and a 20 ohm impedance for multi-point applications. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

Refer to the IBM application note *ASIC I/O Test Considerations* for required MCP pin test connections. The application note is available from your IBM representative or at the following URL:

<http://www.chips.ibm.com/techlib/products/asics/apnotes.html>

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
PAD	Driver output/receiver input
Z	Non-hysteresis receiver output
ZH	Noninverting receiver output with hysteresis
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)
MCP	Driver mode control

Pin Group: (Z,ZH): (1,2)



Driver Mode Control Table

MCP	Driver Mode of Operation
0	Multi-point mode
1	Point-to-point mode

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Driver Propagation Delays (Point-to-Point Mode)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.628 + 0.022D_{std}$	$1.030 + 0.015D_{std}$	$0.765 + 0.011D_{std}$
		t_{PHL}	$1.690 + 0.023D_{std}$	$1.137 + 0.015D_{std}$	$0.847 + 0.012D_{std}$

Receiver Propagation Delays (Point-to-Point Mode)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.749 + 0.002N _{std}	0.554 + 0.001N _{std}	0.455 + 0.001N _{std}
		t _{PHL}	0.320 + 0.001N _{std}	0.248 + 0.000N _{std}	0.191 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.790 + 0.002N _{std}	0.568 + 0.001N _{std}	0.461 + 0.001N _{std}
		t _{PHL}	0.467 + 0.000N _{std}	0.389 + 0.000N _{std}	0.329 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	19.516
DI	12.138
MCP	3.028
PAD (Receiver Input)	680.000
RG	2.282
RI	3.387
TS	12.505
Internal	294.614
Cell Units	1 cell

Cell: BPCIX3PU, BPCIX3PU_PM

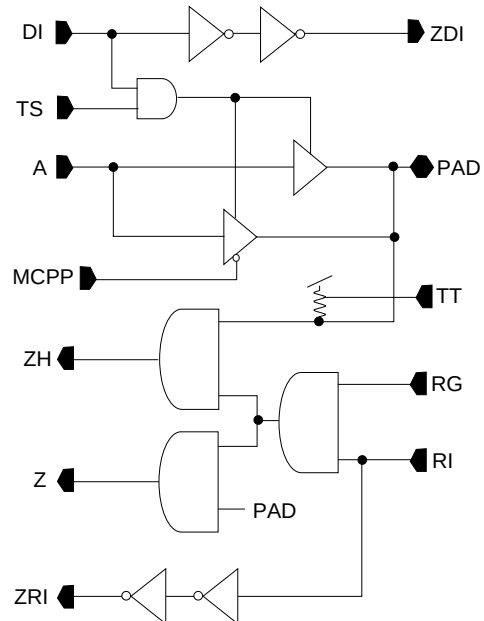
Function: 3.3V PCI-X/PCI Nontest 3-State CIO w/Pull-Up

Description:

A noninverting three-state nontest driver/receiver that interfaces 1.8V internal functions with 3.3V PCI-X or PCI off-chip bidirectional data buses. Both non-hysteresis and hysteresis receiver outputs are provided. The hysteresis output path will have improved noise immunity, but a slightly slower propagation delay. A mode control (MCP) provides a 40 ohm driver impedance for point-to-point applications and a 20 ohm impedance for multi-point applications. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} . PAD is pulled up to logic "1" (3.3V) through 14k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test.

Refer to the IBM application note *ASIC I/O Test Considerations* for required MCP pin test connections. The application note is available from your IBM representative or at the following URL:

<http://www.chips.ibm.com/techlib/products/asics/apnotes.html>



A	Driver data input
TS	Driver three-state control
TT	Pull-up resistor enable
DI	Driver inhibit input (DI in)
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
PAD	Driver output/receiver input
Z	Non-hysteresis receiver output
ZH	Noninverting receiver output with hysteresis
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)
MCP	Driver mode control

Pin Group: (Z,ZH): (1,2)



Driver Mode Control Table

MCP	Driver Mode of Operation
0	Multi-point mode
1	Point-to-point mode

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Propagation Delays (Point-to-Point Mode)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$1.367 + 0.032D_{std}$	$0.869 + 0.023D_{std}$	$0.608 + 0.017D_{std}$
		t_{PHL}	$1.873 + 0.042D_{std}$	$1.270 + 0.028D_{std}$	$0.936 + 0.021D_{std}$

Receiver Propagation Delays (Point-to-Point Mode)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.700 + 0.001N _{std}	0.496 + 0.001N _{std}	0.390 + 0.001N _{std}
		t _{PHL}	0.270 + 0.001N _{std}	0.200 + 0.000N _{std}	0.121 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.752 + 0.002N _{std}	0.521 + 0.001N _{std}	0.402 + 0.001N _{std}
		t _{PHL}	0.434 + 0.000N _{std}	0.351 + 0.000N _{std}	0.264 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	19.128
DI	12.570
MCP	2.931
PAD (Receiver Input)	671.000
RG	2.283
RI	3.505
TS	13.155
TT	7.830
Internal	294.917
Cell Units	1 cell

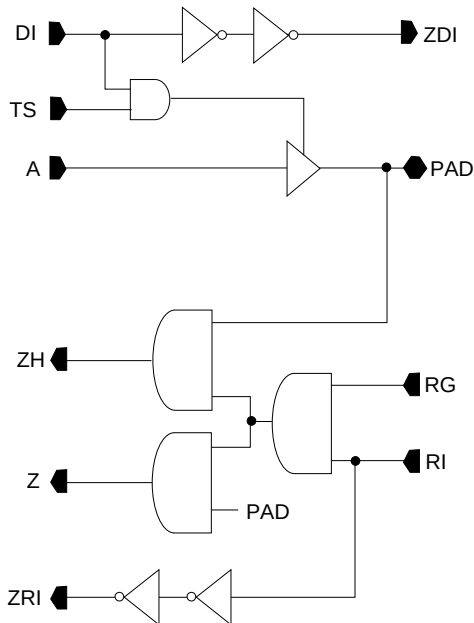
Cell: BPCI5, BPCI5_PM

Function: 3.3V/5V Tolerant PCI Nontest 3-State CIO

Description:

A noninverting three-state nontest driver/receiver that interfaces 1.8V internal functions with 5V PCI off-chip bidirectional data buses. Both non-hysteresis and hysteresis receiver outputs are provided. The hysteresis output path will have improved noise immunity, but a slightly slower propagation delay. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- Z Non-hysteresis receiver output
- ZH Noninverting receiver output with hysteresis
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z,ZH): (1,2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.558 + 0.024D _{std}	0.982 + 0.017D _{std}	0.710 + 0.013D _{std}
		t _{PHL}	1.787 + 0.014D _{std}	1.183 + 0.009D _{std}	0.871 + 0.007D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	1.073 + 0.003N _{std}	0.623 + 0.002N _{std}	0.429 + 0.001N _{std}
		t _{PHL}	0.571 + 0.001N _{std}	0.455 + 0.000N _{std}	0.378 + 0.000N _{std}
PAD-ZH		t _{PLH}	1.249 + 0.002N _{std}	0.657 + 0.001N _{std}	0.429 + 0.001N _{std}
		t _{PHL}	0.719 + 0.000N _{std}	0.593 + 0.000N _{std}	0.511 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	18.409
DI	6.853
PAD (Receiver Input)	634.667
RG	2.332
RI	3.480
TS	6.771
Internal	1450.000
Cell Units	1 cell

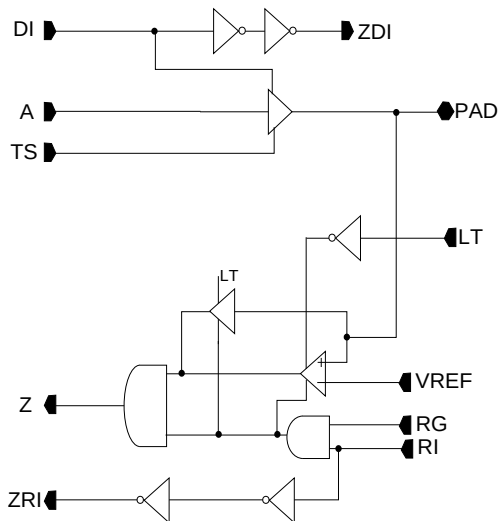
Cell: BSSTL2C1, BSSTL2C1_PM

Function: SSTL 2.5V Class 1 Nontest 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V SSTL2 Class 1 off-chip bidirectional data buses. Driver is designed to provide a minimum 7.6 mA sink/source current at SSTL levels. Input receiver requires reference voltage of $V_{dd250}/2$. A, TS, Z, LT and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- LT I_{ddq} leakage test control
- VREF Reference voltage input
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z ¹	DI
-	0	-	Hi-Z ¹	DI
-	1	1	A	DI

¹. PAD is Hi-Z if driver is not externally terminated. Pad is at V_{TT} ($V_{dd250}/2$) if driver is terminated off-chip.

Note: Timing model will be based on driver terminated off-chip.

Receiver Truth Table

Inputs					Outputs		Comments
PAD	LT	RI	RG	VREF	Z	ZRI	
-	-	0	-	-	0	RI	Receiver disabled (no DC current) - test control
-	-	-	0	-	0	RI	Receiver disabled (no DC current) - user control
0 ¹	1	1	1	-	0	RI	Bypass test receiver enabled (no DC current)
1 ¹	1	1	1	-	1	RI	Bypass test receiver enabled (no DC current)
Hi-Z ¹	1	1	1	-	X	RI	Bypass test receiver enabled (no DC current)
0 ²	0	1	1	V _{dd250} /2	0	RI	Functional receiver enabled
1 ²	0	1	1	V _{dd250} /2	1	RI	Functional receiver enabled
Hi-Z ²	0	1	1	V _{dd250} /2	X	RI	Functional receiver enabled

1. PAD input requires 2.5V CMOS levels.

2. PAD input requires 2.5V SSTL levels.

Note: LT, RG, and RI can all turn off turn off SSTL input differential amplifier DC bias current.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	0.759 + 0.025D _{std}	0.552 + 0.022D _{std}	0.421 + 0.020D _{std}
		t _{PHL}	0.709 + 0.026D _{std}	0.501 + 0.022D _{std}	0.367 + 0.019D _{std}
	B	t _{PLH}	0.730 + 0.024D _{std}	0.530 + 0.021D _{std}	0.405 + 0.019D _{std}
		t _{PHL}	0.666 + 0.026D _{std}	0.471 + 0.021D _{std}	0.347 + 0.019D _{std}



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	1.027 + 0.001N _{std}	0.641 + 0.001N _{std}	0.424 + 0.000N _{std}
		t _{PHL}	1.022 + 0.003N _{std}	0.634 + 0.001N _{std}	0.428 + 0.001N _{std}
	B	t _{PLH}	1.027 + 0.001N _{std}	0.641 + 0.001N _{std}	0.424 + 0.000N _{std}
		t _{PHL}	1.022 + 0.003N _{std}	0.634 + 0.001N _{std}	0.428 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	31.104	34.562
DI	4.845	4.862
LT	3.531	3.531
PAD (Receiver Input)	322.250	322.167
RG	5.563	5.561
RI	6.603	6.602
TS	2.501	2.501
VREF	109.517	109.517
Internal	585.000	595.000
Cell Units	1 cell	1 cell

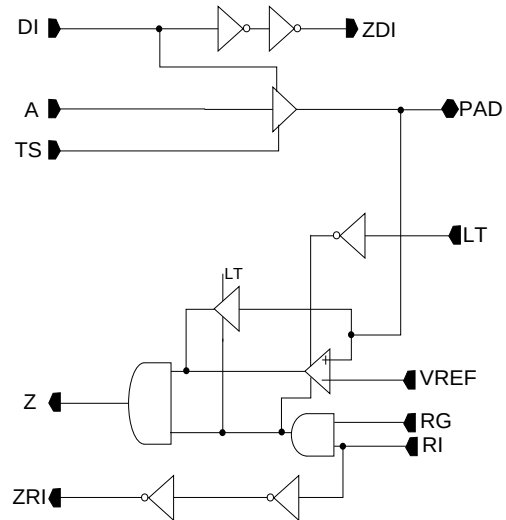
Cell: BSSTL2C2, BSSTL2C2_PM

Function: SSTL 2.5V Class 2 Nontest 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V SSTL2 Class 2 off-chip bidirectional data buses. Driver is designed to provide a minimum 15.2 mA sink/source current at SSTL levels. Input receiver requires reference voltage of $V_{dd250}/2$. A, TS, Z, LT and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- LT I_{ddq} leakage test control
- VREF Reference voltage input
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z ¹	DI
-	0	-	Hi-Z ¹	DI
-	1	1	A	DI

¹ PAD is Hi-Z if driver is not externally terminated. Pad is at V_{TT} ($V_{dd250}/2$) if driver is terminated off-chip.

Note: Timing model will be based on driver terminated off-chip.



Receiver Truth Table

Inputs					Outputs		Comments
PAD	LT	RI	RG	VREF	Z	ZRI	
-	-	0	-	-	0	RI	Receiver disabled (no DC current) - test control
-	-	-	0	-	0	RI	Receiver disabled (no DC current) - user control
0 ¹	1	1	1	-	0	RI	Bypass test receiver enabled (no DC current)
1 ¹	1	1	1	-	1	RI	Bypass test receiver enabled (no DC current)
Hi-Z ¹	1	1	1	-	X	RI	Bypass test receiver enabled (no DC current)
0 ²	0	1	1	V _{dd250} /2	0	RI	Functional receiver enabled
1 ²	0	1	1	V _{dd250} /2	1	RI	Functional receiver enabled
Hi-Z ²	0	1	1	V _{dd250} /2	X	RI	Functional receiver enabled

¹. PAD input requires 2.5V CMOS levels.

². PAD input requires 2.5V SSTL levels.

Note: LT, RG, and RI can all turn off turn off SSTL input differential amplifier DC bias current.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.033 + 0.015D _{std}	0.741 + 0.013D _{std}	0.559 + 0.011D _{std}
		t _{PHL}	1.029 + 0.017D _{std}	0.709 + 0.013D _{std}	0.515 + 0.011D _{std}
	B	t _{PLH}	0.791 + 0.013D _{std}	0.558 + 0.011D _{std}	0.419 + 0.010D _{std}
		t _{PHL}	0.746 + 0.014D _{std}	0.513 + 0.011D _{std}	0.374 + 0.010D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$1.027 + 0.001N_{std}$	$0.641 + 0.001N_{std}$	$0.424 + 0.000N_{std}$
		t_{PHL}	$1.022 + 0.003N_{std}$	$0.634 + 0.001N_{std}$	$0.428 + 0.001N_{std}$
	B	t_{PLH}	$1.027 + 0.001N_{std}$	$0.641 + 0.001N_{std}$	$0.424 + 0.000N_{std}$
		t_{PHL}	$1.022 + 0.003N_{std}$	$0.634 + 0.001N_{std}$	$0.428 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	34.575	34.625
DI	4.843	4.869
LT	3.531	3.531
PAD (Receiver Input)	478.250	478.375
RG	5.561	5.562
RI	6.602	6.602
TS	2.527	2.526
VREF	109.517	109.517
Internal	786.000	810.000
Cell Units	1 cell	1 cell

Cell: VSSTL2R1, VSSTL2R1_PM

Function: Voltage Reference Receiver

Description:

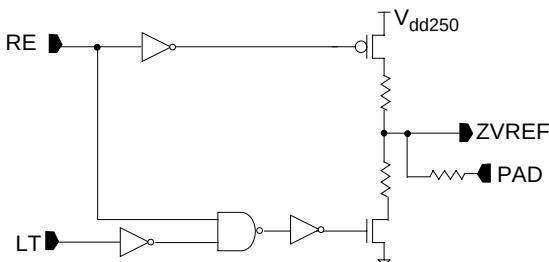
This cell generates a precision on-chip reference voltage ($V_{dd250}/2$). At system mode, the reference may be disabled ($RE = 0$) to apply an external reference voltage through the PAD pin, or the on-chip reference generator may remain enabled ($RE = 1$). When enabled, the reference generator requires 1.0 mA of current.

RE Reference enable input

LT DC current gate (I_{dd} test) input

PAD Connection to package pin

ZVREF Reference voltage



Driver Truth Table

Inputs			Output	Comments
PAD	LT	RE	ZVREF	
-	0	1	X	$ZVREF = 0.5 * V_{dd250}$; used during wafer test
-	1	1	X	$ZVREF = V_{dd250}$
-	-	0	X	Reference generator is Hi-Z; used during packaged device test

Notes:

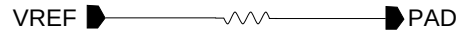
- Resistance between PAD and VREF is negligible.
- This cell is NOT ALLOWED in 64 test pin locations.

Cell: VSSTL2R2, VSSTL2R2_PM

Function: Supplemental SSTL2 Voltage Reference Pin (VREF Driver)

Description:

This cell provides additional PAD for external reference voltage. Additional pads are required to stabilize reference voltage due to noise. A minimum of one is recommended.



VREF Reference voltage

PAD Off-chip supplied reference voltage

Driver Truth Table

Inputs	Outputs	Comments
VREF	PAD	
-	X	Supplemental external VREF pin

Notes:

- This cell is NOT ALLOWED in 64 test pin locations.
- PAD is electrically hard-wired to VREF. It is used as a supplementary external VREF pin. The customer can provide as many pins on the chip as required.

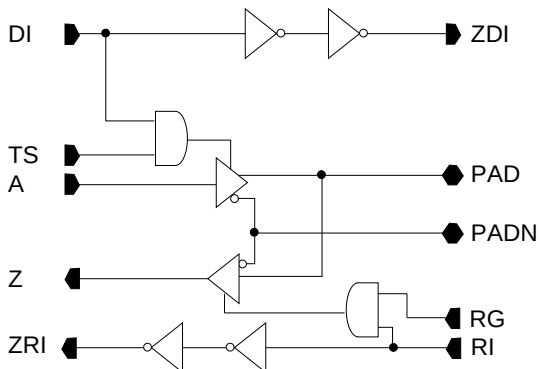
Cell: BSSTL2DIFF, BSSTL2DIFF_PM

Function: 2.5V BSSTL2DIFF Differential CIO Nontest

Description:

Noninverting, fully differential dual power supply driver used to drive complementary SSTL2 clock signals. All inputs are 1.8V (nominal) CMOS. A differential termination of 120 ohms between PAD and PADN at the far end receiver is required.

- A Driver data input
- TS Driver three-state control
- DI Driver input (DI1 in/ I_{ddq} test)
- RI Receiver input (RI in/ I_{ddq} test)
- RG Receiver gate control
- PAD In-phase driver out
- PADN Out-phase driver out
- Z Receiver out
- ZRI Receiver inhibit (RI out)
- ZDI Driver inhibit out (DI1 out)



Driver Truth Table

Inputs			Outputs			Comments
A	TS	DI	PAD	PADN	ZDI	
-	0	-	Hi-Z	Hi-Z	DI	Functional mode
-	-	0	Hi-Z	Hi-Z	DI	Leakage test
-	1	1	A	$\bar{A}$	DI	Functional mode

Receiver Truth Table

Inputs				Outputs		Comments
PAD	PADN	RG	RI	Z	ZRI	
0	1	1	1	0	RI	Functional mode
1	0	1	1	1	RI	Functional mode
1	1	1	1	X	RI	Functional mode
0	0	1	1	X	RI	Functional mode
-	-	-	0	0	RI	Leakage test
-	-	0	-	0	RI	Disable receiver

Usage Notes:

1. Normal driver operation requires a termination at the far end of the net at input to the receiver.
2. Termination must be one of the following:
 - A split 120 ohm differential termination of 60 ohms from the (+) input and 60 ohms from the (-) input to a center tap connected to V_{TT} ($V_{ddq}/2$).
 - A 120 ohm terminator between (+) and (-) receiver inputs.
3. Inputs to the receiver must be complementary during functional mode; otherwise the output will be indeterminate.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$1.073 + 0.021D_{std}$	$0.746 + 0.017D_{std}$	$0.550 + 0.014D_{std}$
		t_{PHL}	$1.059 + 0.021D_{std}$	$0.747 + 0.017D_{std}$	$0.546 + 0.014D_{std}$



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.606 + 0.001N_{std}$	$0.417 + 0.001N_{std}$	$0.292 + 0.000N_{std}$
		t_{PHL}	$0.697 + 0.001N_{std}$	$0.463 + 0.001N_{std}$	$0.303 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	68.429
DI	5.126
PAD (Receiver Input)	443.417
PADN (Receiver Input)	449.542
RG	6.124
RI	6.860
TS	2.670
Internal	950.000
Cell Units	2 cells

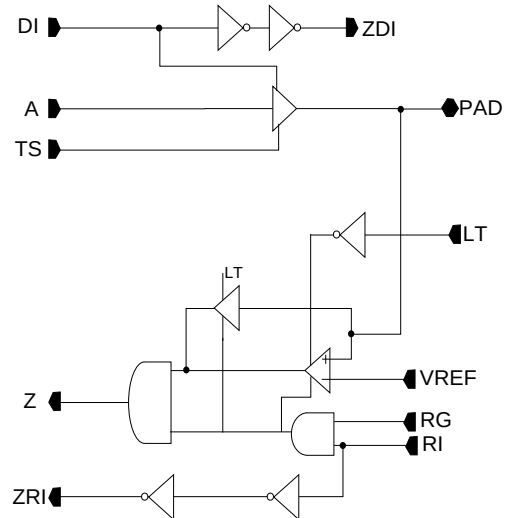
Cell: BSSTL2C50, BSSTL2C50_PM

Function: 2.5V SSTL Nontest 3-State CIO With Half-Strength Driver

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V SSTL2 off-chip bidirectional data buses. Driver is designed for use with transmission line impedances of 45 to 55 ohms. Input receiver requires reference voltage of $V_{dd250}/2$. A, TS, Z, LT and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- LT I_{ddq} leakage test control
- VRER Reference voltage input
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z ¹	DI
-	0	-	Hi-Z ¹	DI
-	1	1	A	DI

¹. PAD is Hi-Z if driver is not externally terminated. Pad is at V_{TT} ($V_{dd250}/2$) if driver is terminated off-chip.

Note: NDR will assume off-chip termination.



Receiver Truth Table

Inputs					Outputs		Comments
PAD	LT	RI	RG	VREF	Z	ZRI	
-	-	0	-	-	0	RI	Receiver disabled (no DC current); test control
-	-	-	0	-	0	RI	Receiver disabled (no DC current); user control
0 ¹	1	1	1	-	0	RI	Bypass test receiver enabled (no DC current)
1 ¹	1	1	1	-	1	RI	Bypass test receiver enabled (no DC current)
Hi-Z ¹	1	1	1	-	X	RI	Bypass test receiver enabled (no DC current)
0 ²	0	1	1	V _{dd250} /2	0	RI	Functional receiver enabled
1 ²	0	1	1	V _{dd250} /2	1	RI	Functional receiver enabled
Hi-Z ²	0	1	1	V _{dd250} /2	X	RI	Functional receiver enabled

¹. Pad input requires CMOS levels.

². PAD input requires SSTL levels.

Note: LT, RG, and RI can all turn off turn off DC bias current of the SSTL input differential amplifier. VREF is supplied by voltage reference cells VSSTL2R1_A and VSSTL2R2_A.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.089 + 0.041D _{std}	0.776 + 0.031D _{std}	0.581 + 0.026D _{std}
		t _{PHL}	1.209 + 0.045D _{std}	0.806 + 0.032D _{std}	0.564 + 0.026D _{std}
	B	t _{PLH}	0.766 + 0.040D _{std}	0.544 + 0.030D _{std}	0.403 + 0.025D _{std}
		t _{PHL}	0.829 + 0.042D _{std}	0.567 + 0.031D _{std}	0.410 + 0.026D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$1.027 + 0.001N_{std}$	$0.641 + 0.001N_{std}$	$0.424 + 0.000N_{std}$
		t_{PHL}	$1.022 + 0.003N_{std}$	$0.634 + 0.001N_{std}$	$0.428 + 0.001N_{std}$
	B	t_{PLH}	$1.027 + 0.001N_{std}$	$0.641 + 0.001N_{std}$	$0.424 + 0.000N_{std}$
		t_{PHL}	$1.022 + 0.003N_{std}$	$0.634 + 0.001N_{std}$	$0.428 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	37.754	37.871
DI	4.730	4.849
LT	3.582	3.582
PAD (Receiver Input)	423.833	424.000
RG	5.539	5.539
RI	6.575	6.575
TS	2.536	2.521
VREF	116.013	116.017
Internal	1411.026	1491.394
Cell Units	1 cell	1 cell

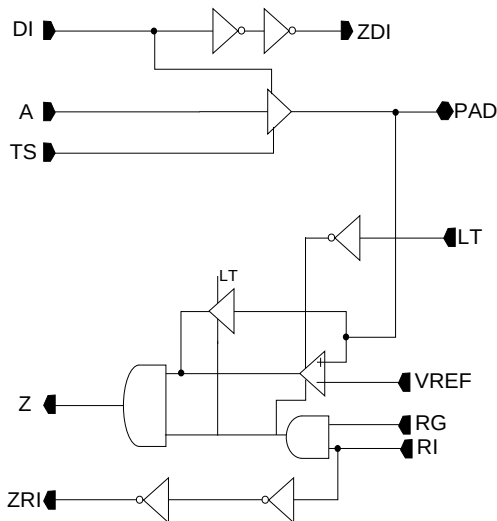
Cell: BSSTL2C56, BSSTL2C56_PM

Function: 2.5V SSTL Nontest 3-State CIO With Half-Strength Driver

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V SSTL2 off-chip bidirectional data buses. Driver is designed for use with transmission line impedances of 50 to 62 ohms. Input receiver requires reference voltage of $V_{dd250}/2$. A, TS, Z, LT and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- LT I_{ddq} leakage test control
- VRER Reference voltage input
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z ¹	DI
-	0	-	Hi-Z ¹	DI
-	1	1	A	DI

¹. PAD is Hi-Z if driver is not externally terminated. Pad is at V_{TT} ($V_{dd250}/2$) if driver is terminated off-chip.

Note: NDR will assume off-chip termination.

Receiver Truth Table

Inputs					Outputs		Comments
PAD	LT	RI	RG	VREF	Z	ZRI	
-	-	0	-	-	0	RI	Receiver disabled (no DC current); test control
-	-	-	0	-	0	RI	Receiver disabled (no DC current); user control
0 ¹	1	1	1	-	0	RI	Bypass test receiver enabled (no DC current)
1 ¹	1	1	1	-	1	RI	Bypass test receiver enabled (no DC current)
Hi-Z ¹	1	1	1	-	X	RI	Bypass test receiver enabled (no DC current)
0 ²	0	1	1	V _{dd250} /2	0	RI	Functional receiver enabled
1 ²	0	1	1	V _{dd250} /2	1	RI	Functional receiver enabled
Hi-Z ²	0	1	1	V _{dd250} /2	X	RI	Functional receiver enabled

¹. Pad input requires CMOS levels.

². PAD input requires SSTL levels.

Note: LT, RG, and RI can all turn off turn off DC bias current of the SSTL input differential amplifier. VREF is supplied by voltage reference cells VSSTL2R1_A and VSSTL2R2_A.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.083 + 0.049D _{std}	0.775 + 0.037D _{std}	0.578 + 0.031D _{std}
		t _{PHL}	1.203 + 0.051D _{std}	0.809 + 0.038D _{std}	0.568 + 0.031D _{std}
	B	t _{PLH}	0.760 + 0.047D _{std}	0.544 + 0.036D _{std}	0.405 + 0.031D _{std}
		t _{PHL}	0.824 + 0.049D _{std}	0.566 + 0.036D _{std}	0.410 + 0.030D _{std}



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	1.027 + 0.001N _{std}	0.641 + 0.001N _{std}	0.424 + 0.000N _{std}
		t _{PHL}	1.022 + 0.003N _{std}	0.634 + 0.001N _{std}	0.428 + 0.001N _{std}
	B	t _{PLH}	1.027 + 0.001N _{std}	0.641 + 0.001N _{std}	0.424 + 0.000N _{std}
		t _{PHL}	1.022 + 0.003N _{std}	0.634 + 0.001N _{std}	0.428 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	37.754	37.875
DI	4.705	4.848
LT	3.582	3.582
PAD (Receiver Input)	415.917	416.208
RG	5.535	5.535
RI	6.575	6.575
TS	2.536	2.533
VREF	116.013	116.017
Internal	1412.044	1492.598
Cell Units	1 cell	1 cell

Cell: BT3320, BT3320_PM

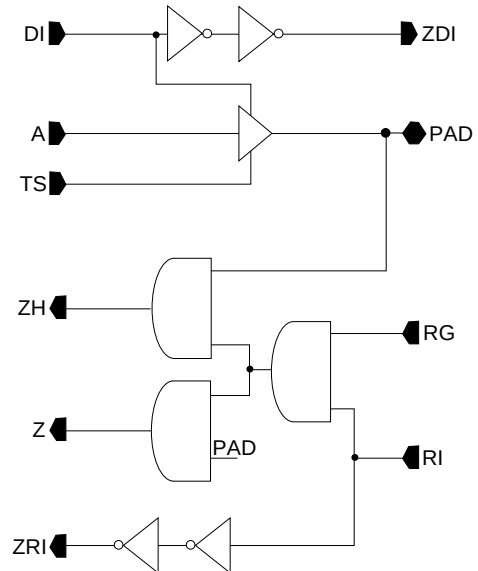
Function: 3.3V LVTTTL Nontest 20 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.644 + 0.024D _{std}	1.177 + 0.017D _{std}	0.889 + 0.014D _{std}
		t _{PHL}	1.485 + 0.024D _{std}	1.041 + 0.016D _{std}	0.788 + 0.013D _{std}
	B	t _{PLH}	1.503 + 0.021D _{std}	1.064 + 0.016D _{std}	0.810 + 0.012D _{std}
		t _{PHL}	1.388 + 0.022D _{std}	0.960 + 0.015D _{std}	0.727 + 0.011D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.282 + 0.002N _{std}	0.168 + 0.001N _{std}	0.097 + 0.001N _{std}
		t _{PHL}	0.492 + 0.001N _{std}	0.421 + 0.001N _{std}	0.379 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.410 + 0.002N _{std}	0.273 + 0.001N _{std}	0.197 + 0.001N _{std}
		t _{PHL}	0.577 + 0.001N _{std}	0.496 + 0.001N _{std}	0.442 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.287 + 0.002N _{std}	0.153 + 0.001N _{std}	0.075 + 0.001N _{std}
		t _{PHL}	0.493 + 0.001N _{std}	0.432 + 0.001N _{std}	0.388 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.417 + 0.002N _{std}	0.263 + 0.001N _{std}	0.181 + 0.001N _{std}
		t _{PHL}	0.579 + 0.001N _{std}	0.508 + 0.001N _{std}	0.453 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.625	11.624
DI	5.396	5.394
PAD (Receiver Input)	534.333	534.333
RG	2.002	2.002
RI	3.154	3.154
TS	4.298	4.298
Internal	169.000	166.041
Cell Units	1 cell	1 cell

Cell: BT3335, BT3335_PM

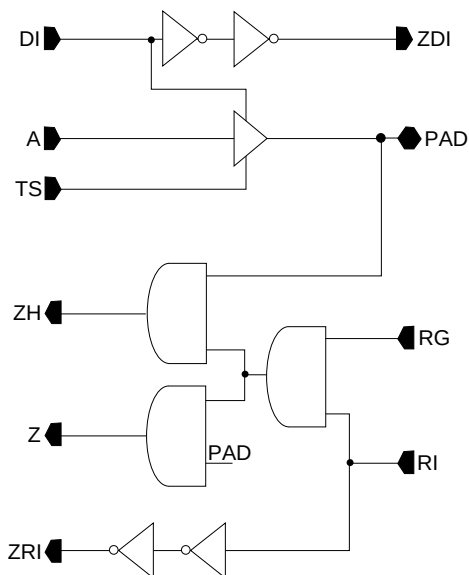
Function: 3.3V LVTTL Nontest 35 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTL off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.616 + 0.031D _{std}	1.163 + 0.024D _{std}	0.883 + 0.019D _{std}
		t _{PHL}	1.470 + 0.031D _{std}	1.037 + 0.022D _{std}	0.790 + 0.018D _{std}
	B	t _{PLH}	1.438 + 0.030D _{std}	1.035 + 0.022D _{std}	0.799 + 0.018D _{std}
		t _{PHL}	1.349 + 0.030D _{std}	0.950 + 0.021D _{std}	0.732 + 0.017D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.282 + 0.002N _{std}	0.168 + 0.001N _{std}	0.097 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.492 + 0.001N _{std}	0.421 + 0.001N _{std}	0.379 + 0.001N _{std}
		t _{PLH}	0.410 + 0.002N _{std}	0.273 + 0.001N _{std}	0.197 + 0.001N _{std}
		t _{PHL}	0.577 + 0.001N _{std}	0.496 + 0.001N _{std}	0.442 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.287 + 0.002N _{std}	0.153 + 0.001N _{std}	0.075 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.493 + 0.001N _{std}	0.431 + 0.001N _{std}	0.388 + 0.000N _{std}
		t _{PLH}	0.417 + 0.002N _{std}	0.263 + 0.001N _{std}	0.181 + 0.001N _{std}
		t _{PHL}	0.579 + 0.001N _{std}	0.508 + 0.001N _{std}	0.453 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.570	11.569
DI	5.396	5.396
PAD (Receiver Input)	456.958	457.042
RG	2.002	2.002
RI	3.154	3.154
TS	4.297	4.297
Internal	220.815	218.845
Cell Units	1 cell	1 cell

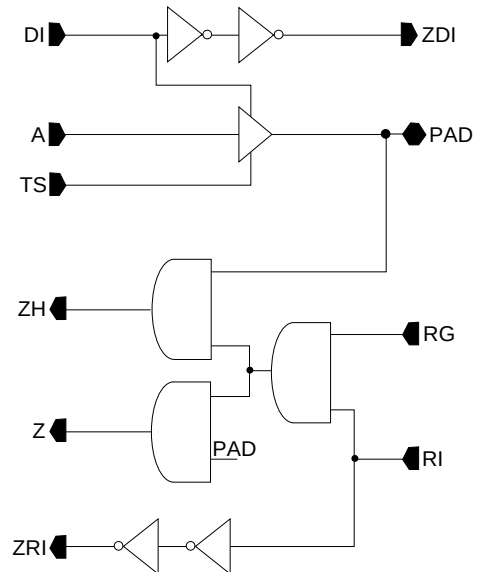
Cell: BT3350, BT3350_PM

Function: 3.3V LVTTTL Nontest 50 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.491 + 0.042D _{std}	1.082 + 0.032D _{std}	0.827 + 0.027D _{std}
		t _{PHL}	1.394 + 0.042D _{std}	0.974 + 0.031D _{std}	0.741 + 0.026D _{std}
	B	t _{PLH}	1.302 + 0.040D _{std}	0.961 + 0.030D _{std}	0.760 + 0.025D _{std}
		t _{PHL}	1.209 + 0.041D _{std}	0.865 + 0.029D _{std}	0.676 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.282 + 0.002N _{std}	0.168 + 0.001N _{std}	0.097 + 0.001N _{std}
		t _{PHL}	0.492 + 0.001N _{std}	0.421 + 0.001N _{std}	0.379 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.410 + 0.002N _{std}	0.273 + 0.001N _{std}	0.197 + 0.001N _{std}
		t _{PHL}	0.577 + 0.001N _{std}	0.496 + 0.001N _{std}	0.442 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.288 + 0.002N _{std}	0.153 + 0.001N _{std}	0.075 + 0.001N _{std}
		t _{PHL}	0.494 + 0.001N _{std}	0.432 + 0.001N _{std}	0.388 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.417 + 0.002N _{std}	0.263 + 0.001N _{std}	0.181 + 0.001N _{std}
		t _{PHL}	0.579 + 0.001N _{std}	0.508 + 0.001N _{std}	0.453 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.635	11.635
DI	5.403	5.396
PAD (Receiver Input)	424.917	425.083
RG	2.003	2.002
RI	3.156	3.154
TS	4.299	4.298
Internal	282.787	281.684
Cell Units	1 cell	1 cell

Cell: BT3350LV, BT3350LV_PM

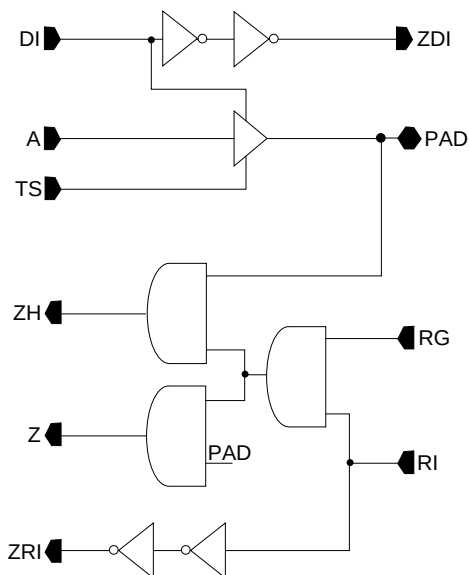
Function: Low Voltage 3.3V LVTTL Nontest 50 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces low voltage (as low as 0.9V) internal functions with 3.3V LVTTL off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$2.216 + 0.046D_{std}$	$1.599 + 0.035D_{std}$	$1.220 + 0.029D_{std}$
		t_{PHL}	$2.272 + 0.042D_{std}$	$1.567 + 0.030D_{std}$	$1.169 + 0.025D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125° C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25° C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0° C Process = Fast
PAD-Z	A	t _{PLH}	0.312 + 0.001N _{std}	0.166 + 0.001N _{std}	0.088 + 0.000N _{std}
		t _{PHL}	0.600 + 0.001N _{std}	0.484 + 0.000N _{std}	0.423 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.434 + 0.001N _{std}	0.270 + 0.001N _{std}	0.189 + 0.000N _{std}
		t _{PHL}	0.684 + 0.001N _{std}	0.559 + 0.000N _{std}	0.488 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	27.038
DI	5.320
PAD (Receiver Input)	445.292
RG	2.353
RI	3.536
TS	4.400
Internal	382.547
Cell Units	1 cell

Cell: BT3365, BT3365_PM

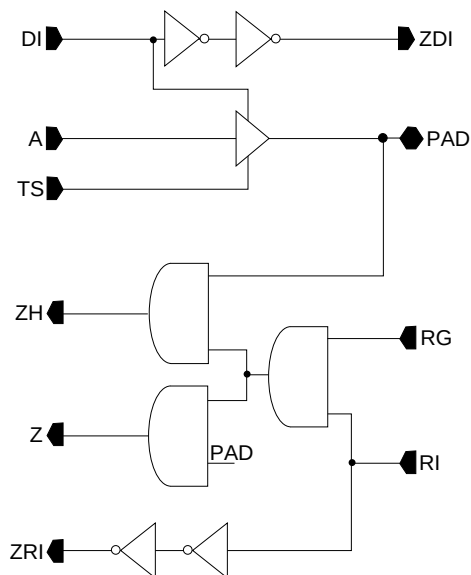
Function: 3.3V LVTTL Nontest 65 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTL off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.322 + 0.054D _{std}	0.956 + 0.041D _{std}	0.731 + 0.034D _{std}
		t _{PHL}	1.262 + 0.054D _{std}	0.864 + 0.039D _{std}	0.649 + 0.033D _{std}
	B	t _{PLH}	1.118 + 0.053D _{std}	0.836 + 0.040D _{std}	0.672 + 0.034D _{std}
		t _{PHL}	1.111 + 0.053D _{std}	0.793 + 0.039D _{std}	0.629 + 0.032D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.282 + 0.002N _{std}	0.168 + 0.001N _{std}	0.097 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.492 + 0.001N _{std}	0.421 + 0.001N _{std}	0.379 + 0.001N _{std}
		t _{PLH}	0.410 + 0.002N _{std}	0.273 + 0.001N _{std}	0.197 + 0.001N _{std}
		t _{PHL}	0.577 + 0.001N _{std}	0.496 + 0.001N _{std}	0.442 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.287 + 0.002N _{std}	0.153 + 0.001N _{std}	0.075 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.493 + 0.001N _{std}	0.431 + 0.001N _{std}	0.388 + 0.000N _{std}
		t _{PLH}	0.417 + 0.002N _{std}	0.263 + 0.001N _{std}	0.181 + 0.001N _{std}
		t _{PHL}	0.579 + 0.001N _{std}	0.508 + 0.001N _{std}	0.453 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.635	11.636
DI	5.395	5.395
PAD (Receiver Input)	367.917	367.917
RG	2.002	2.002
RI	3.154	3.154
TS	4.296	4.297
Internal	346.958	346.474
Cell Units	1 cell	1 cell

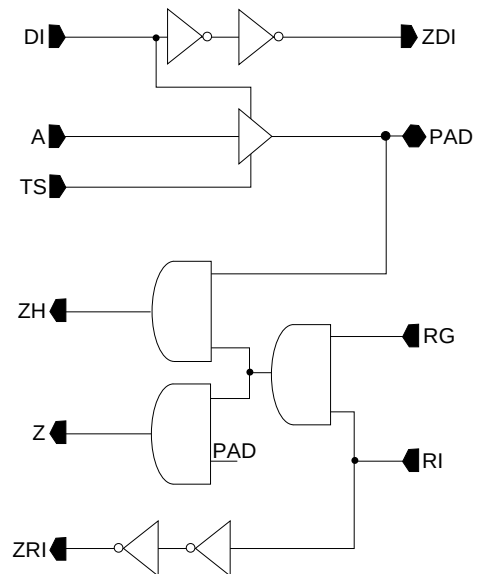
Cell: BT3390, BT3390_PM

Function: 3.3V LVTTTL Nontest 90 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs		
PAD	RI	RG	Z	ZH	ZRI
-	0	-	0	0	RI
-	-	0	0	0	RI
0	1	1	0	0	RI
1	1	1	1	1	RI
Hi-Z	1	1	X	X	RI



Driver Propagation Delays

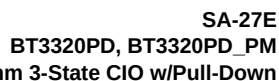
Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.215 + 0.075D _{std}	0.882 + 0.057D _{std}	0.678 + 0.048D _{std}
		t _{PHL}	1.179 + 0.073D _{std}	0.799 + 0.054D _{std}	0.598 + 0.045D _{std}
	B	t _{PLH}	1.001 + 0.075D _{std}	0.765 + 0.056D _{std}	0.629 + 0.048D _{std}
		t _{PHL}	1.077 + 0.071D _{std}	0.795 + 0.052D _{std}	0.648 + 0.044D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.282 + 0.002N _{std}	0.168 + 0.001N _{std}	0.097 + 0.001N _{std}
		t _{PHL}	0.492 + 0.001N _{std}	0.421 + 0.001N _{std}	0.379 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.409 + 0.002N _{std}	0.273 + 0.001N _{std}	0.197 + 0.001N _{std}
		t _{PHL}	0.576 + 0.001N _{std}	0.496 + 0.001N _{std}	0.442 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.287 + 0.002N _{std}	0.153 + 0.001N _{std}	0.075 + 0.001N _{std}
		t _{PHL}	0.493 + 0.001N _{std}	0.431 + 0.001N _{std}	0.388 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.416 + 0.002N _{std}	0.263 + 0.001N _{std}	0.181 + 0.001N _{std}
		t _{PHL}	0.578 + 0.001N _{std}	0.508 + 0.001N _{std}	0.453 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.630	11.638
DI	5.394	5.393
PAD (Receiver Input)	330.250	330.250
RG	2.002	2.002
RI	3.154	3.154
TS	4.294	4.294
Internal	344.000	346.000
Cell Units	1 cell	1 cell

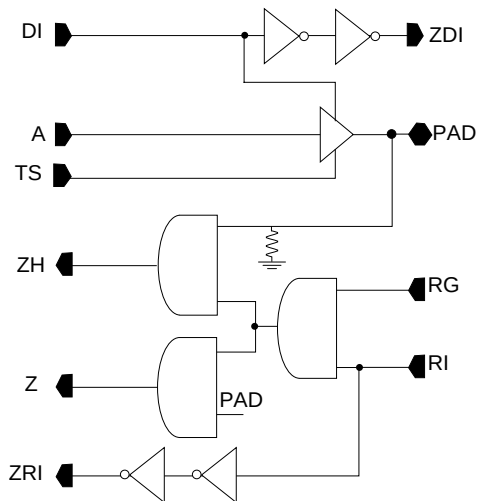


Function: 3.3V LVTTL Nontest 20 Ohm 3-State CIO w/Pull-Down

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
PAD	Driver output/receiver input
ZH	Hysteresis receiver output
Z	Non-hysteresis receiver output
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs		Comments
A	TS	DI	PAD	ZDI	
-	0	-	L	DI	Functional mode
-	-	0	L	DI	Test mode
-	1	1	A	DI	Functional mode

Receiver Truth Table

Inputs			Outputs			Comments
PAD	RI	RG	Z	ZH	ZRI	
-	0	-	0	0	RI	Test mode
-	-	0	0	0	RI	Functional/test mode
0	1	1	0	0	RI	Functional mode
1	1	1	1	1	RI	Functional mode

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.647 + 0.024D _{std}	1.180 + 0.017D _{std}	0.892 + 0.014D _{std}
		t _{PHL}	1.478 + 0.024D _{std}	1.034 + 0.016D _{std}	0.783 + 0.013D _{std}
	B	t _{PLH}	1.505 + 0.021D _{std}	1.066 + 0.016D _{std}	0.810 + 0.012D _{std}
		t _{PHL}	1.383 + 0.022D _{std}	0.956 + 0.015D _{std}	0.724 + 0.011D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.278 + 0.002N _{std}	0.173 + 0.001N _{std}	0.103 + 0.001N _{std}
		t _{PHL}	0.520 + 0.001N _{std}	0.434 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.413 + 0.002N _{std}	0.283 + 0.001N _{std}	0.208 + 0.001N _{std}
		t _{PHL}	0.620 + 0.001N _{std}	0.522 + 0.001N _{std}	0.460 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.284 + 0.002N _{std}	0.158 + 0.001N _{std}	0.080 + 0.001N _{std}
		t _{PHL}	0.522 + 0.001N _{std}	0.444 + 0.001N _{std}	0.397 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.420 + 0.002N _{std}	0.274 + 0.001N _{std}	0.192 + 0.001N _{std}
		t _{PHL}	0.622 + 0.001N _{std}	0.533 + 0.001N _{std}	0.471 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.610	11.609
DI	5.369	5.395
PAD (Receiver Input)	534.958	534.958
RG	2.002	2.002
RI	3.154	3.154
TS	4.297	4.297
Internal	288.291	278.841
Cell Units	1 cell	1 cell

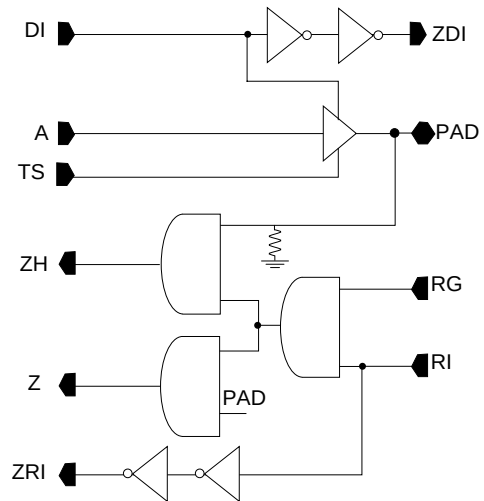
Cell: BT3335PD, BT3335PD_PM

Function: 3.3V LVTTTL Nontest 35 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs		Comments
A	TS	DI	PAD	ZDI	
-	0	-	L	DI	Functional mode
-	-	0	L	DI	Test mode
-	1	1	A	DI	Functional mode



Receiver Truth Table

Inputs			Outputs			Comments
PAD	RI	RG	Z	ZH	ZRI	
-	0	-	0	0	RI	Test mode
-	-	0	0	0	RI	Functional/test mode
0	1	1	0	0	RI	Functional mode
1	1	1	1	1	RI	Functional mode

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.619 + 0.032D _{std}	1.167 + 0.024D _{std}	0.887 + 0.019D _{std}
		t _{PHL}	1.463 + 0.031D _{std}	1.030 + 0.022D _{std}	0.784 + 0.018D _{std}
	B	t _{PLH}	1.440 + 0.030D _{std}	1.037 + 0.022D _{std}	0.800 + 0.018D _{std}
		t _{PHL}	1.344 + 0.030D _{std}	0.945 + 0.021D _{std}	0.727 + 0.017D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.278 + 0.002N _{std}	0.173 + 0.001N _{std}	0.103 + 0.001N _{std}
		t _{PHL}	0.521 + 0.001N _{std}	0.434 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.413 + 0.002N _{std}	0.283 + 0.001N _{std}	0.208 + 0.001N _{std}
		t _{PHL}	0.620 + 0.001N _{std}	0.522 + 0.001N _{std}	0.460 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.284 + 0.002N _{std}	0.158 + 0.001N _{std}	0.080 + 0.001N _{std}
		t _{PHL}	0.522 + 0.001N _{std}	0.444 + 0.001N _{std}	0.397 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.420 + 0.002N _{std}	0.274 + 0.001N _{std}	0.192 + 0.001N _{std}
		t _{PHL}	0.622 + 0.001N _{std}	0.533 + 0.001N _{std}	0.471 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.555	11.555
DI	5.381	5.369
PAD (Receiver Input)	457.583	457.542
RG	2.002	2.002
RI	3.154	3.154
TS	4.300	4.297
Internal	404.504	399.081
Cell Units	1 cell	1 cell

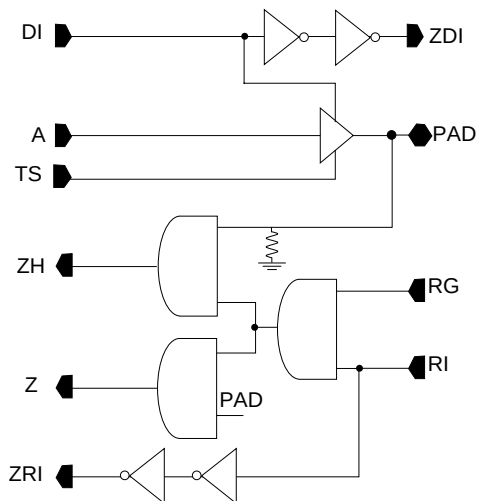
Cell: BT3350PD, BT3350PD_PM

Function: 3.3V LVTTTL Nontest 50 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs		Comments
A	TS	DI	PAD	ZDI	
-	0	-	L	DI	Functional mode
-	-	0	L	DI	Test mode
-	1	1	A	DI	Functional mode

Receiver Truth Table

Inputs			Outputs			Comments
PAD	RI	RG	Z	ZH	ZRI	
-	0	-	0	0	RI	Test mode
-	-	0	0	0	RI	Functional/test mode
0	1	1	0	0	RI	Functional mode
1	1	1	1	1	RI	Functional mode

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$1.494 + 0.042D_{std}$	$1.085 + 0.032D_{std}$	$0.830 + 0.027D_{std}$
		t_{PHL}	$1.388 + 0.041D_{std}$	$0.967 + 0.030D_{std}$	$0.734 + 0.025D_{std}$
	B	t_{PLH}	$1.303 + 0.041D_{std}$	$0.963 + 0.031D_{std}$	$0.763 + 0.026D_{std}$
		t_{PHL}	$1.207 + 0.040D_{std}$	$0.860 + 0.029D_{std}$	$0.671 + 0.024D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.278 + 0.002N _{std}	0.173 + 0.001N _{std}	0.103 + 0.001N _{std}
		t _{PHL}	0.520 + 0.001N _{std}	0.434 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.413 + 0.002N _{std}	0.283 + 0.001N _{std}	0.208 + 0.001N _{std}
		t _{PHL}	0.620 + 0.001N _{std}	0.522 + 0.001N _{std}	0.460 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.284 + 0.002N _{std}	0.158 + 0.001N _{std}	0.080 + 0.001N _{std}
		t _{PHL}	0.522 + 0.001N _{std}	0.444 + 0.001N _{std}	0.397 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.420 + 0.002N _{std}	0.274 + 0.001N _{std}	0.192 + 0.001N _{std}
		t _{PHL}	0.622 + 0.001N _{std}	0.533 + 0.001N _{std}	0.471 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.621	11.620
DI	5.377	5.369
PAD (Receiver Input)	425.750	425.667
RG	2.002	2.002
RI	3.154	3.154
TS	4.297	4.297
Internal	552.033	548.520
Cell Units	1 cell	1 cell

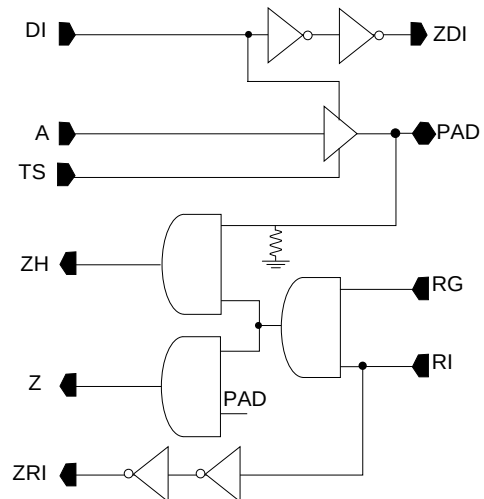
Cell: BT3350LVPD, BT3350LVPD_PM

Function: Low Voltage 3.3V LVTTTL Nontest 50 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces low voltage (as low as 0.9V) internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs		Comments
A	TS	DI	PAD	ZDI	
-	0	-	L	DI	Functional mode
-	-	0	L	DI	Test mode
-	1	1	A	DI	Functional mode



Receiver Truth Table

Inputs			Outputs			Comments
PAD	RI	RG	Z	ZH	ZRI	
-	0	-	0	0	RI	Test mode
-	-	0	0	0	RI	Functional/test mode
0	1	1	0	0	RI	Functional mode
1	1	1	1	1	RI	Functional mode

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	2.225 + 0.046D _{std}	1.610 + 0.035D _{std}	1.229 + 0.029D _{std}
		t _{PHL}	2.267 + 0.041D _{std}	1.560 + 0.030D _{std}	1.164 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.326 + 0.001N _{std}	0.186 + 0.001N _{std}	0.110 + 0.000N _{std}
		t _{PHL}	0.596 + 0.001N _{std}	0.471 + 0.000N _{std}	0.408 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.448 + 0.001N _{std}	0.291 + 0.001N _{std}	0.212 + 0.000N _{std}
		t _{PHL}	0.683 + 0.001N _{std}	0.549 + 0.000N _{std}	0.475 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	27.038
DI	5.302
PAD (Receiver Input)	447.708
RG	2.336
RI	3.533
TS	4.385
Internal	552.047
Cell Units	1 cell

Cell: BT3365PD, BT3365PD_PM

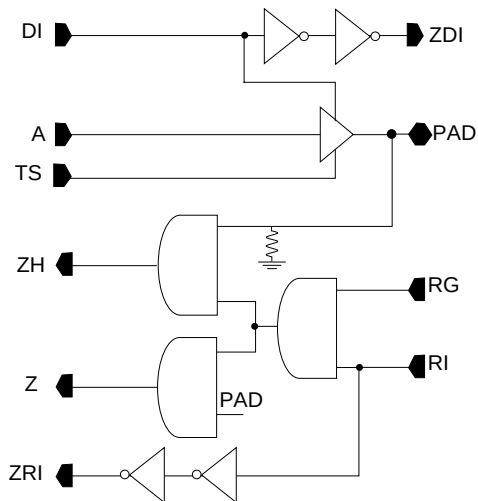
Function: 3.3V LVTTTL Nontest 65 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Driver Truth Table

Inputs			Outputs		Comments
A	TS	DI	PAD	ZDI	
-	0	-	L	DI	Functional mode
-	-	0	L	DI	Test mode
-	1	1	A	DI	Functional mode

Receiver Truth Table

Inputs			Outputs			Comments
PAD	RI	RG	Z	ZH	ZRI	
-	0	-	0	0	RI	Test mode
-	-	0	0	0	RI	Functional/test mode
0	1	1	0	0	RI	Functional mode
1	1	1	1	1	RI	Functional mode

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$1.324 + 0.054D_{std}$	$0.959 + 0.041D_{std}$	$0.734 + 0.034D_{std}$
		t_{PHL}	$1.256 + 0.053D_{std}$	$0.857 + 0.038D_{std}$	$0.643 + 0.032D_{std}$
	B	t_{PLH}	$1.117 + 0.053D_{std}$	$0.835 + 0.040D_{std}$	$0.676 + 0.034D_{std}$
		t_{PHL}	$1.109 + 0.052D_{std}$	$0.789 + 0.038D_{std}$	$0.617 + 0.032D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.278 + 0.002N _{std}	0.173 + 0.001N _{std}	0.102 + 0.001N _{std}
		t _{PHL}	0.520 + 0.001N _{std}	0.433 + 0.001N _{std}	0.386 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.413 + 0.002N _{std}	0.283 + 0.001N _{std}	0.207 + 0.001N _{std}
		t _{PHL}	0.620 + 0.001N _{std}	0.522 + 0.001N _{std}	0.460 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.284 + 0.002N _{std}	0.157 + 0.001N _{std}	0.080 + 0.001N _{std}
		t _{PHL}	0.521 + 0.001N _{std}	0.443 + 0.001N _{std}	0.396 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.420 + 0.002N _{std}	0.274 + 0.001N _{std}	0.192 + 0.001N _{std}
		t _{PHL}	0.622 + 0.001N _{std}	0.533 + 0.001N _{std}	0.471 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.621	11.617
DI	5.377	5.381
PAD (Receiver Input)	368.667	368.667
RG	2.002	2.002
RI	3.154	3.154
TS	4.297	4.297
Internal	706.112	704.091
Cell Units	1 cell	1 cell

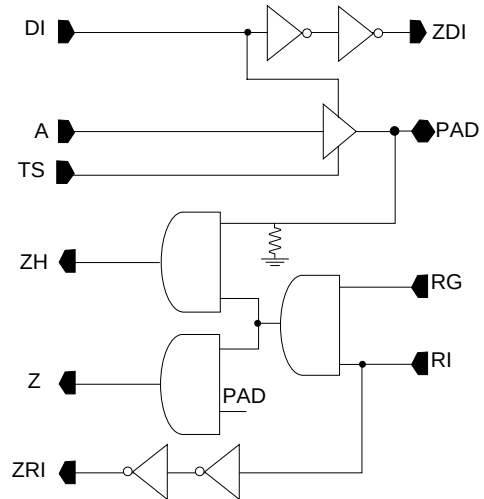
Cell: BT3390PD, BT3390PD_PM

Function: 3.3V LVTTTL Nontest 90 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Pin Group: (Z, ZH): (1, 2)

Driver Truth Table

Inputs			Outputs		Comments
A	TS	DI	PAD	ZDI	
-	0	-	L	DI	Functional mode
-	-	0	L	DI	Test mode
-	1	1	A	DI	Functional mode



Receiver Truth Table

Inputs			Outputs			Comments
PAD	RI	RG	Z	ZH	ZRI	
-	0	-	0	0	RI	Test mode
-	-	0	0	0	RI	Functional/test mode
0	1	1	0	0	RI	Functional mode
1	1	1	1	1	RI	Functional mode

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.215 + 0.075D _{std}	0.882 + 0.057D _{std}	0.678 + 0.048D _{std}
		t _{PHL}	1.179 + 0.073D _{std}	0.799 + 0.054D _{std}	0.598 + 0.045D _{std}
	B	t _{PLH}	1.001 + 0.075D _{std}	0.765 + 0.056D _{std}	0.629 + 0.048D _{std}
		t _{PHL}	1.077 + 0.071D _{std}	0.795 + 0.052D _{std}	0.648 + 0.044D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.278 + 0.002N _{std}	0.173 + 0.001N _{std}	0.102 + 0.001N _{std}
		t _{PHL}	0.520 + 0.001N _{std}	0.433 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.412 + 0.002N _{std}	0.283 + 0.001N _{std}	0.207 + 0.001N _{std}
		t _{PHL}	0.619 + 0.001N _{std}	0.521 + 0.001N _{std}	0.460 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.284 + 0.002N _{std}	0.157 + 0.001N _{std}	0.080 + 0.001N _{std}
		t _{PHL}	0.521 + 0.001N _{std}	0.443 + 0.001N _{std}	0.396 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.419 + 0.002N _{std}	0.274 + 0.001N _{std}	0.191 + 0.001N _{std}
		t _{PHL}	0.621 + 0.001N _{std}	0.533 + 0.001N _{std}	0.470 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.620	11.623
DI	5.376	5.376
PAD (Receiver Input)	331.125	331.125
RG	2.002	2.002
RI	3.154	3.154
TS	4.297	4.297
Internal	668.000	672.000
Cell Units	1 cell	1 cell

Cell: BT3320PU, BT3320PU_PM

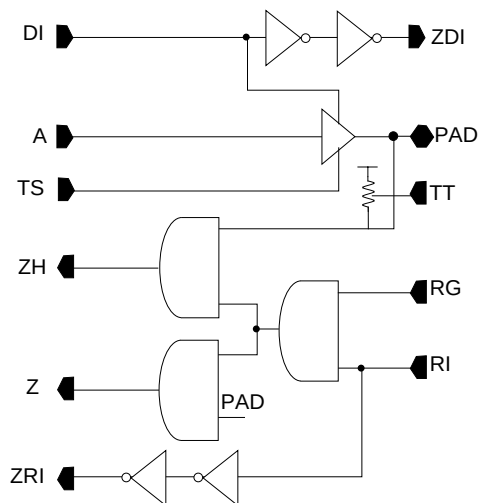
Function: 3.3V LVTTL Nontest 20 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTL off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, and Z must be wired to latches for boundary-scan. PAD is pulled up to logic "1" (3.3V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. If RG is used, it must be wired to a latch for boundary-scan. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1, H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$1.636 + 0.024D_{std}$	$1.171 + 0.017D_{std}$	$0.885 + 0.014D_{std}$
		t_{PHL}	$1.488 + 0.024D_{std}$	$1.043 + 0.016D_{std}$	$0.790 + 0.013D_{std}$
	B	t_{PLH}	$1.497 + 0.021D_{std}$	$1.060 + 0.015D_{std}$	$0.807 + 0.012D_{std}$
		t_{PHL}	$1.390 + 0.022D_{std}$	$0.962 + 0.015D_{std}$	$0.729 + 0.011D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^{\circ}C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.271 + 0.002N_{std}$	$0.154 + 0.001N_{std}$	$0.083 + 0.001N_{std}$
		t_{PHL}	$0.502 + 0.001N_{std}$	$0.433 + 0.001N_{std}$	$0.392 + 0.001N_{std}$
PAD-ZH		t_{PLH}	$0.401 + 0.002N_{std}$	$0.261 + 0.001N_{std}$	$0.184 + 0.001N_{std}$
		t_{PHL}	$0.585 + 0.001N_{std}$	$0.508 + 0.001N_{std}$	$0.455 + 0.001N_{std}$



Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.276 + 0.002N _{std}	0.137 + 0.001N _{std}	0.058 + 0.001N _{std}
		t _{PHL}	0.503 + 0.001N _{std}	0.446 + 0.001N _{std}	0.404 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.408 + 0.002N _{std}	0.250 + 0.001N _{std}	0.166 + 0.001N _{std}
		t _{PHL}	0.587 + 0.001N _{std}	0.522 + 0.001N _{std}	0.468 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.623	11.623
DI	5.393	5.393
PAD (Receiver Input)	536.083	536.167
RG	2.002	2.002
RI	3.154	3.154
TS	4.298	4.299
TT	8.386	8.376
Internal	169.282	165.690
Cell Units	1 cell	1 cell

Cell: BT3335PU, BT3335PU_PM

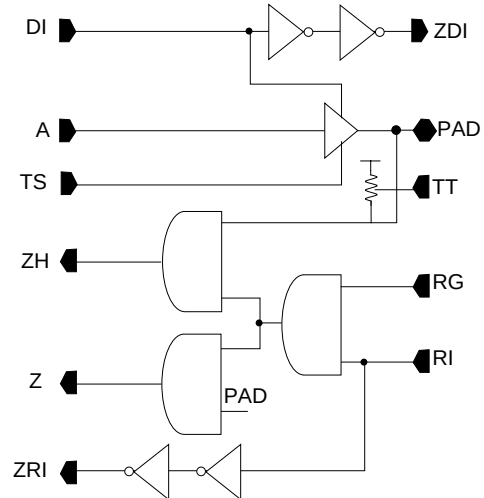
Function: 3.3V LVTTTL Nontest 35 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, and Z must be wired to latches for boundary-scan. PAD is pulled up to logic "1" (3.3V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. If RG is used, it must be wired to a latch for boundary-scan. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1, H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$1.608 + 0.031D_{std}$	$1.156 + 0.023D_{std}$	$0.878 + 0.019D_{std}$
		t_{PHL}	$1.473 + 0.032D_{std}$	$1.039 + 0.022D_{std}$	$0.792 + 0.018D_{std}$
	B	t_{PLH}	$1.433 + 0.029D_{std}$	$1.030 + 0.022D_{std}$	$0.795 + 0.018D_{std}$
		t_{PHL}	$1.351 + 0.030D_{std}$	$0.952 + 0.021D_{std}$	$0.734 + 0.017D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^{\circ}C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.271 + 0.002N_{std}$	$0.154 + 0.001N_{std}$	$0.083 + 0.001N_{std}$
		t_{PHL}	$0.502 + 0.001N_{std}$	$0.433 + 0.001N_{std}$	$0.392 + 0.001N_{std}$
PAD-ZH		t_{PLH}	$0.401 + 0.002N_{std}$	$0.261 + 0.001N_{std}$	$0.184 + 0.001N_{std}$
		t_{PHL}	$0.585 + 0.001N_{std}$	$0.508 + 0.001N_{std}$	$0.455 + 0.001N_{std}$



Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.276 + 0.002N _{std}	0.137 + 0.001N _{std}	0.058 + 0.001N _{std}
		t _{PHL}	0.503 + 0.001N _{std}	0.446 + 0.001N _{std}	0.404 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.408 + 0.002N _{std}	0.250 + 0.001N _{std}	0.166 + 0.001N _{std}
		t _{PHL}	0.587 + 0.001N _{std}	0.522 + 0.001N _{std}	0.468 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.570	11.569
DI	5.393	5.394
PAD (Receiver Input)	458.625	458.583
RG	2.002	2.002
RI	3.154	3.154
TS	4.297	4.297
TT	8.386	8.376
Internal	220.801	218.881
Cell Units	1 cell	1 cell

Cell: BT3350PU, BT3350PU_PM

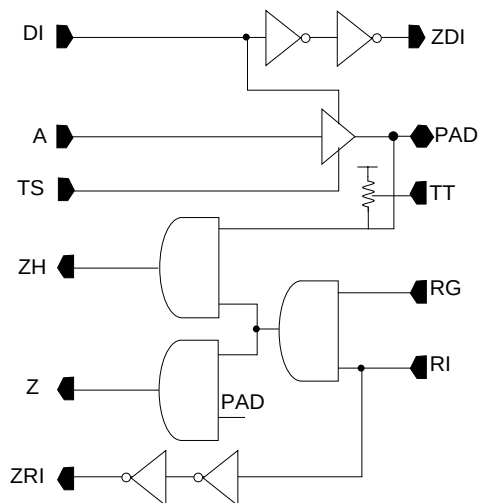
Function: 3.3V LVTTL Nontest 50 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTL off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, and Z must be wired to latches for boundary-scan. PAD is pulled up to logic "1" (3.3V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. If RG is used, it must be wired to a latch for boundary-scan. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1, H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$1.482 + 0.041D_{std}$	$1.074 + 0.031D_{std}$	$0.821 + 0.026D_{std}$
		t_{PHL}	$1.397 + 0.042D_{std}$	$0.977 + 0.031D_{std}$	$0.743 + 0.026D_{std}$
	B	t_{PLH}	$1.297 + 0.040D_{std}$	$0.956 + 0.030D_{std}$	$0.755 + 0.025D_{std}$
		t_{PHL}	$1.210 + 0.041D_{std}$	$0.866 + 0.030D_{std}$	$0.678 + 0.025D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^{\circ}C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.271 + 0.002N_{std}$	$0.154 + 0.001N_{std}$	$0.082 + 0.001N_{std}$
		t_{PHL}	$0.502 + 0.001N_{std}$	$0.433 + 0.001N_{std}$	$0.392 + 0.001N_{std}$
PAD-ZH		t_{PLH}	$0.401 + 0.002N_{std}$	$0.261 + 0.001N_{std}$	$0.184 + 0.001N_{std}$
		t_{PHL}	$0.585 + 0.001N_{std}$	$0.508 + 0.001N_{std}$	$0.455 + 0.001N_{std}$



Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.276 + 0.002N _{std}	0.137 + 0.001N _{std}	0.058 + 0.001N _{std}
		t _{PHL}	0.503 + 0.001N _{std}	0.446 + 0.001N _{std}	0.404 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.408 + 0.002N _{std}	0.250 + 0.001N _{std}	0.166 + 0.001N _{std}
		t _{PHL}	0.587 + 0.001N _{std}	0.521 + 0.001N _{std}	0.468 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.635	11.635
DI	5.395	5.393
PAD (Receiver Input)	426.708	426.750
RG	2.002	2.002
RI	3.154	3.154
TS	4.298	4.298
TT	8.386	8.386
Internal	282.797	280.944
Cell Units	1 cell	1 cell

Cell: BT3350LVPU, BT3350LVPU_PM

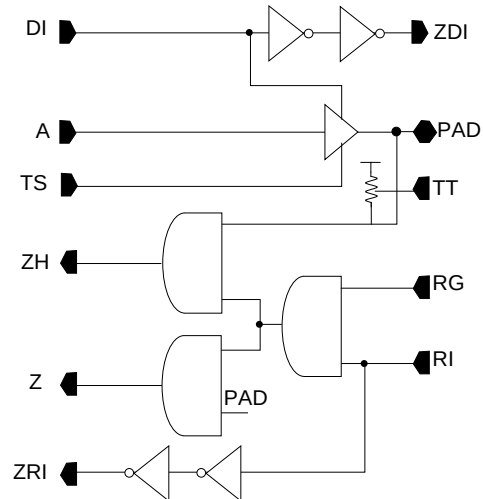
Function: Low Voltage 3.3V LVTTTL Nontest 50 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces low voltage (as low as 0.9V) internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, and Z must be wired to latches for boundary-scan. PAD is pulled up to logic "1" (3.3V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. If RG is used, it must be wired to a latch for boundary-scan. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1,H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$2.191 + 0.045D_{std}$	$1.579 + 0.034D_{std}$	$1.204 + 0.029D_{std}$
		t_{PHL}	$2.274 + 0.042D_{std}$	$1.569 + 0.031D_{std}$	$1.171 + 0.026D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.315 + 0.001N _{std}	0.157 + 0.001N _{std}	0.075 + 0.000N _{std}
		t _{PHL}	0.607 + 0.001N _{std}	0.496 + 0.000N _{std}	0.438 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.427 + 0.001N _{std}	0.257 + 0.001N _{std}	0.175 + 0.000N _{std}
		t _{PHL}	0.664 + 0.001N _{std}	0.550 + 0.000N _{std}	0.486 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	27.038
DI	5.319
PAD (Receiver Input)	447.208
RG	2.354
RI	3.537
TS	4.396
TT	12.477
Internal	382.764
Cell Units	1 cell

Cell: BT3365PU, BT3365PU_PM

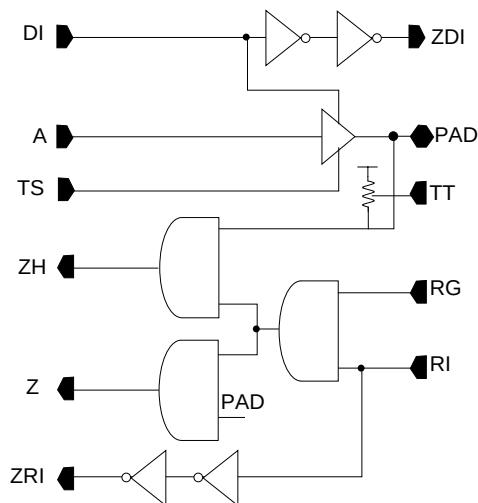
Function: 3.3V LVTTL Nontest 65 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTL off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, and Z must be wired to latches for boundary-scan. PAD is pulled up to logic "1" (3.3V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. If RG is used, it must be wired to a latch for boundary-scan. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1, H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.314 + 0.053D_{std}$	$0.949 + 0.040D_{std}$	$0.725 + 0.033D_{std}$
		t_{PHL}	$1.260 + 0.055D_{std}$	$0.864 + 0.040D_{std}$	$0.650 + 0.033D_{std}$
	B	t_{PLH}	$1.114 + 0.052D_{std}$	$0.830 + 0.039D_{std}$	$0.668 + 0.033D_{std}$
		t_{PHL}	$1.107 + 0.054D_{std}$	$0.797 + 0.039D_{std}$	$0.631 + 0.033D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.270 + 0.002N_{std}$	$0.154 + 0.001N_{std}$	$0.083 + 0.001N_{std}$
		t_{PHL}	$0.502 + 0.001N_{std}$	$0.433 + 0.001N_{std}$	$0.392 + 0.001N_{std}$
PAD-ZH		t_{PLH}	$0.401 + 0.002N_{std}$	$0.261 + 0.001N_{std}$	$0.184 + 0.001N_{std}$
		t_{PHL}	$0.585 + 0.001N_{std}$	$0.508 + 0.001N_{std}$	$0.455 + 0.001N_{std}$



Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.276 + 0.002N _{std}	0.137 + 0.001N _{std}	0.058 + 0.001N _{std}
		t _{PHL}	0.503 + 0.001N _{std}	0.446 + 0.001N _{std}	0.404 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.408 + 0.002N _{std}	0.250 + 0.001N _{std}	0.166 + 0.001N _{std}
		t _{PHL}	0.587 + 0.001N _{std}	0.521 + 0.001N _{std}	0.468 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.631	11.637
DI	5.395	5.395
PAD (Receiver Input)	369.750	369.750
RG	2.002	2.002
RI	3.154	3.154
TS	4.299	4.298
TT	8.386	8.386
Internal	346.950	346.522
Cell Units	1 cell	1 cell

Cell: BT3390PU, BT3390PU_PM

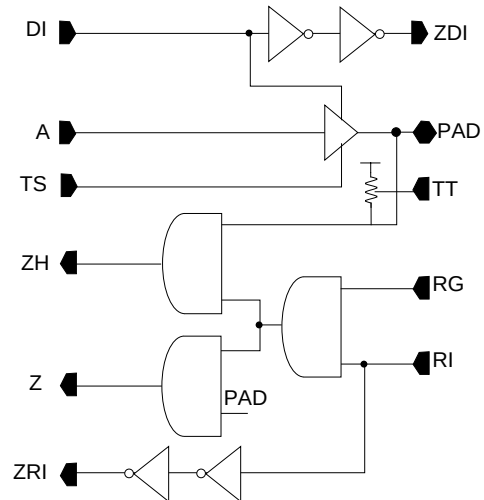
Function: 3.3V LVTTTL Nontest 90 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. A, TS, and Z must be wired to latches for boundary-scan. PAD is pulled up to logic "1" (3.3V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. If RG is used, it must be wired to a latch for boundary-scan. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)

Pin Group: (Z, ZH): (1, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs				Outputs		
PAD	RI	RG	TT	Z	ZH	ZRI
-	0	-	-	0	0	RI
-	-	0	-	0	0	RI
0	1	1	-	0	0	RI
1, H	1	1	-	1	1	RI
Hi-Z	1	1	0	X	X	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.209 + 0.073D _{std}	0.936 + 0.055D _{std}	0.765 + 0.047D _{std}
		t _{PHL}	1.199 + 0.073D _{std}	0.898 + 0.053D _{std}	0.730 + 0.045D _{std}
	B	t _{PLH}	0.985 + 0.073D _{std}	0.756 + 0.055D _{std}	0.628 + 0.046D _{std}
		t _{PHL}	1.075 + 0.072D _{std}	0.790 + 0.053D _{std}	0.643 + 0.045D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.270 + 0.002N _{std}	0.154 + 0.001N _{std}	0.083 + 0.001N _{std}
		t _{PHL}	0.502 + 0.001N _{std}	0.433 + 0.001N _{std}	0.392 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.401 + 0.002N _{std}	0.261 + 0.001N _{std}	0.184 + 0.001N _{std}
		t _{PHL}	0.585 + 0.001N _{std}	0.508 + 0.001N _{std}	0.455 + 0.001N _{std}



Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.276 + 0.002N _{std}	0.137 + 0.001N _{std}	0.058 + 0.001N _{std}
		t _{PHL}	0.503 + 0.001N _{std}	0.446 + 0.001N _{std}	0.404 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.408 + 0.002N _{std}	0.250 + 0.001N _{std}	0.166 + 0.001N _{std}
		t _{PHL}	0.586 + 0.001N _{std}	0.521 + 0.001N _{std}	0.468 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.630	11.628
DI	5.365	5.365
PAD (Receiver Input)	332.167	332.167
RG	2.002	2.002
RI	3.154	3.154
TS	4.299	4.298
TT	8.386	8.386
Internal	498.919	498.919
Cell Units	1 cell	1 cell

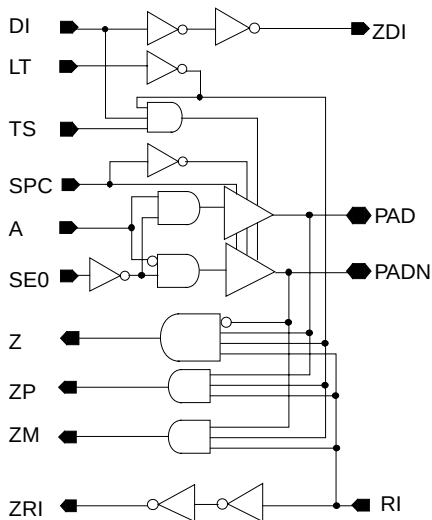
Cell: BUSB2

Function: USB Nontest 3-State CIO

Description:

Noninverting, fully differential driver/receiver used to drive/receive complementary signals according to Universal Serial Bus Specification Revision 1.1. This I/O requires the 3.3V power supply, V_{dd330} .

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RI	Receiver inhibit input (RI in)
LT	DC current gate (I_{dd} test) input
SE0	Single-ended zero input
SPC	Full (low) speed select '1' set full speed; '0' set low speed
PAD	D+ driver output/receiver input
PADN	D- driver output/receiver input
Z	Differential receiver output
ZP	D+ receiver output
ZM	D- receiver output
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)



Driver Truth Table

Inputs						Outputs		
A	TS	DI	LT	SE0	SPC	PAD	PADN	ZDI
-	0	-	-	-	-	Hi-Z	Hi-Z	DI
-	-	0	-	-	-	Hi-Z	Hi-Z	DI
-	-	-	1	-	-	Hi-Z	Hi-Z	DI
1	1	1	0	0	-	1	0	DI
0	1	1	0	0	-	0	1	DI
-	1	1	0	1	-	0	0	DI

Receiver Truth Table

Inputs				Outputs			
PAD	PADN	LT	RI	Z	ZP	ZM	ZRI
1	0	0	1	1	1	0	RI
0	1	0	1	0	0	1	RI
0	0	0	1	x	0	0	RI
-	-	0	0	0	0	0	RI
-	-	1	-	0	0	0	RI

Usage Notes:

1. The pull-up is a USB requirement to allow the host to identify the device type.
2. Termination must be one of the following:
 - On the downstream end of the cable, the pull-up terminator (1.5k ohm to V_{dd}) is needed on the PAD line.
 - On the upstream end of the cable, the pull-down terminator (15k ohm to GND) is needed on the PAD and PADN lines.
3. If the input to the receiver is unknown (Hi-Z), then the output is indeterminate.

Low Speed Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$109.686 + 0.442D_{std}$	$84.975 + 0.249D_{std}$	$70.080 + 0.172D_{std}$
		t_{PHL}	$106.697 + 0.452D_{std}$	$84.793 + 0.249D_{std}$	$69.929 + 0.172D_{std}$

Full Speed Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$6.155 + 0.053N_{std}$	$4.266 + 0.036N_{std}$	$3.293 + 0.028N_{std}$
		t_{PHL}	$6.205 + 0.053N_{std}$	$4.309 + 0.036N_{std}$	$3.354 + 0.028N_{std}$



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	4.383 + 0.023N _{std}	2.650 + 0.017N _{std}	1.948 + 0.013N _{std}
		t _{PHL}	4.076 + 0.006N _{std}	2.437 + 0.005N _{std}	1.805 + 0.005N _{std}
PAD-ZP		t _{PLH}	0.536 + 0.016N _{std}	0.468 + 0.011N _{std}	0.471 + 0.009N _{std}
		t _{PHL}	0.678 + 0.005N _{std}	0.531 + 0.003N _{std}	0.393 + 0.002N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	3.262
DI	4.472
LT	3.105
PAD (Receiver Input)	633.917
PADN (Receiver Input)	636.167
RI	3.522
SE0	4.194
SPC	2.426
TS	2.172
Internal	390.00
Cell Units	2 cells

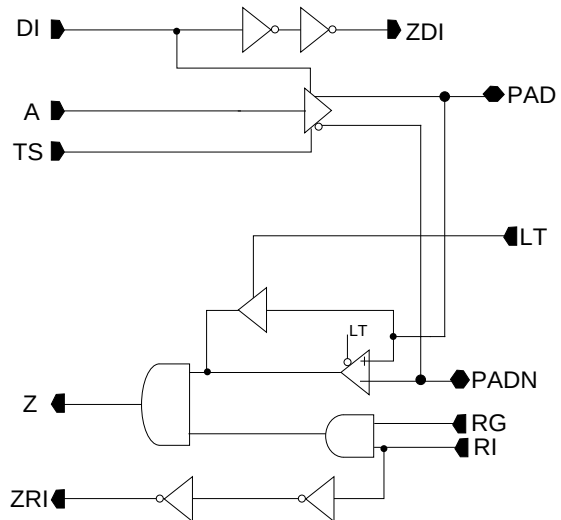
Cell: IHSTL, IHSTL_PM

Function: HSTL Nontest Differential Receiver

Description:

Noninverting differential receiver used to receive complementary 1.8V HSTL signals. A differential termination between PAD and PADN inputs is recommended. This receiver requires only a 1.8V V_{dd} supply. A driver is provided for AC wrap test. This driver must be disabled during system mode.

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RI	Receiver inhibit input (RI in)
RG	Receiver gate control
LT	DC current gate (I_{dd} test) input
PAD	In-phase receiver input
PADN	Out-phase receiver input
Z	Receiver output
ZRI	Receiver inhibit output (RI out)
ZDI	Driver inhibit output (DI out)



Wrap Driver Truth Table

Inputs			Outputs		
A	TS	DI	PAD	PADN	ZDI
-	0	-	Hi-Z	Hi-Z	DI
-	-	0	Hi-Z	Hi-Z	DI
-	1	1	A	$\bar{A}$	DI



Receiver Truth Table

Inputs					Outputs		Comments
PAD	PADN	LT	RI	RG	Z	ZRI	
-	-	-	0	-	0	RI	Test mode
-	-	-	-	0	0	RI	Test mode
0 ¹	1	0	1	1	0	RI	Functional mode
1 ¹	0	0	1	1	1	RI	Functional mode
1 ¹	1	0	1	1	X	RI	Functional mode
0 ¹	0	0	1	1	X	RI	Functional mode
_2	-	1	1	1	PAD	RI	Bypass mode

¹. PAD input requires HSTL levels.

². PAD input requires CMOS levels.

Usage Notes:

1. The wrap driver in this circuit is only used during wrap test with a CMOS output level and is not intended for functional use.

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.535 + 0.001N _{std}	0.327 + 0.001N _{std}	0.181 + 0.000N _{std}
		t _{PHL}	0.536 + 0.001N _{std}	0.344 + 0.001N _{std}	0.211 + 0.001N _{std}
PADN-Z		t _{PLH}	0.535 + 0.001N _{std}	0.327 + 0.001N _{std}	0.181 + 0.000N _{std}
		t _{PHL}	0.536 + 0.001N _{std}	0.344 + 0.001N _{std}	0.211 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	31.787
DI	3.779
LT	3.300
PAD (Receiver Input)	362.333
PADN (Receiver Input)	364.333
RG	7.342
RI	6.423
TS	3.121
Internal	383.194
Cell Units	2 cells

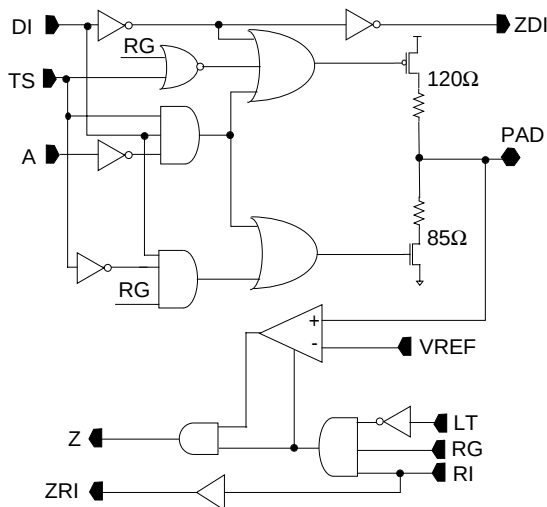
Cell: IHSTLTERM, IHSTLTERM_PM

Function: 1.5V HSTL Receiver with Termination

Description:

HSTL receiver that operates off $V_{dd} = 1.8V$. Receiver provides $50\ \Omega$ termination to $0.417 \cdot V_{dd}$ (0.75V) through on-chip termination. Driver (present for test purposes only) is integrated with termination. A, TS, Z and RG must have a boundary-scan structure.

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input
LT	DC current gate (I_{dd} test) input
RI	Receiver inhibit input
RG	Receiver gate control
VREF	Voltage reference input
PAD	Driver output/receiver input
ZDI	DI output
ZRI	RI output
Z	Receiver output



Usage Notes:

1. Termination will be tested parametrically (rather than functionally).
2. A VREF signal of 0.75V must be applied through the VHSTLR1 and VHSTLR2 cells.

Receiver Truth Table

PAD	LT	RI	RG	Z	Comment
-	-	-	0	0	Test mode
-	-	0	-	0	Test mode
-	1	-	-	0	Test mode
-	0	1	1	PAD	Functional mode

Combined Driver-Termination Truth Table

A	DI	TS	RG	PAD	Termination	Comment
-	0	-	-	Hi-Z	Open circuit	Tested
-	-	0	0	Hi-Z	Open circuit	Tested
0	1	1	-	0	85 Ω to V_{ss}	Tested
1	1	1	-	1	120 Ω to V_{dd}	Tested
-	1	0	1	Note ¹	50 Ω to 0.417* V_{dd}	Functional (untested)

¹. Hi-Z for logic simulation purposes.

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.402 + 0.001N_{std}$	$0.265 + 0.001N_{std}$	$0.184 + 0.000N_{std}$
		t_{PHL}	$0.461 + 0.001N_{std}$	$0.287 + 0.001N_{std}$	$0.186 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	1.245
DI	4.793
LT	3.007
PAD (Receiver Input)	309.083
RG	5.964
RI	4.029
TS	5.670
VREF	108.600
Internal	408.063
Cell Units	1 cell

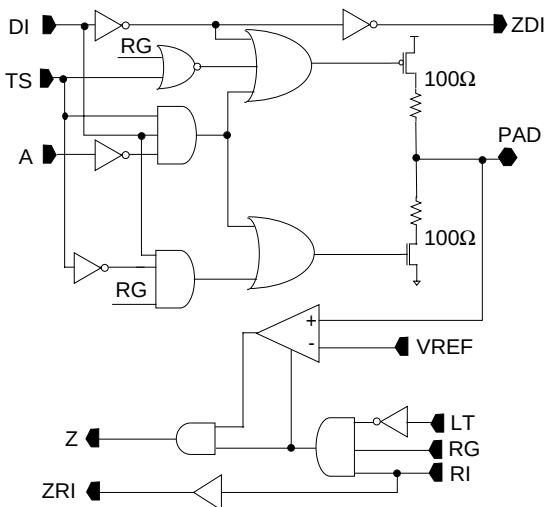
Cell: IHSTL18TERM, IHSTL18TERM_PM

Function: 1.8V HSTL Nontest Receiver with Termination

Description:

HSTL receiver that operates off $V_{dd} = 1.8V$. Receiver provides 50Ω termination to $0.5 \cdot V_{dd}$ through on-chip termination. Driver (present for test purposes only) is integrated with termination. A, TS, Z and RG must have a boundary-scan structure.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input
- LT DC current gate (I_{dd} test) input
- RI Receiver inhibit input
- RG Receiver gate control
- VREF Voltage reference input
- PAD Driver output/receiver input
- ZDI DI output
- ZRI RI output
- Z Receiver output



Usage Notes:

1. Termination will be tested parametrically (rather than functionally).
2. A VREF signal of 0.90V must be applied through the VHSTL18R1 and VHSTL18R2 cells.

Receiver Truth Table

PAD	LT	RI	RG	Z	Comment
-	-	-	0	0	Test mode
-	-	0	-	0	Test mode
-	1	-	-	0	Test mode
-	0	1	1	PAD	Functional mode

Combined Driver-Termination Truth Table

A	DI	TS	RG	PAD	Termination	Comment
-	0	-	-	Hi-Z	Open circuit	Tested
-	-	0	0	Hi-Z	Open circuit	Tested
0	1	1	-	0	100Ω to V _{ss}	Tested
1	1	1	-	1	100Ω to V _{dd}	Tested
-	1	0	1	Note ¹	50Ω to 0.5*V _{dd}	Functional (untested)

¹. Hi-Z for logic simulation purposes.

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.509 + 0.001N _{std}	0.352 + 0.001N _{std}	0.276 + 0.000N _{std}
		t _{PHL}	0.505 + 0.001N _{std}	0.323 + 0.001N _{std}	0.198 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	1.263
DI	3.947
LT	3.050
PAD (Receiver Input)	308.292
RG	6.001
RI	4.032
TS	5.701
VREF	111.467
Internal	390.763
Cell Units	1 cell

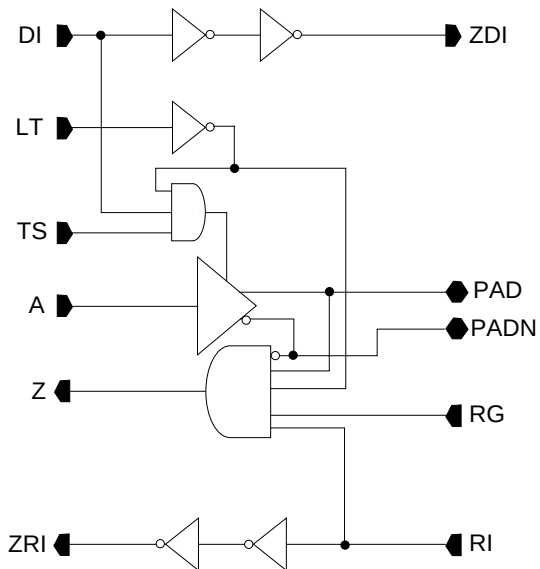
Cell: ILVDS, ILVDS_PM

Function: 1.8V Nontest LVDS Wide Common Mode Receiver

Description:

Noninverting differential receiver that interfaces off-chip unidirectional LVDS data buses with 1.8V internal logic. Receiver has a wide input common mode ranging from 0V to V_{dd} supply. A differential driver is provided for AC wrap test. Driver must be disabled during system mode.

- A Wrap driver input
- TS Driver three-state control
- DI Driver inhibit in (DI1 in)
- RI Receiver inhibit in (RI in)
- RG Receiver gate control
- LT DC current gate (I_{dd} test) input
- PAD In-phase receiver in
- PADN Out-phase receiver in
- Z Receiver out
- ZRI Receiver inhibit out (RI out)
- ZDI Driver inhibit out (DI1 out)



Wrap Driver Truth Table

Inputs			Outputs			Comments
A	TS	DI	PAD	PADN	ZDI	
-	0	-	Hi-Z	Hi-Z	DI	Functional/test mode
-	-	0	Hi-Z	Hi-Z	DI	Test mode
-	-	-	Hi-Z	Hi-Z	DI	Test mode
-	1	1	A	$\bar{A}$	DI	Test mode

Receiver Truth Table

Inputs					Outputs		Comments
PAD	PADN	LT	RI	RG	Z	ZRI	
0	1	0	1	1	0	RI	Functional mode
1	0	0	1	1	1	RI	Functional mode
1	1	0	1	1	X	RI	Functional mode
0	0	0	1	1	X	RI	Functional mode
-	-	-	-	0	0	RI	Functional mode/test mode (rec power off)
-	-	-	0	-	0	RI	Test mode
-	-	1	-	-	0	RI	Test mode

Usage Notes:

1. Driver is designed to be used only as “wrap driver” during I/O AC wrap test. It must be three-stated (Hi-Z) during functional/system mode.
2. Receiver can accommodate a very wide common mode ranging from V_{dd} to 0V. Minimum input swing requires ± 50 mV around the common mode voltage. See “LVDS Receiver DC Specifications” on page 124 for more details.
3. An off-chip 100 ohm terminator is required between the PAD and PADN inputs of the receiver when used with OLVDS. Use ILVDS if on-chip terminator is desired.

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.478 + 0.001N_{std}$	$0.287 + 0.001N_{std}$	$0.180 + 0.001N_{std}$
		t_{PHL}	$0.487 + 0.001N_{std}$	$0.297 + 0.001N_{std}$	$0.187 + 0.001N_{std}$
	B	t_{PLH}	$0.439 + 0.001N_{std}$	$0.258 + 0.001N_{std}$	$0.158 + 0.001N_{std}$
		t_{PHL}	$0.465 + 0.001N_{std}$	$0.279 + 0.001N_{std}$	$0.174 + 0.001N_{std}$



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	17.512	18.606
DI	8.491	4.984
LT	6.956	5.567
PAD (Receiver Input)	201.000	212.667
PADN (Receiver Input)	208.500	219.167
RG	4.754	4.585
RI	7.626	7.622
TS	7.597	4.165
Internal	138.669	194.832
Cell Units	2 cells	2 cells

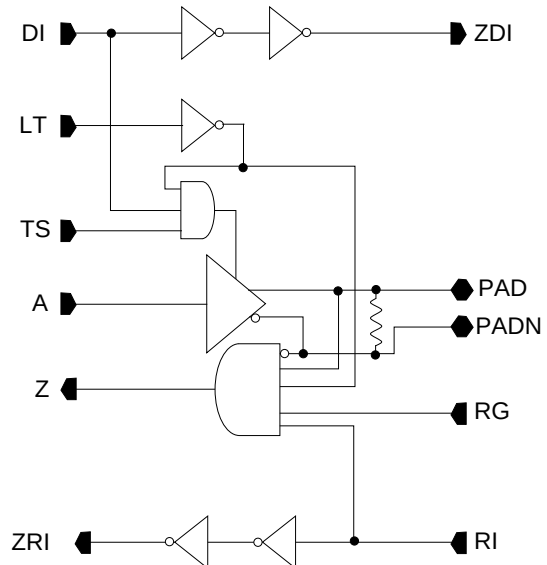
Cell: ILVDS, ILVDS_PM

Function: 1.8V Nontest LVDS Wide Common Mode Receiver w/Terminator

Description:

Noninverting differential receiver that interfaces between off-chip unidirectional LVDS data buses and 1.8V internal logic. An on-chip differential terminator of 100 ohm between PAD and PADN inputs is provided. Receiver has wide input common mode ranging from 0V to V_{dd} supply. A differential driver is provided for AC wrap test. Driver must be disabled during system mode.

- A Wrap driver input
- TS Driver three-state control
- DI Driver inhibit in (DI1 in)
- RI Receiver inhibit in (RI in)
- RG Receiver gate control
- LT DC current gate (I_{dd} test) input
- PAD In-phase receiver in
- PADN Out-phase receiver in
- Z Receiver out
- ZRI Receiver inhibit out (RI out)
- ZDI Driver inhibit out (DI1 out)



Wrap Driver Truth Table

Inputs			Outputs			Comments
A	TS	DI	PAD	PADN	ZDI	
-	0	-	Hi-Z	Hi-Z	DI	Functional/test mode
-	-	0	Hi-Z	Hi-Z	DI	Test mode
-	-	-	Hi-Z	Hi-Z	DI	Test mode
-	1	1	A	$\bar{A}$	DI	Test mode



Receiver Truth Table

Inputs					Outputs		Comments
PAD	PADN	LT	RI	RG	Z	ZRI	
0	1	0	1	1	0	RI	Functional mode
1	0	0	1	1	1	RI	Functional mode
1	1	0	1	1	X	RI	Functional mode
0	0	0	1	1	X	RI	Functional mode
-	-	-	-	0	0	RI	Functional mode/test mode (rec power off)
-	-	-	0	-	0	RI	Test mode
-	-	1	-	-	0	RI	Test mode

Usage Notes:

1. Driver is designed to be used only as “wrap driver” during I/O AC wrap test. It must be three-stated (Hi-Z) during functional/system mode.
2. Receiver can accommodate a very wide common mode ranging from V_{dd} to 0V. Minimum input swing requires ± 50 mV around the common mode voltage. See “LVDS Receiver DC Specifications” on page 124 for more details.
3. On-chip 100 ohm terminator has approximately $\pm 26\%$ tolerance over process range and temperature range between 0°C and 100°C.

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.480 + 0.001N_{std}$	$0.289 + 0.001N_{std}$	$0.182 + 0.001N_{std}$
		t_{PHL}	$0.489 + 0.001N_{std}$	$0.298 + 0.001N_{std}$	$0.188 + 0.001N_{std}$
	B	t_{PLH}	$0.439 + 0.001N_{std}$	$0.258 + 0.001N_{std}$	$0.158 + 0.001N_{std}$
		t_{PHL}	$0.465 + 0.001N_{std}$	$0.279 + 0.001N_{std}$	$0.174 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	17.513	18.557
DI	8.357	4.995
LT	6.957	5.479
PAD (Receiver Input)	211.292	219.708
PADN (Receiver Input)	216.542	226.333
RG	4.771	4.585
RI	7.647	7.622
TS	7.628	4.167
Internal	138.349	194.442
Cell Units	2 cells	2 cells

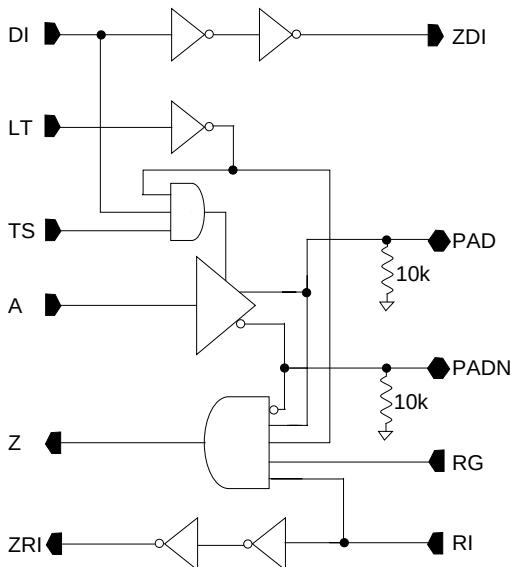
Cell: ILVDSAO, ILVDSAO_PM

Function: 1.8V Nontest LVDS Wide Common Mode Receiver

Description:

Noninverting differential receiver that interfaces between off-chip unidirectional LVDS data buses and 1.8V internal logic. An off-chip differential terminator of 100 ohms between PAD and PADN inputs is recommended. Receiver has wide input common mode ranging from 0V to V_{dd} supply. A differential driver is provided for AC wrap test. The driver must be disabled during system mode. An anti-oscillation feature powers down the receiver when PAD and PADN are disconnected (driver in Hi-Z state). Common mode voltages below 500 mV should not be used since they can activate the anti-oscillation circuit.

A	Wrap driver input
TS	Driver three-state control
DI	Driver inhibit in (DI1 in)
RI	Receiver inhibit in (RI in)
RG	Receiver gate control
LT	DC current gate (I_{dd} test) input
PAD	In-phase receiver in
PADN	Out-phase receiver in
Z	Receiver out
ZRI	Receiver inhibit out (RI out)
ZDI	Driver inhibit out (DI1 out)



Wrap Driver Truth Table

Inputs			Outputs			Comments
A	TS	DI	PAD	PADN	ZDI	
-	0	-	L	L	DI	Functional/test mode
-	-	0	L	L	DI	Test mode
-	1	1	A	$\bar{A}$	DI	Test mode

Receiver Truth Table

Inputs					Outputs		Comments
PAD	PADN	LT	RI	RG	Z	ZRI	
0	1	0	1	1	0	RI	Functional mode
1	0	0	1	1	1	RI	Functional mode
1	1	0	1	1	X	RI	Functional mode
0	0	0	1	1	X	RI	Functional mode
L	L	-	-	-	0	RI	Disconnected receiver (receiver power off)
-	-	-	-	0	0	RI	Functional mode/test mode (receiver power off)
-	-	-	0	-	0	RI	Test mode
-	-	1	-	-	0	RI	Test mode

Usage Notes:

1. Driver is designed to be used only as “wrap driver” during I/O AC wrap test. It must be in Hi-Z during functional/system mode.
2. Receiver can accommodate a very wide common mode ranging from V_{dd} to 0V. Minimum input swing requires ± 50 mV around the common mode voltage. See “LVDS Specifications” on page 124 for more details.
3. In the receiver truth table, “0” and “1” refer to the logic levels of the driver. Level “L” is defined by a 10 kohm pull-down resistor when the driver is in Hi-Z state.

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.478 + 0.001N_{std}$	$0.287 + 0.001N_{std}$	$0.180 + 0.001N_{std}$
		t_{PHL}	$0.487 + 0.001N_{std}$	$0.297 + 0.001N_{std}$	$0.187 + 0.001N_{std}$



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	17.512
DI	8.491
LT	6.956
PAD (Receiver Input)	201.000
PADN (Receiver Input)	208.500
RG	4.754
RI	7.626
TS	7.597
Internal	138.669
Cell Units	2 cells

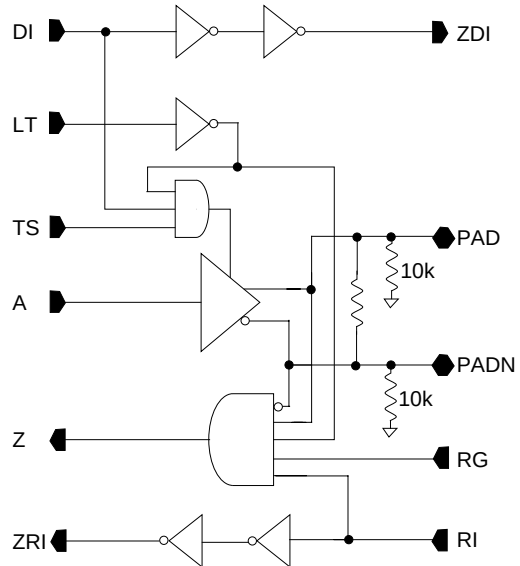
Cell: ILVDSDAO, ILVDSDAO_PM

Function: 1.8V Nontest LVDS Wide Common Mode Receiver with Terminator

Description:

Noninverting differential receiver that interfaces between off-chip unidirectional LVDS data buses and 1.8V internal logic. An on-chip differential terminator of 100 ohm between PAD and PADN inputs is provided. Receiver has wide input common mode ranging from 0V to V_{dd} supply. A differential driver is provided for AC wrap test. Driver must be disabled during system mode. An anti-oscillation feature powers down the receiver when PAD and PADN are disconnected (driver in Hi-Z state). Common mode voltages below 500 mV should not be used, as they can activate the anti-oscillation circuit.

A	Wrap driver input
TS	Driver three-state control
DI	Driver inhibit in (DI1 in)
RI	Receiver inhibit in (RI in)
RG	Receiver gate control
LT	DC current gate (I_{dd} test) input
PAD	In-phase receiver in
PADN	Out-phase receiver in
Z	Receiver out
ZRI	Receiver inhibit out (RI out)
ZDI	Driver inhibit out (DI1 out)



Wrap Driver Truth Table

Inputs			Outputs			Comments
A	TS	DI	PAD	PADN	ZDI	
-	0	-	L	L	DI	Functional/test mode
-	-	0	L	L	DI	Test mode
-	1	1	A	$\bar{A}$	DI	Test mode



Receiver Truth Table

Inputs					Outputs		Comments
PAD	PADN	LT	RI	RG	Z	ZRI	
0	1	0	1	1	0	RI	Functional mode
1	0	0	1	1	1	RI	Functional mode
1	1	0	1	1	X	RI	Functional mode
0	0	0	1	1	X	RI	Functional mode
L	L	-	-	-	0	RI	Disconnected receiver (receiver power off)
-	-	-	-	0	0	RI	Functional mode/test mode (receiver power off)
-	-	-	0	-	0	RI	Test mode
-	-	1	-	-	0	RI	Test mode

Usage Notes:

1. Driver is designed to be used only as “wrap driver” during I/O AC wrap test. It must in Hi-Z during functional/system mode.
2. Receiver can accommodate a very wide common mode ranging from V_{dd} to 0V. Minimum input swing requires ± 50 mV around the common mode voltage. See “LVDS Specifications” on page 124 for more details.
3. On-chip 100 ohm terminator has approximately $\pm 26\%$ tolerance over process range and temperature range between 0°C and 100°C.
4. In the receiver truth table, “0” and “1” refer to the logic levels of the driver. Level “L” is defined by a 10 kohm pulldown resistor when the driver is in Hi-Z state.

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.480 + 0.001N_{std}$	$0.289 + 0.001N_{std}$	$0.182 + 0.001N_{std}$
		t_{PHL}	$0.489 + 0.001N_{std}$	$0.298 + 0.001N_{std}$	$0.188 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	17.513
DI	8.357
LT	6.957
PAD (Receiver Input)	211.292
PADN (Receiver Input)	216.542
RG	4.771
RI	7.647
TS	7.628
Internal	138.349
Cell Units	2 cells

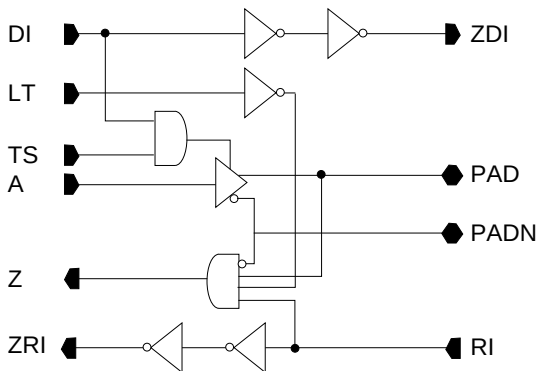
Cell: IPECL, IPECL_PM

Function: 1.8V/2.5V PECL Nontest Differential Receiver

Description:

Noninverting differential receiver used to receive complementary ECL signals referenced to V_{dd250} (2.5V nominal) supply. All pins exclusive of PAD and PADN are referenced to the V_{dd} supply (1.8V nominal). A differential termination of 100 ohms between PAD and PADN inputs is recommended.

- A Driver data input
- TS Driver three-state control
- DI Driver input (DI1 in)
- RI Receiver input (RI in)
- LT DC current gate (I_{dd} test) input
- PAD In-phase driver in
- PADN Out-phase driver in
- Z Receiver out
- ZRI Receiver inhibit (RI out)
- ZDI Driver inhibit out (DI1 out)



Wrap Driver Truth Table

Inputs			Outputs		
A	TS	DI	PAD	PADN	ZDI
-	0	-	Hi-Z	Hi-Z	DI
-	-	0	Hi-Z	Hi-Z	DI
-	1	1	A	$\bar{A}$	DI

Receiver Truth Table

Inputs				Outputs		Comments
PAD	PADN	LT	RI	Z	ZRI	
0	1	0	1	0	RI	Function mode
1	0	0	1	1	RI	Function mode
1	1	0	1	X	RI	Function mode
0	0	0	1	X	RI	Function mode
-	-	0	0	0	RI	Test mode
-	-	1	-	0	RI	Leakage test

Usage Notes:

1. The wrap driver in this cell is only used during wrap test with CMOS output levels and is not intended for functional use.
2. During I_{ddq} test LT = 1 and the receiver is disabled.

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^{\circ}C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.489 + 0.001N_{std}$	$0.324 + 0.001N_{std}$	$0.227 + 0.001N_{std}$
		t_{PHL}	$0.532 + 0.001N_{std}$	$0.354 + 0.000N_{std}$	$0.249 + 0.000N_{std}$



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	17.926
DI	5.666
LT	2.585
PAD (Receiver Input)	227.208
PADN (Receiver Input)	229.500
RI	9.483
TS	3.470
Internal	225.000
Cell Units	2 cells

Refer to "PECL Receiver Specifications" on page 134 for more information.

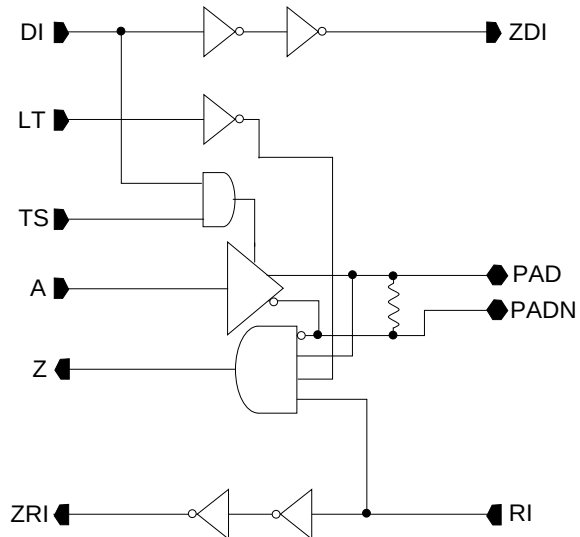
Cell: IPECLD, IPECLD_PM

Function: 1.8V/2.5V PECL Nontest Differential Receiver w/Termination

Description:

Noninverting differential receiver used to receive complementary ECL signals referenced to V_{dd250} (2.5V nominal) supply. All pins exclusive of PAD and PADN are referenced to the V_{dd} supply (1.8V nominal). A differential termination of 100 ohms is inserted between PAD and PADN.

- A Driver data input
- TS Driver three-state control
- DI Driver input (DI1 in)
- RI Receiver input (RI in)
- LT DC current gate (I_{dd} test) input
- PAD In-phase driver in
- PADN Out-phase driver in
- Z Receiver out
- ZRI Receiver inhibit (RI out)
- ZDI Driver inhibit out (DI1 out)



Wrap Driver Truth Table

Inputs			Outputs		
A	TS	DI	PAD	PADN	ZDI
-	0	-	Hi-Z	Hi-Z	DI
-	-	0	Hi-Z	Hi-Z	DI
-	1	1	A	$\bar{A}$	DI



Receiver Truth Table

Inputs				Outputs		Comments
PAD	PADN	LT	RI	Z	ZRI	
0	1	0	1	0	RI	Function mode
1	0	0	1	1	RI	Function mode
1	1	0	1	X	RI	Function mode
0	0	0	1	X	RI	Function mode
-	-	0	0	0	RI	Test mode
-	-	1	-	0	RI	Leakage test

Usage Notes:

- 1.The wrap driver in this cell is only used during wrap-test with CMOS output levels and is not intended for functional use.
- 2.During I_{ddq} test LT = 1 and the receiver is disabled.

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^{\circ}C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.489 + 0.001N_{std}$	$0.324 + 0.001N_{std}$	$0.227 + 0.001N_{std}$
		t_{PHL}	$0.532 + 0.001N_{std}$	$0.354 + 0.000N_{std}$	$0.249 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	17.917
DI	5.666
LT	2.585
PAD (Receiver Input)	249.875
PADN (Receiver Input)	252.458
RI	9.483
TS	3.469
Internal	205.432
Cell Units	2 cells

Refer to "PECL Receiver Specifications" on page 134 for more information.

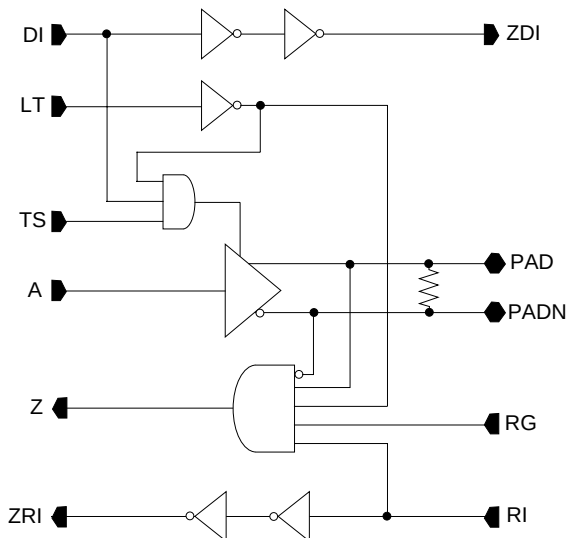
Cell: ISTI18D, ISTI18D_PM

Function: 1.8V STI Nontest Terminated Differential Receiver

Description:

Noninverting terminated differential receiver that can be used to receive complementary signals. STI is a very high-speed asynchronous communications protocol used to connect devices that may be 1 to 15 meters apart. A differential termination of 100 ohms is between PAD and PADN inputs.

- A Driver data input
- TS Driver three-state control
- DI Driver input (DI1 in)
- RI Receiver input (RI in)
- RG Receiver gate control
- LT DC current gate (I_{dd} test) input
- PAD In-phase receiver in
- PADN Out-phase receiver in
- Z Receiver out
- ZRI Receiver inhibit (RI out)
- ZDI Driver inhibit out (DI1 out)



Wrap Driver Truth Table

Inputs				Outputs			Comments
A	TS	DI	LT	PAD	PADN	ZDI	
-	0	-	-	Hi-Z	Hi-Z	DI	Functional mode
-	-	0	-	Hi-Z	Hi-Z	DI	Test mode
-	-	-	1	Hi-Z	Hi-Z	DI	Leakage test
-	1	1	0	A	$\bar{A}$	DI	Functional mode

Receiver Truth Table

Inputs					Outputs		Comments
PAD	PADN	LT	RI	RG	Z	ZRI	
0	1	0	1	1	0	RI	Functional mode
1	0	0	1	1	1	RI	Functional mode
1	1	0	1	1	X	RI	Functional mode
0	0	0	1	1	X	RI	Functional mode
-	-	-	-	0	0	RI	Functional mode (rec power off)
-	-	-	0	-	0	RI	Test mode
-	-	1	-	-	0	RI	Test mode (leakage current test)

Usage Notes:

1. The wrap driver in this circuit is only used during wrap test and does not require a terminator.
2. Normal receiver operation requires a differential input signal of ± 500 mV around a common mode input signal of 1.1V.

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.598 + 0.002N _{std}	0.374 + 0.002N _{std}	0.253 + 0.001N _{std}
		t _{PHL}	0.671 + 0.002N _{std}	0.409 + 0.001N _{std}	0.262 + 0.001N _{std}
PADN-Z		t _{PLH}	0.598 + 0.002N _{std}	0.374 + 0.002N _{std}	0.253 + 0.001N _{std}
		t _{PHL}	0.671 + 0.002N _{std}	0.409 + 0.001N _{std}	0.262 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	7.580
DI	3.176
LT	1.768
PAD (Receiver Input)	205.000
PADN (Receiver Input)	205.000
RG	2.643
RI	3.195
TS	1.920
Internal	850.000
Cell Units	2 cells

For more information, see "Other Driver and Receiver Specifications" on page 118.

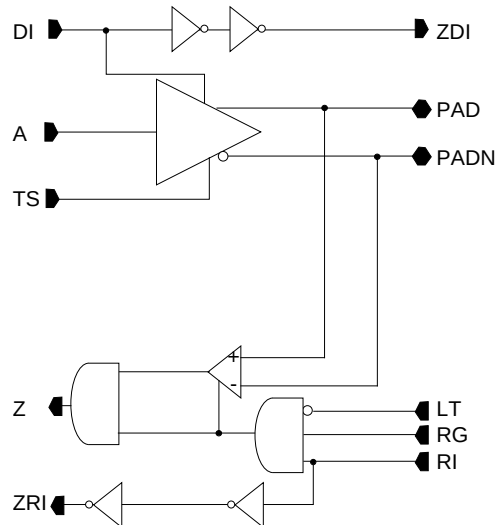
Cell: OHSTL, OHSTL_PM

Function: HSTL 1.5V Class 2 Differential Driver

Description:

Noninverting differential driver that interfaces 1.8 V internal functions with differential 1.5V HSTL receivers. Multiple far end termination options are possible, but 100 ohms differential termination is preferred. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} . A "wrap-receiver" is provided for test and can be disabled with the RG pin during system mode. Driver requires the use of a second power supply, V_{dd150} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RI Receiver inhibit input (RI in)
- RG Receiver gate control
- LT DC current gate (I_{dd} test) input
- PAD Driver/receiver in-phase output/input
- PADN Driver/receiver out-of-phase output/in-put
- Z Receiver output
- ZDI Driver inhibit output (DI out)
- ZRI Receiver inhibit output (RI out)



Driver Truth Table

Inputs			Outputs		
A	TS	DI	PAD	PADN	ZDI
-	-	0	Hi-Z	Hi-Z	DI
-	0	-	Hi-Z	Hi-Z	DI
-	1	1	A	A	DI



Wrap Receiver Truth Table

Inputs					Outputs	
PAD	PADN	LT	RI	RG	Z	ZRI
-	-	-	0	-	0	RI
-	-	-	-	0	0	RI
0	1	0	1	1	0	RI
1	0	0	1	1	1	RI
0	0	0	1	1	X	RI
1	1	0	1	1	X	RI
-	-	1	-	-	0	RI

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd150} = 1.4V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd150} = 1.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd150} = 1.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$0.583 + 0.016D_{std}$	$0.392 + 0.013D_{std}$	$0.285 + 0.010D_{std}$
		t_{PHL}	$0.615 + 0.017D_{std}$	$0.423 + 0.012D_{std}$	$0.311 + 0.010D_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	11.564
DI	3.772
LT	3.282
PAD (Receiver Input)	361.375
PADN (Receiver Input)	363.333
RG	7.072
RI	6.401
TS	3.070
Internal	390.00
Cell Units	2 cells

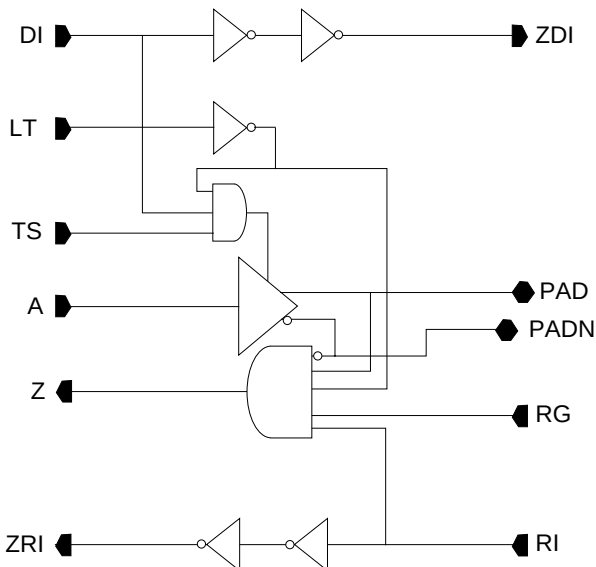
Cell: OLVDS, OLVDS_PM

Function: Low-Voltage Differential Swing Driver (Nontest)

Description:

Noninverting differential high-speed buffer (driver) interfacing off-chip unidirectional LVDS data buses with 1.8V internal logic. This design requires both 1.8V and 2.5V supplies. To achieve an LVDS signal, a 100 ohm terminator between the differential inputs of the far-end receiver is required. A "wrap-receiver" is provided for test and can be disabled with the RG pin during system mode.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit in (DI1 in)
- RI Wrap receiver inhibit in (RI in)
- RG Wrap receiver gate control
- LT DC current gate (I_{dd} test) input
- PAD In-phase driver out
- PADN Out-of-phase driver out
- Z Wrap receiver out
- ZRI Wrap receiver inhibit out (RI out)
- ZDI Driver inhibit out (DI1 out)



Driver Truth Table

Inputs				Outputs			Comments
A	TS	DI	LT	PAD	PADN	ZDI	
-	0	-	-	Hi-Z	Hi-Z	DI	Functional/test mode
-	-	0	-	Hi-Z	Hi-Z	DI	Test mode
-	-	-	1	Hi-Z	Hi-Z	DI	Test mode
-	1	1	0	A	$\bar{A}$	DI	Functional mode

Receiver Truth Table

Inputs					Outputs		Comments
PAD	PADN	LT	RI	RG	Z	ZRI	
0	1	0	1	1	0	RI	Functional mode
1	0	0	1	1	1	RI	Functional mode
1	1	0	1	1	X	RI	Functional mode
0	0	0	1	1	X	RI	Functional mode
-	-	-	-	0	0	RI	Functional mode/test mode (rec power off)
-	-	-	0	-	0	RI	Test mode
-	-	1	-	-	0	RI	Test mode

Usage Notes:

1. In functional/system mode, the wrap receiver can be disabled by the RG pin as an option to save power. The wrap receiver is designed to be used for wrap test only. It cannot be used as a functional receiver.
2. LVDS buffer offers two performance levels. Performance level A supports up to 622 MHz; performance level B supports up to 1.25 GHz (at 100°C and worst-case process) in an ideal environment. Detailed waveform integrity analysis is required to determine optimal performance on a specific net.
3. Although the buffer design supports functionality up to 125°C, metal reliability (electromigration) degrades rapidly over 100°C. Consult your IBM application engineer for more details regarding operation at temperatures above 100°C.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	0.654 + 0.026D _{std}	0.445 + 0.023D _{std}	0.323 + 0.021D _{std}
		t _{PHL}	0.642 + 0.026D _{std}	0.438 + 0.023D _{std}	0.322 + 0.022D _{std}
	B	t _{PLH}	0.542 + 0.003D _{std}	0.319 + 0.012D _{std}	0.275 + 0.012D _{std}
		t _{PHL}	0.548 + 0.003D _{std}	0.325 + 0.012D _{std}	0.279 + 0.012D _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	6.487	25.963
DI	5.685	5.588
LT	5.542	6.035
PAD (Receiver Input)	341.167	341.167
PADN (Receiver Input)	314.542	314.542
RG	3.440	3.262
RI	5.170	5.193
TS	3.805	3.702
Internal	266.000	272.000
Cell Units	2 cells	2 cells

Refer to Table 66, "LVDS Driver DC Specifications: OLVDS_A," on page 125 and Table 67, "LVDS Driver DC Specifications: OLVDS_B," on page 126 for more information

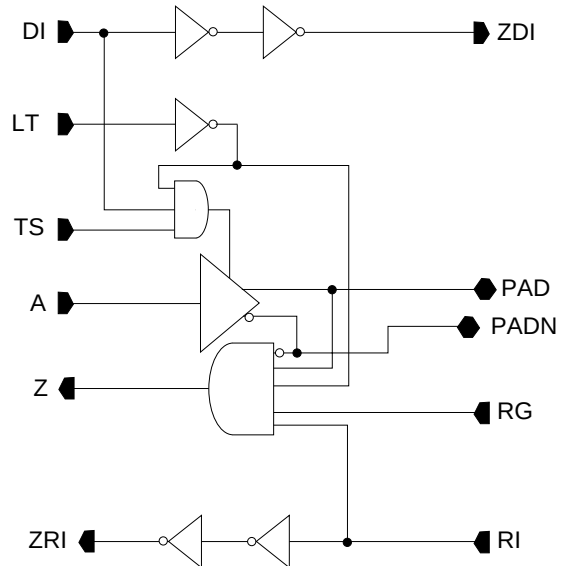
Cell: OLVDS18, OLVDS18_PM

Function: Low-Voltage Differential Swing Driver (Nontest)

Description:

Noninverting differential high speed buffer (driver) interfacing off-chip unidirectional LVDS data buses and 1.8V internal logic. This design requires only the 1.8V core supply voltage. To achieve LVDS signal, a 100 ohm terminator between the differential inputs of the far-end receiver is required. A "wrap-receiver" is provided for test and it can be disabled with RG pin during system mode.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit in (DI1 in)
- RI Wrap receiver inhibit in (RI in)
- RG Wrap receiver gate control
- LT DC current gate (I_{dd} test) input
- PAD In-phase driver out
- PADN Out-of-phase driver out
- Z Wrap receiver out
- ZRI Wrap receiver inhibit out (RI out)
- ZDI Driver inhibit out (DI1 out)



Driver Truth Table

Inputs				Outputs			Comments
A	TS	DI	LT	PAD	PADN	ZDI	
-	0	-	-	Hi-Z	Hi-Z	DI	Functional/test mode
-	-	0	-	Hi-Z	Hi-Z	DI	Test mode
-	-	-	1	Hi-Z	Hi-Z	DI	Test mode
-	1	1	0	A	$\bar{A}$	DI	Functional mode



Receiver Truth Table

Inputs					Outputs		Comments
PAD	PADN	LT	RI	RG	Z	ZRI	
0	1	0	1	1	0	RI	Functional mode
1	0	0	1	1	1	RI	Functional mode
1	1	0	1	1	X	RI	Functional mode
0	0	0	1	1	X	RI	Functional mode
-	-	-	-	0	0	RI	Functional mode/test mode (receiver power off)
-	-	-	0	-	0	RI	Test mode
-	-	1	-	-	0	RI	Test mode

Usage Notes:

1. In functional/system mode, the wrap receiver can be disabled by the RG pin as an option to save power. The wrap receiver is designed to be used for wrap test only. It cannot be used as a functional receiver.
2. Normal driver operation requires a differential terminator of 100 ohms at the differential input of a “far-end” receiver. The normal driver output swing is 400 mV peak-to-peak (DC) with a common mode voltage of 1.20V.
3. The OLVDS18 and OLVDS18_PM buffers are designed to support 1.250 Gbps data rates (625 MHz clock rate). Detailed analysis is required to determine actual system performance.
4. Although buffer design supports functionality up to 125°C, metal reliability (electromigration) degrades rapidly over 100°C. Consult an IBM application engineer for more details regarding operation at temperature above 100°C.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$0.810 + 0.024D_{std}$	$0.529 + 0.023D_{std}$	$0.384 + 0.022D_{std}$
		t_{PHL}	$0.807 + 0.024D_{std}$	$0.533 + 0.023D_{std}$	$0.388 + 0.022D_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	10.917
DI	5.366
LT	2.977
PAD (Receiver Input)	390.125
PADN (Receiver Input)	390.167
RG	3.574
RI	5.489
TS	3.950
Internal	358.188
Cell Units	2 cells

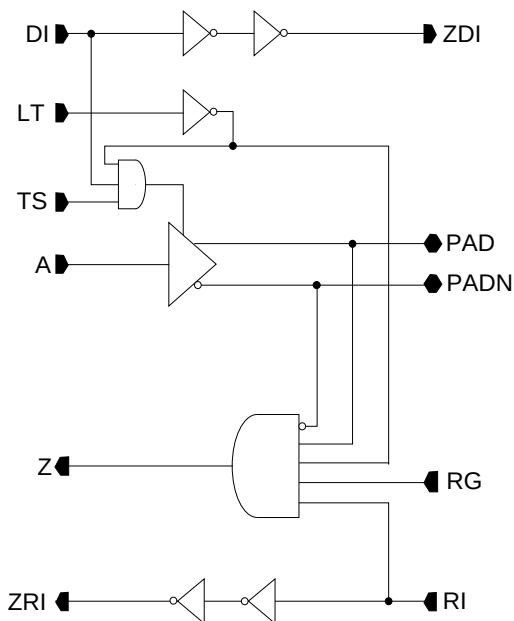
Cell: OPLVDS, OPLVDS_PM

Function: Pseudo Low-Voltage Differential Swing Driver (Nontest)

Description:

Noninverting differential high-speed driver which interface off-chip unidirectional LVDS data buses with 1.8V internal logic. The operation of the pseudo LVDS driver is similar to the standard IEEE LVDS driver except for a much wider output voltage swing. The pseudo LVDS driver is compatible with LVDS receivers. It requires a single 1.8V power supply. A 100 ohm terminator between the differential inputs of the far-end receiver is also required. A "wrap-receiver" is provided for test and can be disabled in the functional mode via the RG pin.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit in (DI1 in)
- RI Wrap receiver inhibit in (RI in)
- RG Wrap receiver gate control
- LT DC current gate (I_{dd} test) input
- PAD In-phase driver out
- PADN Out-of-phase driver out
- Z Wrap receiver out
- ZRI Wrap receiver inhibit out (RI out)
- ZDI Driver inhibit out (DI1 out)



Driver Truth Table

Inputs				Outputs			Comments
A	TS	DI	LT	PAD	PADN	ZDI	
-	0	-	-	Hi-Z	Hi-Z	DI	Functional/test mode
-	-	0	-	Hi-Z	Hi-Z	DI	Test mode
-	-	-	1	Hi-Z	Hi-Z	DI	Test mode
-	1	1	0	A	$\bar{A}$	DI	Functional mode

Receiver Truth Table

Inputs					Outputs		Comments
PAD	PADN	LT	RI	RG	Z	ZRI	
0	1	0	1	1	0	RI	Functional mode
1	0	0	1	1	1	RI	Functional mode
1	1	0	1	1	X	RI	Functional mode
0	0	0	1	1	X	RI	Functional mode
-	-	-	-	0	0	RI	Functional mode/test mode (receiver power off)
-	-	-	0	-	0	RI	Test mode
-	-	1	-	-	0	RI	Test mode

Usage Notes:

1. Normal driver operation requires a 100 ohm termination at the far end of the net (receiver input).
2. The pseudo LVDS driver does not comply with standard IEEE LVDS DC levels and output impedance. However, its larger signal swing provides improved performance at high frequencies and over a longer distances between chips while dissipating lower power than a conventional LVDS driver.
3. Under ideal conditions, the pseudo LVDS driver supports operation at up to 1.5 GHz at 125°C and worst-case process. Detailed waveform integrity analysis is required to determine the optimal performance on a specific net.
4. Although the driver design supports functionality up to 125°C, metal reliability (electromigration) degrades rapidly over 100°C. Consult an IBM application engineer for more details regarding operation at temperatures above 100°C.
5. In the functional mode, the wrap receiver can be disabled by the RG pin as an option to save power. The wrap receiver is designed to be used for wrap test only. It cannot be used as a functional receiver.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	0.522 + 0.013D _{std}	0.343 + 0.010D _{std}	0.248 + 0.008D _{std}
		t _{PHL}	0.513 + 0.013D _{std}	0.341 + 0.010D _{std}	0.245 + 0.008D _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	11.957
DI	3.161
LT	1.612
PAD (Receiver Input)	295.625
PADN (Receiver Input)	264.500
RG	2.876
RI	3.701
TS	5.845
Internal	483.00
Cell Units	2 cells

Refer to Table 68, “LVDS Driver DC Specifications: OPLVDS_A,” on page 127 for more information.

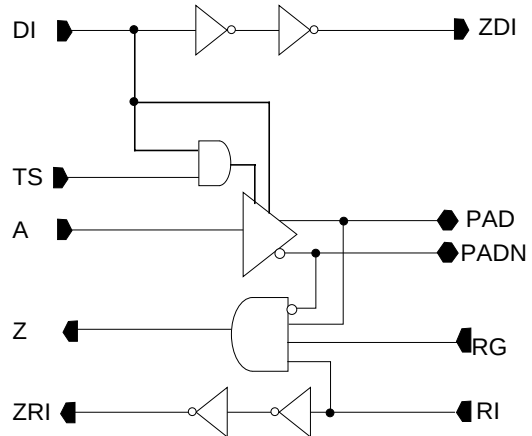
Cell: OPECL

Function: 1.8V/3.3V PECL Non-Test Differential Driver

Description:

Noninverting, fully differential dual power supply driver used to drive complementary pseudo ECL signals referenced to V_{dd330} (3.3V nominal) supply. All inputs are 1.8V (nominal) CMOS. A differential termination of 100 ohms between PAD and PADN inputs at the far end of the receiver is recommended.

- A Driver data input
- TS Driver three state control
- DI Driver input (DI1 in/ I_{ddq} test)
- RI Receiver input (RI in/ I_{ddq} test)
- RG Receiver gate control
- PAD In-phase driver out
- PADN Out-phase driver out
- Z Receiver out
- ZRI Receiver inhibit (RI out)
- ZDI Driver inhibit out (DI1 out)



Driver Truth Table

Inputs			Outputs			Comments
A	TS	DI	PAD	PADN	ZDI	
-	0	-	Hi-Z	Hi-Z	DI	Function mode
-	-	0	Hi-Z	Hi-Z	DI	Leakage test
-	1	1	A	$\bar{A}$	DI	Function mode

Wrap Receiver Truth Table

Inputs				Outputs		Comments
PAD	PADN	RG	RI	Z	ZRI	
0	1	1	1	0	RI	Function mode
1	0	1	1	1	RI	Function mode
1	1	1	1	X	RI	Function mode
0	0	1	1	X	RI	Function mode
-	-	-	0	0	RI	Leakage test
-	-	0	-	0	RI	Disable receiver

Usage Notes:

1. Normal driver operation requires a termination at the far end of the net at input to the receiver.
2. Termination must be one of the following:
 - A split 100 ohm differential termination of 50 ohms from the (+) input and 50 ohms from the (-) input to the center tap with a 100 pF to GND (for short nets)
 - A 100 ohm differential terminator between (+) and (-) receiver inputs (for cable nets > 10 meters)
 - A 50 ohm Thevenin equivalent circuit between 3.3V (V_{dd330}) and GND with a common mode voltage of 2.0V
3. The wrap receiver in this cell is only used during wrap test.
4. Inputs to the receiver must be complementary during functional mode; otherwise the output will be indeterminate.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.132 + 0.020D_{std}$	$0.720 + 0.015D_{std}$	$0.514 + 0.013D_{std}$
		t_{PHL}	$1.053 + 0.020D_{std}$	$0.682 + 0.015D_{std}$	$0.488 + 0.013D_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	15.590
DI	8.621
PAD (Receiver Input)	384.750
PADN (Receiver Input)	387.792
RG	5.464
RI	8.534
TS	3.719
Internal	636.561
Cell Units	2 cells

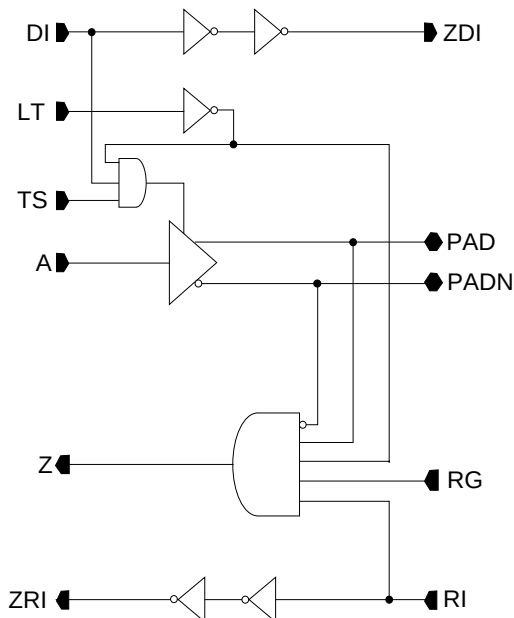
Cell: OSTI18, OSTI18_PM

Function: 1.8V STI Nontest Differential Driver

Description:

Noninverting, fully differential driver used to drive complementary signals into a differential far end receiver. STI is a very high-speed asynchronous communications protocol used to connect devices that can be 1 to 15 meters apart. A termination of 100 ohms between PAD and PADN inputs of the far-end receiver is always recommended.

A	Driver data input
TS	Driver three-state control
DI	Driver input (DI1 in)
RI	Receiver input (RI in)
RG	Receiver gate control
LT	DC current gate (I_{dd} test) input
PAD	In-phase driver out
PADN	Out-phase driver out
Z	Receiver out
ZRI	Receiver inhibit (RI out)
ZDI	Driver inhibit out (DI1 out)



Driver Truth Table

Inputs				Outputs			Comments
A	TS	DI	LT	PAD	PADN	ZDI	
-	0	-	-	Hi-Z	Hi-Z	DI	Functional mode
-	-	0	-	Hi-Z	Hi-Z	DI	Test mode
-	-	-	1	Hi-Z	Hi-Z	DI	Leakage test
-	1	1	0	A	$\bar{A}$	DI	Functional mode

Wrap Receiver Truth Table

Inputs					Outputs		Comments
PAD	PADN	LT	RG	RI	Z	ZRI	
0	1	0	1	1	0	RI	Functional mode
1	0	0	1	1	1	RI	Functional mode
0	0	0	1	1	X	RI	Functional mode
1	1	0	1	1	X	RI	Functional mode
-	-	0	1	0	0	RI	Test mode
-	-	0	0	1	0	RI	Functional mode
-	-	1	-	-	0	RI	Leakage test

Usage Notes:

1. Normal driver operation requires a termination at the far end of the net at input to the receiver.
2. Termination must be one of the following:
 - A split 100 ohm differential termination of 50 ohms from the + input and 50 ohms from the - input to the center tap with a 100 pF to GND (for short nets).
 - A 100 ohm differential terminator between + and - receiver inputs (for cable nets >10 meters).
 - A 50 ohm Thevenin equivalent circuit between V_{dd} and GND with a common mode voltage of 0.9V.
3. The wrap receiver in this circuit is only used during wrap test.
4. If the input to the receiver is in an unknown state (Hi-Z), then the output is indeterminate.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$0.463 + 0.019D_{std}$	$0.313 + 0.014D_{std}$	$0.228 + 0.011D_{std}$
		t_{PHL}	$0.449 + 0.019D_{std}$	$0.307 + 0.014D_{std}$	$0.225 + 0.012D_{std}$



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	8.460
DI	4.491
LT	1.933
PAD (Receiver Input)	364.125
PADN (Receiver Input)	365.292
RG	1.631
RI	4.025
TS	2.256
Internal	148.684
Cell Units	2 cells

For more information, see "Other Driver and Receiver Specifications" on page 118.

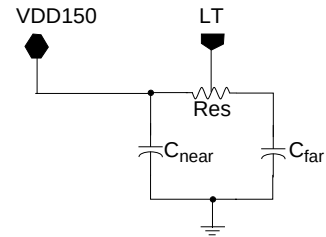
Cell: VDD150DECAP, VDD150DECAP_PM
Function: V_{dd150} - GND Decoupling Capacitor

Description:

The VDD150DECAP cell is a MOS capacitor that can be placed on a chip to provide local noise decoupling from V_{dd150} to GND. It requires an entire I/O cell and should be placed near switching I/Os. The LT pin is used at test to eliminate potential leakage current. The slew of the LT pin is non-critical. The VDD150DECAP cell is modeled as a pi network (see diagram and table below), where C_{near} is defined as the capacitance closest to the switching event.

VDD150DECAP_A use is restricted to area array images. VDD150DECAP_PM_A is used on peripheral C4 images, while the _PM_B version is used on staggered wire bond images. None of these three cells can be used on inline wire bond images.

LT Leakage test input pin



Truth Table

Input	Mode
LT	
0	Decoupling - normal mode
1	Leakage test - decoupling off

Capacitance, Resistance and Cell Sizes

Input Pins	Performance Level	
	A	B (_PM only)
LT (pF)	0.052	0.052
C _{near} (pF)	9.2	5.2
Resistance (ohms)	0.8	3.0
C _{far} (pF)	59.1	43.6
Cell Units	1 I/O cell	1 I/O cell

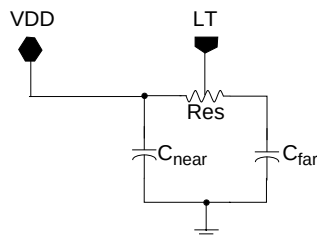
Cell: VDD180DECAP, VDD180DECAP_PM
Function: V_{dd} - GND Decoupling Capacitor

Description:

The VDD180DECAP cell is a MOS capacitor that can be placed on a chip to provide local noise decoupling from V_{dd} to GND. It requires an entire I/O cell and should be placed near switching I/Os. The LT pin is used at test to eliminate potential leakage current. The slew of the LT pin is non-critical. The VDD180DECAP cell is modeled as a pi network (see diagram and table below), where C_{near} is defined as the capacitance closest to the switching event.

VDD180DECAP_A use is restricted to area array images. VDD180DECAP_PM_A is used on peripheral C4 images, while the _PM_B version is used on staggered wire bond images. None of these three cells can be used on inline wire bond images.

LT Leakage test input pin



Truth Table

Input	Mode
LT	
0	Decoupling - normal mode
1	Leakage Test - decoupling off

Capacitance, Resistance and Cell Sizes

Input Pins	Performance Level	
	A	B (_PM Only)
LT (pF)	0.052	0.052
C _{near} (pF)	7.2	4.2
Resistance (ohms)	1.3	1.9
C _{far} (pF)	63.2	45.9
Cell Units	1 I/O cell	1 I/O cell

Cell: VDD250DECAP, VDD250DECAP_PM

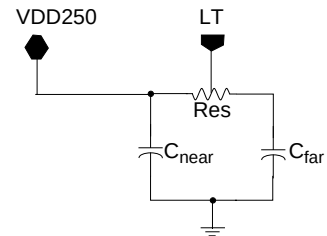
Function: V_{dd250} - GND Decoupling Capacitor

Description:

The VDD250DECAP cell is a MOS capacitor that can be placed on a chip to provide local noise decoupling from V_{dd250} to GND. It requires an entire I/O cell and should be placed near switching I/Os. The LT pin is used at test to eliminate potential leakage current. The slew of the LT pin is non-critical. The VDD250DECAP cell is modeled as a pi network (see diagram and table below), where C_{near} is defined as the capacitance closest to the switching event.

VDD250DECAP_A use is restricted to area array images. VDD250DECAP_PM_A is used on peripheral C4 images, while the _PM_B version is used on staggered wire bond images. None of these three cells can be used on inline wire bond images.

LT Leakage test input pin



Truth Table

Input	Mode
LT	
0	Decoupling - normal mode
1	Leakage test - decoupling off

Capacitance, Resistance and Cell Sizes

Input Pins	Performance Level	
	A	B (_PM only)
LT (pF)	0.052	0.052
C _{near} (pF)	4.70	3.1
Resistance (ohms)	2.7	3.8
C _{far} (pF)	37.9	26.4
Cell Units	1 I/O cell	1 I/O cell

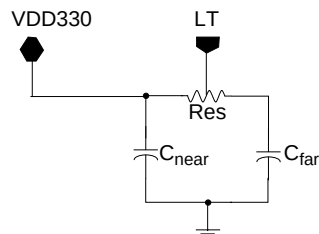
Cell: VDD330DECAP, VDD330DECAP_PM
Function: V_{dd330} - GND Decoupling Capacitor

Description:

The VDD330DECAP cell is a MOS capacitor that can be placed on a chip to provide local noise decoupling from V_{dd330} to GND. It requires an entire I/O cell and should be placed near switching I/Os. The LT pin is used at test to eliminate potential leakage current. The slew of the LT pin is non-critical. The VDD330DECAP cell is modeled as a pi network (see diagram and table below), where C_{near} is defined as the capacitance closest to the switching event.

VDD330DECAP_A use is restricted to area array images. VDD330DECAP_PM_A is used on peripheral C4 images, while the _PM_B version is used on staggered wire bond images. None of these three cells are usable on inline wire bond images.

LT Leakage test input pin



Truth Table

Input	Mode
LT	
0	Decoupling - normal mode
1	Leakage test - decoupling off

Capacitance, Resistance and Cell Sizes

Input Pins	Performance Level	
	A	B (_PM only)
LT (pF)	0.052	0.052
C _{near} (pF)	4.7	3.1
Resistance (ohms)	2.8	3.9
C _{far} (pF)	37.7	26.3
Cell Units	1 I/O cell	1 I/O cell

Cell: THERMAL, THERMAL_PM

Function: Thermal Monitor

Description:

The thermal monitor consists of a resistor connected between pins PADA and PADB. At 25°C this resistance is estimated at 1500 ± 350 ohms. The expected temperature coefficient of the resistance for this technology (t_c) is 0.33% per °C. To determine the actual temperature coefficient, see Measurement Calibration below.



Note: There are electrostatic discharge (ESD) diodes at PADA and PADB.

Temperature Calculation:

The chip temperature can be calculated from

$$T_{chip} = \left[\frac{(R_{measured} - R_{calibrated})}{t_c \times R_{calibrated}} + T_{calibrated} \right] ^\circ C$$

where:

$R_{measured}$ = resistance measured between PADA and PADB at test temperature.

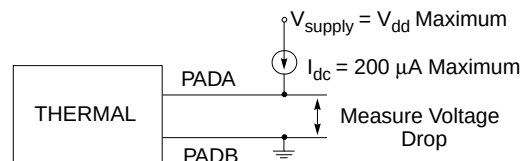
$R_{calibrated}$ = resistance measured between PADA and PADB at known temperature.

$T_{calibrated}$ = known temperature used to measure $R_{calibrated}$.

Measurement Calibration:

In order to use this thermal monitor accurately, the actual temperature coefficient must be calibrated. To do this, measure the voltage drop at two different known temperatures at the package while the chip is dissipating little (less than 100 mW) or no power. Apply I_{dc} and wait for a fixed time " t_m ," where $t_m \approx 1$ ms. Keep t_m short to minimize heating effects on the thermal monitor resistance. Then measure the voltage (V_1) across PADA and PADB at this known temperature (T_1). Next, turn off I_{dc} and raise the package temperature to T_2 . Reapply I_{dc} , wait t_m again and measure the voltage (V_2) across PADA and PADB at the new known temperature (T_2).

The temperature coefficient where: $t_c = \left[\frac{V_2 - V_1}{V_1(T_2 - T_1)} \right] \times 100\% \text{ per } ^\circ C$



Cell: PSRO2PD_A

Function: Performance Screen Ring Oscillator

Description:

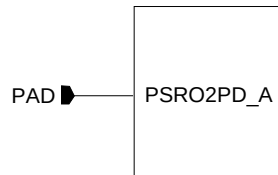
This circuit could be used to screen product based on performance. Circuit performance varies as a function of the manufacturing process. The circuit is comprised of an enable circuit, a ring oscillator, a frequency divider, and an output driver.

When the circuit is activated by applying 1.8V to PAD through a 50 ohm resistance, the signal will swing between approximately 1.8V and 1.1V.

Unless placed in a test I/O location, the circuit will be provided as an untested process monitor circuit.

This is a single cell I/O.

PAD Activate circuit/sense output



Contact IBM ASIC development through your field application engineer for more information.

Cell: PSRO2PU_PM_A

Function: Performance Screen Ring Oscillator

Description:

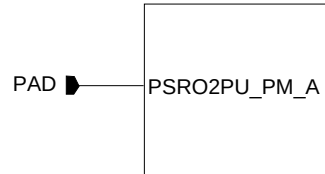
This circuit could be used to screen product based on performance. Circuit performance varies as a function of the manufacturing process. The circuit is comprised of an enable circuit, a ring oscillator, a frequency divider, and an output driver.

When the circuit is activated by applying GND to PAD through a 50 ohm resistance, the signal will swing between approximately 0.7V and GND.

Unless placed in a test I/O location, the circuit will be provided as an untested process monitor circuit.

This is a single cell I/O.

PAD Activate circuit/sense output



Contact IBM ASIC development through your field application engineer for more information.

Standard Cell Test I/O

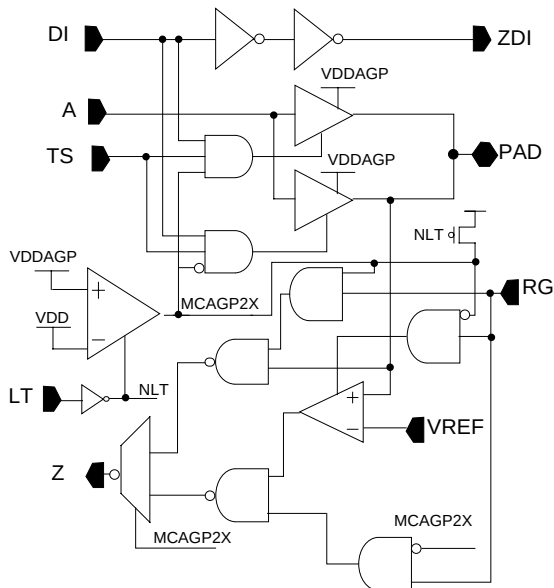
Refer to "DC or Limited-Function Test I/Os" on page 90 for more information on using DC test I/Os.

Cell: BAGP2X4XT, BAGP2X4XT_PM
Function: AGP 2X/4X Dual Mode Test CIO

Description:

Noninverting three-state driver/receiver for 3.3V AGP (accelerated graphics port) 2X operation or 1.5V 4X operation. This I/O requires two power supplies: V_{dd} and VDDAGP. VDDAGP determines the IO's mode of operation. These are bidirectional I/Os. The 4X receiver requires an (off-chip) input reference (0.75V).

A	Driver data input
TS	Driver three-state control
LT	DC current gate (I_{dd} test) input
DI	Driver inhibit input (DI in)
RG	Receiver gate control
PAD	Driver output/receiver input
VREF	Voltage reference input
Z	Receiver output
ZDI	Driver inhibit output (DI out)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A ¹	DI

1. If $VDDAGP = 1.5V \pm 0.1V$, the driver operates in AGP4X mode. Output logical "1" = $VDDAGP = 1.5V$. If $VDDAGP = 3.3V \pm 0.3V$, the driver operates in AGP2X mode. Output logical "1" = $VDDAGP = 3.3V$.
2. During I_{ddq} test, when $LT=1$, the I/O will be forced to 2X operation and VDDAGP must be set to 3.3V.
3. 4X mode will not be fully tested. The customer has the choice of whether or not to use this test I/O.

AGP2X Receiver Truth Table (VDDAGP = 3.3V)

Inputs				Output	Comments
PAD	LT	RG	VREF	Z	
-	0	0	-	0	Functional/test mode (receiver power off)
0 ¹	0	1	-	0	Functional mode
1 ²	0	1	-	1	Functional mode
0 ¹	1 ³	1	-	0	Bypass mode /I _{ddq}
1 ²	1 ³	1	-	1	Bypass mode /I _{ddq}
-	1 ³	0	-	0	I _{ddq} test/burn-in
Hi-Z	-	1	-	X	

1. AGP2X mode input logic "0" is 0V.

2. AGP2X mode input logic "1" is 3.3V ± 0.3V.

3. During I_{ddq} test, when LT = 1, VDDAGP must be set to 3.3V. The 4X receiver will be turned off and the 2X receiver will become the bypass receiver.

AGP4X Receiver Truth Table (VDDAGP = 1.5V)

Inputs				Output	Comments
PAD	LT	RG	VREF	Z	
-	0	0	-	0	Functional/test mode (receiver power off)
0 ¹	0	1	-	0	Functional mode
1 ²	0	1	-	1	Functional mode
0 ³	1 ⁴	1	-	0	Bypass mode /I _{ddq}
1 ⁵	1 ⁴	1	-	1	Bypass mode /I _{ddq}
-	1 ⁴	0	-	0	I _{ddq} test /burn-in
Hi-Z	-	1	-	X	

1. AGP4X mode input logic "0" is 0V.

2. AGP4X mode input logic "1" is 1.5V ± 0.1V.

3. During I_{ddq}, when LT = 1, the PAD input requires an AGP2X logic "0" of 0V.

4. During I_{ddq} when LT = 1, VDDAGP must be set to 3.3V. The 4X receiver will be turned off and the 2X receiver will become the bypass receiver.

5. During I_{ddq}, when LT = 1, the PAD input requires an AGP2X logic "1" of 3.3V ± 0.3V.

6. 4X mode will not be fully tested. The customer has the choice of whether or not to use this test I/O.



AGP 4X Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V VDDAGP = 1.4V T _j = 125°C Process = Slow	V _{dd} = 1.8V VDDAGP = 1.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V VDDAGP = 1.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	0.756 + 0.035D _{std}	0.472 + 0.027D _{std}	0.306 + 0.021D _{std}
		t _{PHL}	0.960 + 0.038D _{std}	0.609 + 0.028D _{std}	0.436 + 0.022D _{std}

AGP 2X Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V VDDAGP = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V VDDAGP = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V VDDAGP = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	2.152 + 0.044D _{std}	1.356 + 0.032D _{std}	0.980 + 0.025D _{std}
		t _{PHL}	2.154 + 0.052D _{std}	1.449 + 0.034D _{std}	1.042 + 0.027D _{std}

AGP 4X Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V VDDAGP = 1.4V T _j = 125°C Process = Slow	V _{dd} = 1.8V VDDAGP = 1.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V VDDAGP = 1.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	1.018 + 0.003N _{std}	0.477 + 0.001N _{std}	0.296 + 0.001N _{std}
		t _{PHL}	0.861 + 0.003N _{std}	0.600 + 0.002N _{std}	0.440 + 0.001N _{std}

AGP 2X Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $VDDAGP = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $VDDAGP = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $VDDAGP = 3.6V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.623 + 0.002N_{std}$	$0.433 + 0.001N_{std}$	$0.334 + 0.001N_{std}$
		t_{PHL}	$0.534 + 0.002N_{std}$	$0.394 + 0.001N_{std}$	$0.317 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	23.683
DI	12.460
LT	11.336
PAD (Receiver Input)	666.167
RG	9.820
TS	7.981
VREF	115.892
Internal	650.000
Cell Units	2 cells

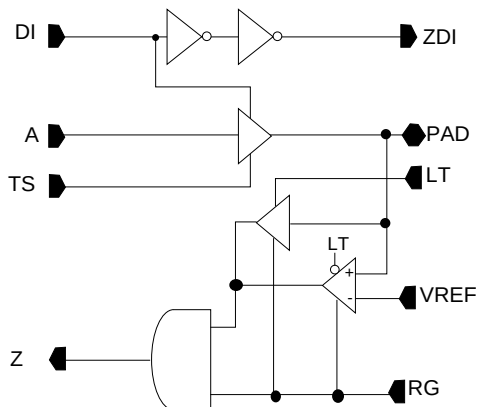
Cell: BAGP4XT, BAGP4XT_PM

Function: 1.5V AGP 4X Test 3-State CIO

Description:

Noninverting three-state driver/receiver for 1.5V AGP (accelerated graphics port) 4X interface. This is a bidirectional I/O. Output di/dt and performance are chosen by performance level selection. Receiver requires (off-chip) input reference ($V_{ddq}/2$).

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- LT DC current gate (I_{dd} test) input
- RG Receiver gate control
- VREF Voltage reference input
- PAD Driver output/receiver input
- ZDI Driver inhibit output (DI out)
- Z Receiver output



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	0	-	Hi-Z	DI
-	-	0	Hi-Z	DI
1	1	1	1 ¹	DI
0	1	1	0	DI

¹. Logical "1" = $V_{ddq} = V_{dd150} = 1.5V$.

Receiver Truth Table

Inputs				Output	Comments
PAD	LT	RG	VREF	Z	
-	-	0	-	0	Test mode
1 ¹	0	1	-	1	Functional mode
0 ²	0	1	-	0	Functional mode
1 ³	1	1	-	1	Bypass mode
0 ⁴	1	1	-	0	Bypass mode

1. PAD input requires AGP4X level "high." (AGP4X "high" is V_{ddq} .)

2. PAD input requires AGP4X level "low." (AGP4X "low" is 0.)

3. PAD input requires CMOS level "high." (CMOS "high" is V_{dd} .)

4. PAD input requires CMOS level "low." (CMOS "low" is 0.)

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd150} = 1.4V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd150} = 1.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd150} = 1.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$0.790 + 0.035D_{std}$	$0.526 + 0.026D_{std}$	$0.386 + 0.021D_{std}$
		t_{PHL}	$0.759 + 0.036D_{std}$	$0.513 + 0.025D_{std}$	$0.376 + 0.021D_{std}$
	B	t_{PLH}	$0.616 + 0.034D_{std}$	$0.437 + 0.025D_{std}$	$0.342 + 0.021D_{std}$
		t_{PHL}	$0.623 + 0.035D_{std}$	$0.454 + 0.025D_{std}$	$0.358 + 0.020D_{std}$
	C	t_{PLH}	$0.501 + 0.034D_{std}$	$0.359 + 0.025D_{std}$	$0.286 + 0.021D_{std}$
		t_{PHL}	$0.526 + 0.034D_{std}$	$0.389 + 0.024D_{std}$	$0.310 + 0.020D_{std}$



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.374 + 0.001N _{std}	0.243 + 0.001N _{std}	0.162 + 0.001N _{std}
		t _{PHL}	0.372 + 0.001N _{std}	0.246 + 0.001N _{std}	0.166 + 0.001N _{std}
	B	t _{PLH}	0.373 + 0.001N _{std}	0.245 + 0.001N _{std}	0.164 + 0.001N _{std}
		t _{PHL}	0.371 + 0.001N _{std}	0.247 + 0.001N _{std}	0.167 + 0.001N _{std}
	C	t _{PLH}	0.373 + 0.001N _{std}	0.245 + 0.001N _{std}	0.164 + 0.001N _{std}
		t _{PHL}	0.371 + 0.001N _{std}	0.247 + 0.001N _{std}	0.167 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	24.792	26.812	29.317
DI	3.937	3.937	3.945
LT	3.996	3.996	3.996
PAD (Receiver Input)	396.250	396.250	396.250
RG	7.409	7.409	7.409
TS	3.098	3.096	3.095
VREF	110.708	110.708	110.708
Internal	345.034	350.596	356.999
Cell Units	1 cell	1 cell	1 cell

Cell: BATAUDMAT, BATAUDMAT_PM

Function: 3.3V (5V Protected) Test UDMA 33/66/100 Data and Strobe 3-State CIO

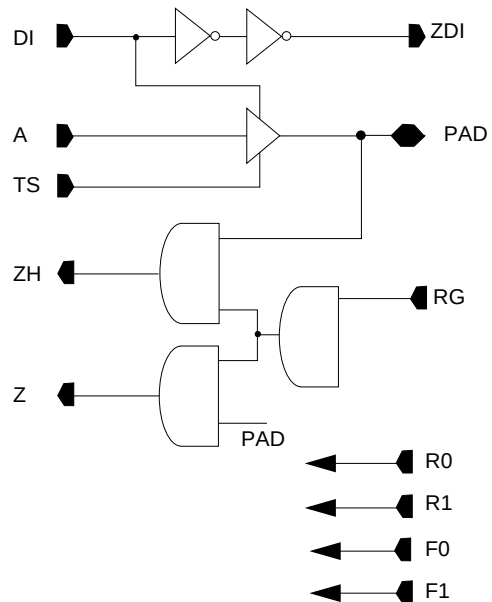
Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with UDMA 33, 66, and 100 Mb/s off-chip bidirectional data buses. Performance level C is used for data; performance level D is used for strobe. R0, R1, F0, and F1 are input control pins to change the output slew rate. R0 and R1 are for rising slew rate; F0 and F1 are for falling. The slew rate inputs need to be observable in a latch or latches so that the logic circuits and wires for the slew rate controls can be tested. The different slew rates cannot be measured during I/O test. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

This I/O should not be used in a high-speed test locations, such as a PLL clock receiver.

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RG	Receiver gate control
PAD	Driver output/receiver input
Z	Non-hysteresis receiver output
ZH	Hysteresis receiver output
ZDI	Driver inhibit output (DI out)
R0	Rising slew rate control input1
R1	Rising slew rate control input 2
F0	Falling slew rate control input1
F1	Falling slew rate control input 2

Pin Group: (Z, ZH): (1, 2)





Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X

Slew Rate Control Truth Table

Slew Rate Control (rising)		Slew Rate Control (falling)		Outputs (PAD)	
R0	R1	F0	F1	Rise (Mb/s)	Fall (Mb/s)
0	0	X	X	33 slow	-
0	1	X	X	33 fast	-
1	0	X	X	66	-
1	1	X	X	100	-
X	X	0	0	-	33 slow
X	X	0	1	-	33 fast
X	X	1	0	-	66
X	X	1	1	-	100

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	C	t_{PLH}	$4.342 + 0.062D_{std}$	$2.860 + 0.043D_{std}$	$2.097 + 0.034D_{std}$
		t_{PHL}	$6.096 + 0.045D_{std}$	$4.127 + 0.030D_{std}$	$2.979 + 0.023D_{std}$
	D	t_{PLH}	$4.461 + 0.060D_{std}$	$2.957 + 0.042D_{std}$	$2.187 + 0.032D_{std}$
		t_{PHL}	$6.274 + 0.044D_{std}$	$4.327 + 0.028D_{std}$	$3.158 + 0.021D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	C	t _{PLH}	0.822 + 0.003N _{std}	0.552 + 0.002N _{std}	0.419 + 0.002N _{std}
		t _{PHL}	1.143 + 0.001N _{std}	0.899 + 0.001N _{std}	0.754 + 0.001N _{std}
PAD-ZH		t _{PLH}	5.640 + 0.003N _{std}	3.310 + 0.002N _{std}	2.218 + 0.002N _{std}
		t _{PHL}	4.650 + 0.003N _{std}	3.424 + 0.002N _{std}	2.713 + 0.001N _{std}
PAD-Z	D	t _{PLH}	0.831 + 0.003N _{std}	0.548 + 0.002N _{std}	0.407 + 0.002N _{std}
		t _{PHL}	1.155 + 0.001N _{std}	0.907 + 0.001N _{std}	0.757 + 0.001N _{std}
PAD-ZH		t _{PLH}	5.727 + 0.003N _{std}	3.318 + 0.002N _{std}	2.221 + 0.001N _{std}
		t _{PHL}	4.643 + 0.003N _{std}	3.424 + 0.002N _{std}	2.711 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	C	D
A	4.002	3.986
DI	2.628	2.622
F0	4.543	4.543
F1	4.358	4.358
PAD (Receiver Input)	530.792	530.917
R0	4.474	4.474
R1	4.503	4.503
RG	1.120	1.119
TS	2.290	2.285
Internal	979.000	979.000
Cell Units	1 cell	1 cell

Cell: BC1820T, BC1820T_PM

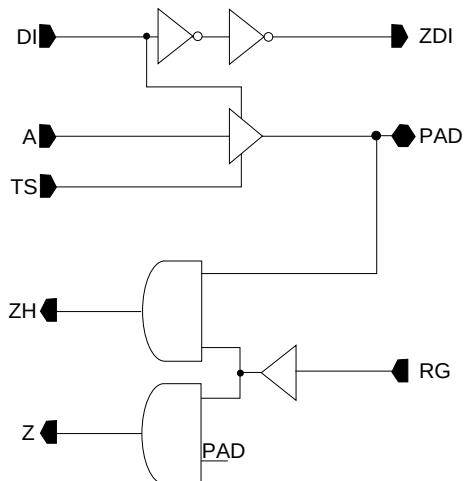
Function: 1.8V CMOS Test 20 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. If RG is not used, it should be tied to V_{dd} .

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
RG Receiver gate control
PAD Driver output/receiver input
ZH Hysteresis receiver output
Z Non-hysteresis receiver output
ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.529 + 0.033D _{std}	1.120 + 0.024D _{std}	0.829 + 0.019D _{std}
		t _{PHL}	1.375 + 0.032D _{std}	0.998 + 0.022D _{std}	0.751 + 0.017D _{std}
	B	t _{PLH}	1.320 + 0.030D _{std}	0.976 + 0.022D _{std}	0.735 + 0.017D _{std}
		t _{PHL}	1.215 + 0.030D _{std}	0.881 + 0.020D _{std}	0.671 + 0.015D _{std}
	C	t _{PLH}	1.000 + 0.028D _{std}	0.718 + 0.020D _{std}	0.539 + 0.016D _{std}
		t _{PHL}	0.941 + 0.028D _{std}	0.664 + 0.019D _{std}	0.500 + 0.014D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.264 + 0.000N _{std}	0.189 + 0.000N _{std}	0.146 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.205 + 0.000N _{std}	0.164 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.460 + 0.000N _{std}	0.337 + 0.000N _{std}	0.276 + 0.000N _{std}
		t _{PHL}	0.404 + 0.001N _{std}	0.330 + 0.000N _{std}	0.270 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.265 + 0.000N _{std}	0.185 + 0.000N _{std}	0.140 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.203 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.266 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.265 + 0.000N _{std}	0.185 + 0.000N _{std}	0.139 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.203 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.266 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

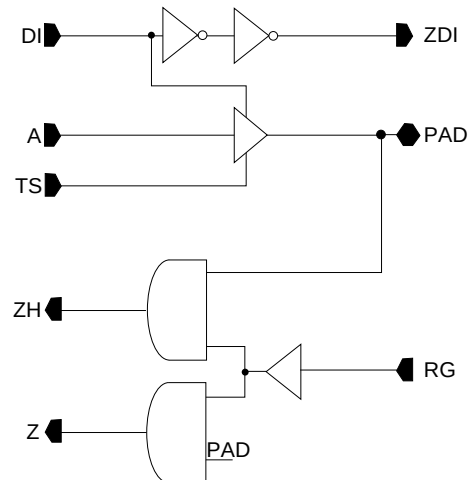
Input Pins	Performance Level		
	A	B	C
A	14.604	15.495	15.798
DI	3.737	3.747	3.757
PAD (Receiver Input)	501.042	501.042	500.458
RG	1.919	1.919	1.919
TS	3.016	3.019	3.022
Internal	635.065	644.740	650.955
Cell Units	1 cell	1 cell	1 cell

Cell: BC1835T, BC1835T_PM
Function: 1.8V CMOS Test 35 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. If RG is not used, it should be tied to V_{dd} .

A Driver data input
 TS Driver three-state control
 DI Driver inhibit input (DI in)
 RG Receiver gate control
 PAD Driver output/receiver input
 ZH Hysteresis receiver output
 Z Non-hysteresis receiver output
 ZDI Driver inhibit output (DI out)



Pin Group: (Z, ZH): (0, 2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.466 + 0.046D _{std}	1.079 + 0.035D _{std}	0.811 + 0.029D _{std}
		t _{PHL}	1.336 + 0.046D _{std}	0.978 + 0.033D _{std}	0.743 + 0.027D _{std}
	B	t _{PLH}	1.198 + 0.043D _{std}	0.893 + 0.032D _{std}	0.685 + 0.026D _{std}
		t _{PHL}	1.061 + 0.044D _{std}	0.788 + 0.031D _{std}	0.615 + 0.025D _{std}
	C	t _{PLH}	0.895 + 0.042D _{std}	0.655 + 0.031D _{std}	0.507 + 0.026D _{std}
		t _{PHL}	0.827 + 0.043D _{std}	0.609 + 0.030D _{std}	0.478 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.264 + 0.000N _{std}	0.189 + 0.000N _{std}	0.146 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.205 + 0.000N _{std}	0.165 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.461 + 0.000N _{std}	0.337 + 0.000N _{std}	0.276 + 0.000N _{std}
		t _{PHL}	0.404 + 0.001N _{std}	0.331 + 0.000N _{std}	0.270 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.140 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.203 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.267 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.140 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.203 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.267 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.687	15.221	15.617
DI	3.748	3.736	3.747
PAD (Receiver Input)	457.292	457.500	457.292
RG	1.919	1.919	1.919
TS	3.023	3.020	3.019
Internal	656.439	673.907	689.066
Cell Units	1 cell	1 cell	1 cell

Cell: BC1850T, BC1850T_PM

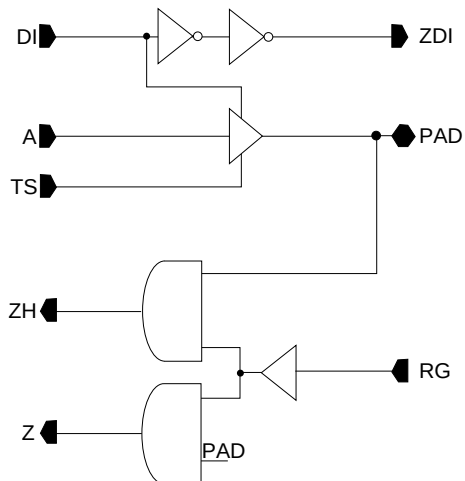
Function: 1.8V CMOS Test 50 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. If RG is not used, it should be tied to V_{dd} .

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RG	Receiver gate control
PAD	Driver output/receiver input
ZH	Hysteresis receiver output
Z	Non-hysteresis receiver output
ZDI	Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.332 + 0.063D _{std}	0.987 + 0.048D _{std}	0.742 + 0.040D _{std}
		t _{PHL}	1.201 + 0.064D _{std}	0.883 + 0.046D _{std}	0.674 + 0.039D _{std}
	B	t _{PLH}	1.045 + 0.060D _{std}	0.776 + 0.045D _{std}	0.601 + 0.038D _{std}
		t _{PHL}	0.895 + 0.062D _{std}	0.680 + 0.045D _{std}	0.539 + 0.037D _{std}
	C	t _{PLH}	0.811 + 0.060D _{std}	0.624 + 0.045D _{std}	0.499 + 0.038D _{std}
		t _{PHL}	0.736 + 0.062D _{std}	0.563 + 0.045D _{std}	0.460 + 0.037D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.264 + 0.000N _{std}	0.189 + 0.000N _{std}	0.146 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.205 + 0.000N _{std}	0.164 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.461 + 0.000N _{std}	0.337 + 0.000N _{std}	0.276 + 0.000N _{std}
		t _{PHL}	0.404 + 0.001N _{std}	0.331 + 0.000N _{std}	0.270 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.140 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.204 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.267 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.140 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.204 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.267 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.643	14.579	15.646
DI	3.748	3.748	3.757
PAD (Receiver Input)	407.792	407.792	407.792
RG	1.919	1.919	1.919
TS	3.015	3.020	3.021
Internal	646.122	644.065	651.812
Cell Units	1 cell	1 cell	1 cell

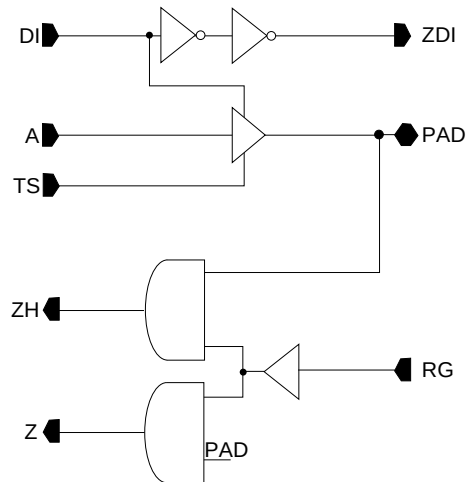
Cell: BC1865T, BC1865T_PM
Function: 1.8V CMOS Test 65 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. If RG is not used, it should be tied to V_{dd} .

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
RG Receiver gate control
PAD Driver output/receiver input
ZH Hysteresis receiver output
Z Non-hysteresis receiver output
ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.174 + 0.081D _{std}	0.875 + 0.061D _{std}	0.662 + 0.051D _{std}
		t _{PHL}	1.052 + 0.083D _{std}	0.772 + 0.060D _{std}	0.588 + 0.049D _{std}
	B	t _{PLH}	0.897 + 0.079D _{std}	0.691 + 0.059D _{std}	0.558 + 0.049D _{std}
		t _{PHL}	0.794 + 0.081D _{std}	0.631 + 0.058D _{std}	0.503 + 0.048D _{std}
	C	t _{PLH}	0.667 + 0.078D _{std}	0.536 + 0.059D _{std}	0.448 + 0.050D _{std}
		t _{PHL}	0.645 + 0.081D _{std}	0.515 + 0.058D _{std}	0.430 + 0.048D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.264 + 0.000N _{std}	0.189 + 0.000N _{std}	0.146 + 0.000N _{std}
PAD-ZH		t _{PHL}	0.252 + 0.001N _{std}	0.205 + 0.000N _{std}	0.165 + 0.000N _{std}
		t _{PLH}	0.461 + 0.000N _{std}	0.337 + 0.000N _{std}	0.276 + 0.000N _{std}
		t _{PHL}	0.404 + 0.001N _{std}	0.331 + 0.000N _{std}	0.270 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.140 + 0.000N _{std}
PAD-ZH		t _{PHL}	0.252 + 0.001N _{std}	0.204 + 0.000N _{std}	0.161 + 0.000N _{std}
		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.267 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.140 + 0.000N _{std}
PAD-ZH		t _{PHL}	0.252 + 0.001N _{std}	0.204 + 0.000N _{std}	0.161 + 0.000N _{std}
		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.267 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.676	14.630	15.710
DI	3.748	3.751	3.757
PAD (Receiver Input)	368.583	368.708	368.708
RG	1.919	1.919	1.919
TS	3.025	3.025	3.019
Internal	590.652	592.057	602.945
Cell Units	1 cell	1 cell	1 cell

Cell: BC1890T, BC1890T_PM

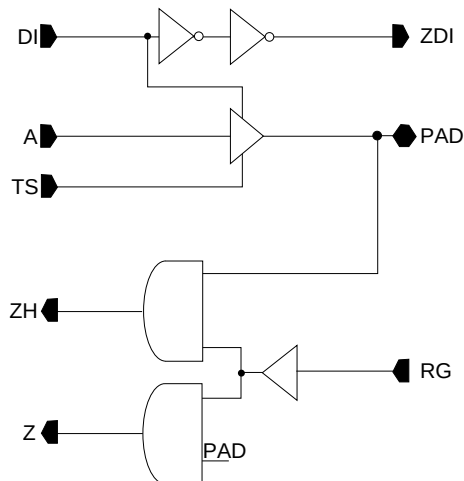
Function: 1.8V CMOS Test 90 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. If RG is not used, it should be tied to V_{dd} .

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
RG Receiver gate control
PAD Driver output/receiver input
ZH Hysteresis receiver output
Z Non-hysteresis receiver output
ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	0.995 + 0.112D _{std}	0.743 + 0.084D _{std}	0.568 + 0.071D _{std}
		t _{PHL}	0.922 + 0.113D _{std}	0.673 + 0.082D _{std}	0.514 + 0.069D _{std}
	B	t _{PLH}	0.795 + 0.110D _{std}	0.609 + 0.083D _{std}	0.440 + 0.071D _{std}
		t _{PHL}	0.727 + 0.111D _{std}	0.601 + 0.081D _{std}	0.504 + 0.068D _{std}
	C	t _{PLH}	0.560 + 0.109D _{std}	0.421 + 0.084D _{std}	0.318 + 0.071D _{std}
		t _{PHL}	0.560 + 0.111D _{std}	0.486 + 0.080D _{std}	0.413 + 0.068D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.264 + 0.000N _{std}	0.189 + 0.000N _{std}	0.146 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.205 + 0.000N _{std}	0.165 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.461 + 0.000N _{std}	0.337 + 0.000N _{std}	0.277 + 0.000N _{std}
		t _{PHL}	0.404 + 0.001N _{std}	0.331 + 0.000N _{std}	0.270 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.140 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.204 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.463 + 0.000N _{std}	0.336 + 0.000N _{std}	0.274 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.267 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.266 + 0.000N _{std}	0.185 + 0.000N _{std}	0.140 + 0.000N _{std}
		t _{PHL}	0.252 + 0.001N _{std}	0.204 + 0.000N _{std}	0.161 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.464 + 0.000N _{std}	0.336 + 0.000N _{std}	0.274 + 0.000N _{std}
		t _{PHL}	0.405 + 0.001N _{std}	0.330 + 0.000N _{std}	0.267 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.743	14.748	16.307
DI	3.753	3.760	3.758
PAD (Receiver Input)	341.083	341.083	341.083
RG	1.919	1.919	1.919
TS	3.024	3.024	3.025
Internal	571.366	564.711	580.181
Cell Units	1 cell	1 cell	1 cell

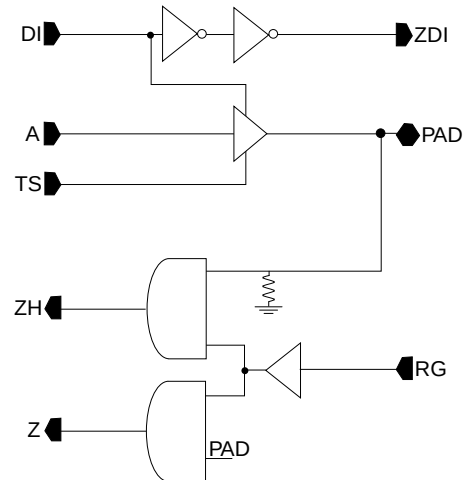
Cell: BC1820PDT, BC1820PDT_PM

Function: 1.8V CMOS Test 20 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)



Pin Group: (Z, ZH): (0, 2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
L	1	0	0



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.534 + 0.033D _{std}	1.125 + 0.024D _{std}	0.834 + 0.019D _{std}
		t _{PHL}	1.367 + 0.032D _{std}	0.990 + 0.022D _{std}	0.741 + 0.017D _{std}
	B	t _{PLH}	1.324 + 0.030D _{std}	0.980 + 0.022D _{std}	0.738 + 0.017D _{std}
		t _{PHL}	1.208 + 0.030D _{std}	0.876 + 0.020D _{std}	0.667 + 0.015D _{std}
	C	t _{PLH}	1.002 + 0.028D _{std}	0.721 + 0.020D _{std}	0.541 + 0.016D _{std}
		t _{PHL}	0.938 + 0.028D _{std}	0.661 + 0.019D _{std}	0.498 + 0.014D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.275 + 0.000N _{std}	0.206 + 0.000N _{std}	0.164 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.192 + 0.000N _{std}	0.149 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.473 + 0.000N _{std}	0.354 + 0.000N _{std}	0.296 + 0.000N _{std}
		t _{PHL}	0.398 + 0.001N _{std}	0.319 + 0.000N _{std}	0.256 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.355 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.399 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.355 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.399 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.594	15.483	15.791
DI	3.737	3.748	3.757
PAD (Receiver Input)	502.625	502.625	502.625
RG	1.919	1.919	1.919
TS	3.018	3.022	3.022
Internal	647.343	657.544	662.579
Cell Units	1 cell	1 cell	1 cell

Cell: BC1835PDT, BC1835PDT_PM

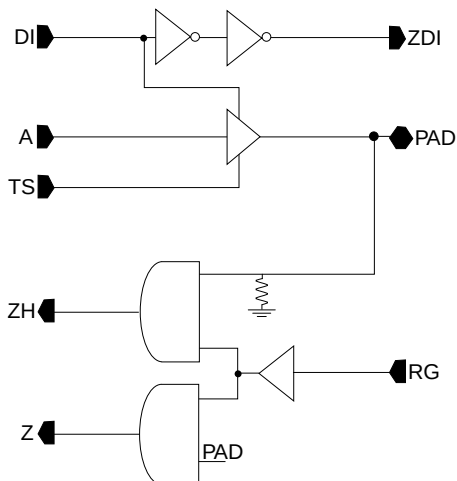
Function: 1.8V CMOS Test 35 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
L	1	0	0

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.472 + 0.046D _{std}	1.086 + 0.035D _{std}	0.818 + 0.029D _{std}
		t _{PHL}	1.328 + 0.046D _{std}	0.969 + 0.033D _{std}	0.735 + 0.027D _{std}
	B	t _{PLH}	1.201 + 0.043D _{std}	0.897 + 0.032D _{std}	0.690 + 0.027D _{std}
		t _{PHL}	1.057 + 0.043D _{std}	0.783 + 0.031D _{std}	0.610 + 0.025D _{std}
	C	t _{PLH}	0.897 + 0.042D _{std}	0.658 + 0.031D _{std}	0.510 + 0.026D _{std}
		t _{PHL}	0.824 + 0.043D _{std}	0.606 + 0.030D _{std}	0.476 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.276 + 0.000N _{std}	0.206 + 0.000N _{std}	0.165 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.191 + 0.000N _{std}	0.149 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.473 + 0.000N _{std}	0.355 + 0.000N _{std}	0.296 + 0.000N _{std}
		t _{PHL}	0.398 + 0.001N _{std}	0.319 + 0.000N _{std}	0.256 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.694	15.232	15.615
DI	3.737	3.737	3.747
PAD (Receiver Input)	458.708	458.708	458.750
RG	1.919	1.919	1.919
TS	3.023	3.021	3.022
Internal	704.119	712.315	731.642
Cell Units	1 cell	1 cell	1 cell

Cell: BC1850PDT, BC1850PDT_PM

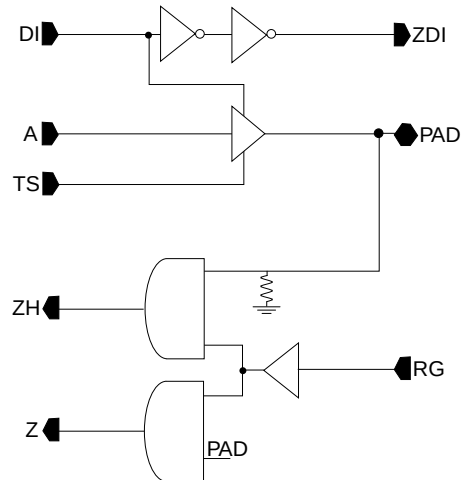
Function: 1.8V CMOS Test 50 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
L	1	0	0



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.338 + 0.063D _{std}	0.993 + 0.048D _{std}	0.748 + 0.040D _{std}
		t _{PHL}	1.192 + 0.063D _{std}	0.874 + 0.046D _{std}	0.666 + 0.038D _{std}
	B	t _{PLH}	1.048 + 0.060D _{std}	0.781 + 0.046D _{std}	0.607 + 0.038D _{std}
		t _{PHL}	0.891 + 0.061D _{std}	0.676 + 0.044D _{std}	0.535 + 0.037D _{std}
	C	t _{PLH}	0.813 + 0.060D _{std}	0.627 + 0.045D _{std}	0.502 + 0.038D _{std}
		t _{PHL}	0.734 + 0.061D _{std}	0.560 + 0.044D _{std}	0.457 + 0.036D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.276 + 0.000N _{std}	0.206 + 0.000N _{std}	0.165 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.191 + 0.000N _{std}	0.149 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.473 + 0.000N _{std}	0.355 + 0.000N _{std}	0.296 + 0.000N _{std}
		t _{PHL}	0.399 + 0.001N _{std}	0.319 + 0.000N _{std}	0.256 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.246 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.246 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.640	14.645	15.653
DI	3.734	3.745	3.754
PAD (Receiver Input)	409.167	409.208	409.208
RG	1.919	1.919	1.919
TS	3.015	3.020	3.022
Internal	732.790	733.277	739.740
Cell Units	1 cell	1 cell	1 cell

Cell: BC1865PDT, BC1865PDT_PM

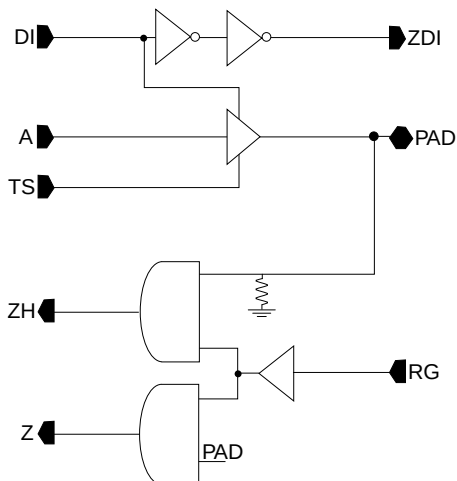
Function: 1.8V CMOS Test 65 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
L	1	0	0

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.179 + 0.082D _{std}	0.881 + 0.062D _{std}	0.668 + 0.052D _{std}
		t _{PHL}	1.044 + 0.081D _{std}	0.762 + 0.058D _{std}	0.581 + 0.048D _{std}
	B	t _{PLH}	0.902 + 0.079D _{std}	0.695 + 0.060D _{std}	0.564 + 0.050D _{std}
		t _{PHL}	0.789 + 0.080D _{std}	0.616 + 0.057D _{std}	0.499 + 0.047D _{std}
	C	t _{PLH}	0.668 + 0.079D _{std}	0.541 + 0.059D _{std}	0.450 + 0.050D _{std}
		t _{PHL}	0.639 + 0.079D _{std}	0.506 + 0.057D _{std}	0.412 + 0.047D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.276 + 0.000N _{std}	0.206 + 0.000N _{std}	0.165 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.191 + 0.000N _{std}	0.149 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.473 + 0.000N _{std}	0.355 + 0.000N _{std}	0.296 + 0.000N _{std}
		t _{PHL}	0.399 + 0.001N _{std}	0.319 + 0.000N _{std}	0.256 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.246 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.277 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.246 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.680	14.688	15.692
DI	3.740	3.740	3.754
PAD (Receiver Input)	370.083	370.167	370.167
RG	1.919	1.919	1.919
TS	3.025	3.025	3.021
Internal	727.411	729.298	741.846
Cell Units	1 cell	1 cell	1 cell

Cell: BC1890PDT, BC1890PDT_PM

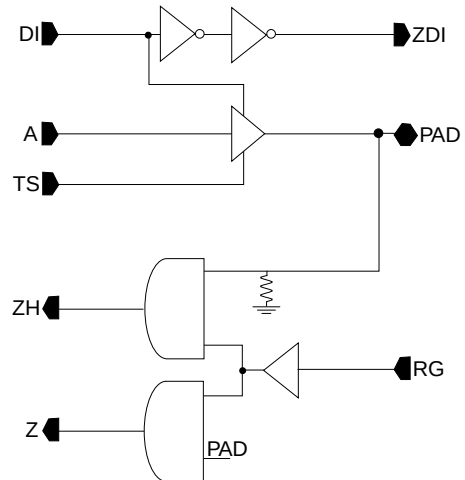
Function: 1.8V CMOS Test 90 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
L	1	0	0



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.000 + 0.113D _{std}	0.749 + 0.086D _{std}	0.574 + 0.072D _{std}
		t _{PHL}	0.912 + 0.111D _{std}	0.664 + 0.080D _{std}	0.506 + 0.067D _{std}
	B	t _{PLH}	0.786 + 0.111D _{std}	0.572 + 0.085D _{std}	0.456 + 0.072D _{std}
		t _{PHL}	0.722 + 0.109D _{std}	0.592 + 0.079D _{std}	0.491 + 0.066D _{std}
	C	t _{PLH}	0.557 + 0.111D _{std}	0.444 + 0.084D _{std}	0.361 + 0.072D _{std}
		t _{PHL}	0.556 + 0.109D _{std}	0.475 + 0.079D _{std}	0.414 + 0.065D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.276 + 0.000N _{std}	0.206 + 0.000N _{std}	0.165 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.192 + 0.000N _{std}	0.149 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.473 + 0.000N _{std}	0.355 + 0.000N _{std}	0.296 + 0.000N _{std}
		t _{PHL}	0.399 + 0.001N _{std}	0.319 + 0.000N _{std}	0.256 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.278 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.246 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.278 + 0.000N _{std}	0.204 + 0.000N _{std}	0.160 + 0.000N _{std}
		t _{PHL}	0.245 + 0.001N _{std}	0.189 + 0.000N _{std}	0.144 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.476 + 0.000N _{std}	0.356 + 0.000N _{std}	0.295 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.317 + 0.000N _{std}	0.251 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.740	14.740	16.318
DI	3.749	3.747	3.755
PAD (Receiver Input)	342.375	342.375	342.375
RG	1.919	1.919	1.919
TS	3.026	3.024	3.025
Internal	789.798	782.707	797.359
Cell Units	1 cell	1 cell	1 cell

Cell: BC1820PUT, BC1820PUT_PM

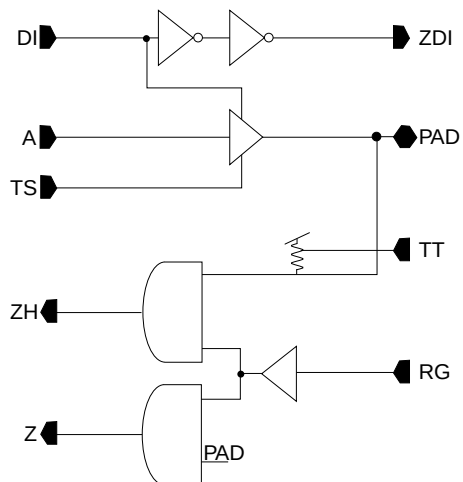
Function: 1.8V CMOS Test 20 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (1.8V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.518 + 0.032D _{std}	1.111 + 0.024D _{std}	0.823 + 0.019D _{std}
		t _{PHL}	1.380 + 0.032D _{std}	1.002 + 0.022D _{std}	0.754 + 0.017D _{std}
	B	t _{PLH}	1.312 + 0.030D _{std}	0.970 + 0.021D _{std}	0.730 + 0.017D _{std}
		t _{PHL}	1.218 + 0.030D _{std}	0.884 + 0.020D _{std}	0.673 + 0.015D _{std}
	C	t _{PLH}	0.995 + 0.027D _{std}	0.715 + 0.020D _{std}	0.536 + 0.015D _{std}
		t _{PHL}	0.944 + 0.028D _{std}	0.666 + 0.019D _{std}	0.501 + 0.014D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.254 + 0.000N _{std}	0.176 + 0.000N _{std}	0.132 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.220 + 0.000N _{std}	0.181 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.451 + 0.000N _{std}	0.325 + 0.000N _{std}	0.263 + 0.000N _{std}
		t _{PHL}	0.419 + 0.001N _{std}	0.347 + 0.000N _{std}	0.287 + 0.000N _{std}



Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.220 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.285 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.220 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.285 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.601	15.483	15.791
DI	3.738	3.737	3.752
PAD (Receiver Input)	502.458	502.542	502.417
RG	1.919	1.919	1.919
TS	3.033	3.039	3.043
TT	1.393	1.393	1.393
Internal	356.921	348.585	341.513
Cell Units	1 cell	1 cell	1 cell

Cell: BC1835PUT, BC1835PUT_PM

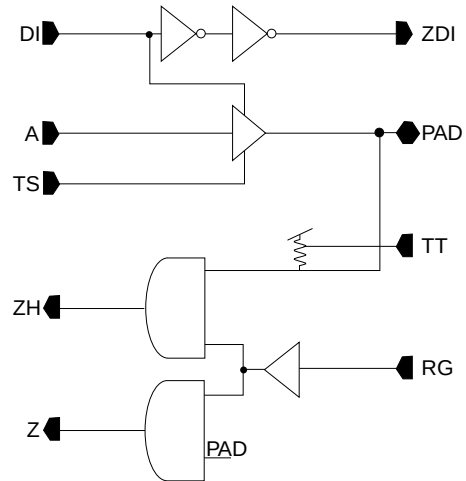
Function: 1.8V CMOS Test 35 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (1.8V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.452 + 0.046D _{std}	1.068 + 0.035D _{std}	0.803 + 0.029D _{std}
		t _{PHL}	1.342 + 0.046D _{std}	0.983 + 0.033D _{std}	0.747 + 0.027D _{std}
	B	t _{PLH}	1.190 + 0.042D _{std}	0.887 + 0.032D _{std}	0.679 + 0.026D _{std}
		t _{PHL}	1.064 + 0.044D _{std}	0.791 + 0.031D _{std}	0.617 + 0.025D _{std}
	C	t _{PLH}	0.891 + 0.041D _{std}	0.652 + 0.031D _{std}	0.505 + 0.026D _{std}
		t _{PHL}	0.829 + 0.043D _{std}	0.611 + 0.031D _{std}	0.480 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.254 + 0.000N _{std}	0.176 + 0.000N _{std}	0.131 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.220 + 0.000N _{std}	0.181 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.452 + 0.000N _{std}	0.325 + 0.000N _{std}	0.264 + 0.000N _{std}
		t _{PHL}	0.419 + 0.001N _{std}	0.347 + 0.000N _{std}	0.287 + 0.000N _{std}

Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.221 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.286 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.267 + 0.001N _{std}	0.221 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.286 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.687	15.220	15.615
DI	3.738	3.738	3.749
PAD (Receiver Input)	458.917	458.917	458.917
RG	1.919	1.919	1.919
TS	3.037	3.039	3.040
TT	1.393	1.393	1.393
Internal	356.000	348.000	341.000
Cell Units	1 cell	1 cell	1 cell

Cell: BC1850PUT, BC1850PUT_PM

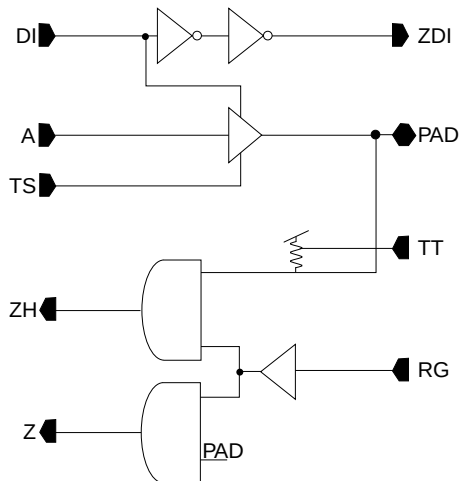
Function: 1.8V CMOS Test 50 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (1.8V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.319 + 0.062D _{std}	0.976 + 0.047D _{std}	0.734 + 0.039D _{std}
		t _{PHL}	1.206 + 0.064D _{std}	0.887 + 0.047D _{std}	0.678 + 0.039D _{std}
	B	t _{PLH}	1.037 + 0.059D _{std}	0.771 + 0.045D _{std}	0.600 + 0.037D _{std}
		t _{PHL}	0.897 + 0.063D _{std}	0.682 + 0.045D _{std}	0.541 + 0.037D _{std}
	C	t _{PLH}	0.802 + 0.059D _{std}	0.620 + 0.044D _{std}	0.495 + 0.037D _{std}
		t _{PHL}	0.737 + 0.062D _{std}	0.565 + 0.045D _{std}	0.458 + 0.037D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.254 + 0.000N _{std}	0.176 + 0.000N _{std}	0.131 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.220 + 0.000N _{std}	0.181 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.452 + 0.000N _{std}	0.325 + 0.000N _{std}	0.263 + 0.000N _{std}
		t _{PHL}	0.419 + 0.001N _{std}	0.348 + 0.000N _{std}	0.288 + 0.000N _{std}



Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.267 + 0.001N _{std}	0.221 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.286 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.267 + 0.001N _{std}	0.221 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.286 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.640	14.572	15.654
DI	3.739	3.750	3.749
PAD (Receiver Input)	409.042	409.167	409.083
RG	1.919	1.919	1.919
TS	3.040	3.042	3.041
TT	1.393	1.393	1.393
Internal	412.404	406.252	403.243
Cell Units	1 cell	1 cell	1 cell

Cell: BC1865PUT, BC1865PUT_PM

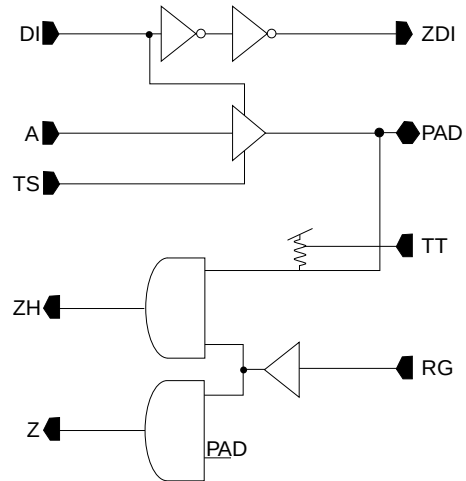
Function: 1.8V CMOS Test 65 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (1.8V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.122 + 0.080D _{std}	0.838 + 0.060D _{std}	0.630 + 0.050D _{std}
		t _{PHL}	1.023 + 0.083D _{std}	0.749 + 0.061D _{std}	0.568 + 0.050D _{std}
	B	t _{PLH}	0.891 + 0.077D _{std}	0.688 + 0.058D _{std}	0.549 + 0.049D _{std}
		t _{PHL}	0.795 + 0.082D _{std}	0.621 + 0.059D _{std}	0.510 + 0.049D _{std}
	C	t _{PLH}	0.662 + 0.077D _{std}	0.531 + 0.058D _{std}	0.435 + 0.049D _{std}
		t _{PHL}	0.647 + 0.081D _{std}	0.509 + 0.059D _{std}	0.430 + 0.049D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.246 + 0.000N _{std}	0.173 + 0.000N _{std}	0.130 + 0.000N _{std}
		t _{PHL}	0.258 + 0.001N _{std}	0.214 + 0.000N _{std}	0.174 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.444 + 0.000N _{std}	0.322 + 0.000N _{std}	0.262 + 0.000N _{std}
		t _{PHL}	0.410 + 0.001N _{std}	0.340 + 0.000N _{std}	0.281 + 0.000N _{std}

Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.221 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.286 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.221 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.420 + 0.001N _{std}	0.348 + 0.000N _{std}	0.286 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	15.321	14.688	15.703
DI	3.895	3.759	3.752
PAD (Receiver Input)	332.667	370.000	370.083
RG	1.933	1.919	1.919
TS	3.029	3.042	3.043
TT	1.398	1.393	1.393
Internal	397.242	408.436	392.889
Cell Units	1 cell	1 cell	1 cell

Cell: BC1890PUT, BC1890PUT_PM

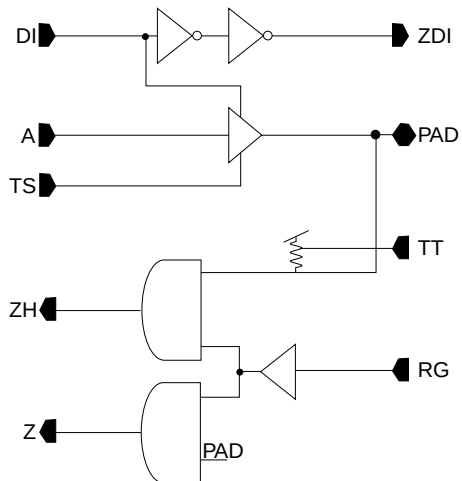
Function: 1.8V CMOS Test 90 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 1.8V CMOS off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (1.8V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	0.981 + 0.109D _{std}	0.732 + 0.082D _{std}	0.558 + 0.069D _{std}
		t _{PHL}	0.923 + 0.115D _{std}	0.676 + 0.083D _{std}	0.516 + 0.070D _{std}
	B	t _{PLH}	0.771 + 0.107D _{std}	0.601 + 0.081D _{std}	0.435 + 0.069D _{std}
		t _{PHL}	0.722 + 0.113D _{std}	0.594 + 0.082D _{std}	0.506 + 0.069D _{std}
	C	t _{PLH}	0.564 + 0.107D _{std}	0.424 + 0.082D _{std}	0.344 + 0.069D _{std}
		t _{PHL}	0.555 + 0.113D _{std}	0.483 + 0.082D _{std}	0.419 + 0.069D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.254 + 0.000N _{std}	0.176 + 0.000N _{std}	0.131 + 0.000N _{std}
		t _{PHL}	0.266 + 0.001N _{std}	0.220 + 0.000N _{std}	0.181 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.452 + 0.000N _{std}	0.325 + 0.000N _{std}	0.263 + 0.000N _{std}
		t _{PHL}	0.419 + 0.001N _{std}	0.348 + 0.000N _{std}	0.288 + 0.000N _{std}



Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.267 + 0.001N _{std}	0.221 + 0.000N _{std}	0.180 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.421 + 0.001N _{std}	0.349 + 0.000N _{std}	0.286 + 0.000N _{std}
PAD-Z	C	t _{PLH}	0.255 + 0.000N _{std}	0.171 + 0.000N _{std}	0.124 + 0.000N _{std}
		t _{PHL}	0.267 + 0.001N _{std}	0.221 + 0.000N _{std}	0.179 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.454 + 0.000N _{std}	0.323 + 0.000N _{std}	0.259 + 0.000N _{std}
		t _{PHL}	0.421 + 0.001N _{std}	0.349 + 0.000N _{std}	0.286 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	14.721	14.740	16.317
DI	3.752	3.760	3.758
PAD (Receiver Input)	342.417	342.458	342.458
RG	1.919	1.919	1.919
TS	3.045	3.045	3.041
TT	1.393	1.393	1.393
Internal	388.000	404.000	396.000
Cell Units	1 cell	1 cell	1 cell

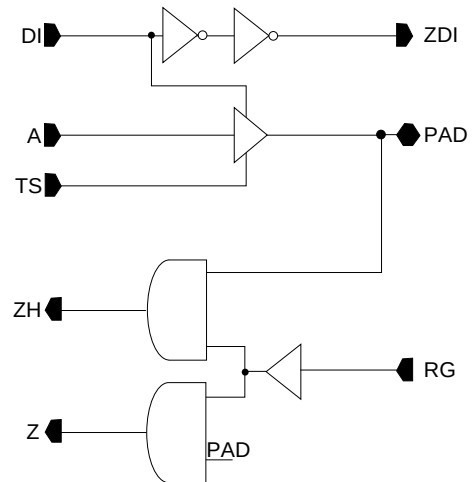
Cell: BC2520T, BC2520T_PM
Function: 2.5V CMOS Test 20 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
RG Receiver gate control
PAD Driver output/receiver input
ZH Hysteresis receiver output
Z Non-hysteresis receiver output
ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.647 + 0.021D _{std}	1.191 + 0.016D _{std}	0.877 + 0.013D _{std}
		t _{PHL}	1.627 + 0.023D _{std}	1.182 + 0.016D _{std}	0.875 + 0.013D _{std}
	B	t _{PLH}	1.526 + 0.019D _{std}	1.082 + 0.014D _{std}	0.794 + 0.011D _{std}
		t _{PHL}	1.495 + 0.021D _{std}	1.069 + 0.015D _{std}	0.794 + 0.011D _{std}
	C	t _{PLH}	1.350 + 0.018D _{std}	0.931 + 0.013D _{std}	0.680 + 0.010D _{std}
		t _{PHL}	1.337 + 0.020D _{std}	0.936 + 0.014D _{std}	0.686 + 0.011D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.292 + 0.001N _{std}	0.220 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.310 + 0.001N _{std}	0.250 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.433 + 0.001N _{std}	0.346 + 0.001N _{std}
		t _{PHL}	0.549 + 0.002N _{std}	0.452 + 0.001N _{std}	0.373 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.427 + 0.002N _{std}	0.289 + 0.001N _{std}	0.215 + 0.001N _{std}
		t _{PHL}	0.397 + 0.002N _{std}	0.310 + 0.001N _{std}	0.246 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.434 + 0.001N _{std}	0.345 + 0.001N _{std}
		t _{PHL}	0.557 + 0.002N _{std}	0.457 + 0.001N _{std}	0.376 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.427 + 0.002N _{std}	0.289 + 0.001N _{std}	0.215 + 0.001N _{std}
		t _{PHL}	0.397 + 0.002N _{std}	0.310 + 0.001N _{std}	0.246 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.434 + 0.001N _{std}	0.345 + 0.001N _{std}
		t _{PHL}	0.557 + 0.002N _{std}	0.457 + 0.001N _{std}	0.376 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.243	11.243	11.243
DI	7.652	7.652	7.660
PAD (Receiver Input)	536.083	536.083	536.083
RG	2.001	2.001	2.001
TS	6.542	6.542	6.542
Internal	475.085	466.218	464.576
Cell Units	1 cell	1 cell	1 cell

Cell: BC2535T, BC2535T_PM

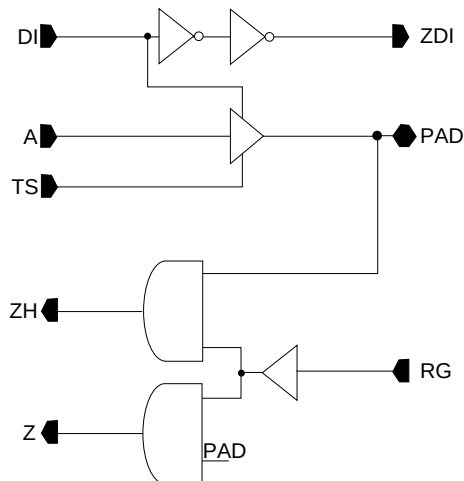
Function: 2.5V CMOS Test 35 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
RG Receiver gate control
PAD Driver output/receiver input
ZH Hysteresis receiver output
Z Non-hysteresis receiver output
ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.616 + 0.031D _{std}	1.173 + 0.023D _{std}	0.864 + 0.019D _{std}
		t _{PHL}	1.590 + 0.032D _{std}	1.156 + 0.023D _{std}	0.857 + 0.019D _{std}
	B	t _{PLH}	1.473 + 0.029D _{std}	1.062 + 0.022D _{std}	0.796 + 0.018D _{std}
		t _{PHL}	1.439 + 0.030D _{std}	1.046 + 0.022D _{std}	0.788 + 0.018D _{std}
	C	t _{PLH}	1.291 + 0.029D _{std}	0.908 + 0.021D _{std}	0.677 + 0.018D _{std}
		t _{PHL}	1.274 + 0.030D _{std}	0.909 + 0.021D _{std}	0.679 + 0.018D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.436 + 0.002N _{std}	0.307 + 0.001N _{std}	0.237 + 0.001N _{std}
		t _{PHL}	0.388 + 0.002N _{std}	0.299 + 0.001N _{std}	0.237 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.620 + 0.002N _{std}	0.449 + 0.001N _{std}	0.363 + 0.001N _{std}
		t _{PHL}	0.547 + 0.002N _{std}	0.442 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
		t _{PHL}	0.393 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.626 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
		t _{PHL}	0.393 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.626 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.244	11.231	11.243
DI	7.651	7.652	7.661
PAD (Receiver Input)	491.583	491.583	491.583
RG	2.001	2.001	2.001
TS	6.542	6.542	6.542
Internal	604.561	603.192	601.635
Cell Units	1 cell	1 cell	1 cell

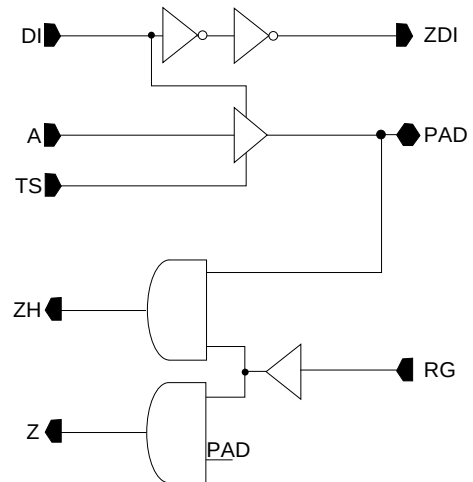
Cell: BC2550T, BC2550T_PM
Function: 2.5V CMOS Test 50 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
RG Receiver gate control
PAD Driver output/receiver input
ZH Hysteresis receiver output
Z Non-hysteresis receiver output
ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.581 + 0.041D _{std}	1.155 + 0.032D _{std}	0.857 + 0.026D _{std}
		t _{PHL}	1.550 + 0.042D _{std}	1.133 + 0.031D _{std}	0.842 + 0.026D _{std}
	B	t _{PLH}	1.421 + 0.040D _{std}	1.048 + 0.030D _{std}	0.799 + 0.025D _{std}
		t _{PHL}	1.386 + 0.041D _{std}	1.028 + 0.030D _{std}	0.789 + 0.025D _{std}
	C	t _{PLH}	1.238 + 0.040D _{std}	0.891 + 0.030D _{std}	0.677 + 0.026D _{std}
		t _{PHL}	1.218 + 0.040D _{std}	0.889 + 0.030D _{std}	0.679 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.292 + 0.001N _{std}	0.221 + 0.001N _{std}
		t _{PHL}	0.393 + 0.002N _{std}	0.310 + 0.001N _{std}	0.250 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.433 + 0.001N _{std}	0.346 + 0.001N _{std}
		t _{PHL}	0.550 + 0.002N _{std}	0.452 + 0.001N _{std}	0.374 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.428 + 0.002N _{std}	0.289 + 0.001N _{std}	0.216 + 0.001N _{std}
		t _{PHL}	0.397 + 0.002N _{std}	0.310 + 0.001N _{std}	0.246 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.435 + 0.001N _{std}	0.345 + 0.001N _{std}
		t _{PHL}	0.557 + 0.002N _{std}	0.457 + 0.001N _{std}	0.376 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.428 + 0.002N _{std}	0.289 + 0.001N _{std}	0.216 + 0.001N _{std}
		t _{PHL}	0.397 + 0.002N _{std}	0.310 + 0.001N _{std}	0.246 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.435 + 0.001N _{std}	0.345 + 0.001N _{std}
		t _{PHL}	0.557 + 0.002N _{std}	0.457 + 0.001N _{std}	0.376 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.244	11.243	11.244
DI	7.651	7.651	7.661
PAD (Receiver Input)	462.042	462.042	462.042
RG	2.001	2.001	2.001
TS	6.542	6.542	6.542
Internal	730.228	730.567	731.401
Cell Units	1 cell	1 cell	1 cell

Cell: BC2565T, BC2565T_PM

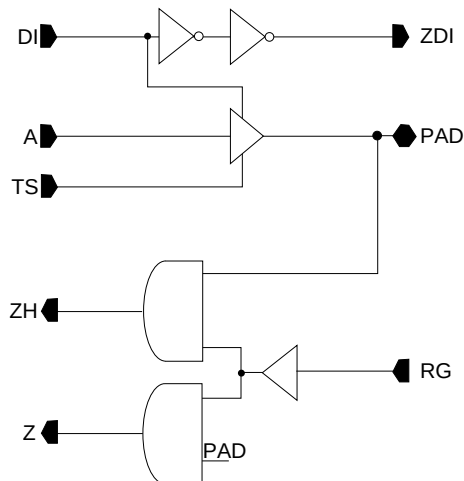
Function: 2.5V CMOS Test 65 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
RG Receiver gate control
PAD Driver output/receiver input
ZH Hysteresis receiver output
Z Non-hysteresis receiver output
ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.562 + 0.052D _{std}	1.144 + 0.040D _{std}	0.855 + 0.034D _{std}
		t _{PHL}	1.548 + 0.052D _{std}	1.119 + 0.040D _{std}	0.835 + 0.034D _{std}
	B	t _{PLH}	1.379 + 0.051D _{std}	1.042 + 0.039D _{std}	0.804 + 0.034D _{std}
		t _{PHL}	1.350 + 0.051D _{std}	1.024 + 0.039D _{std}	0.796 + 0.033D _{std}
	C	t _{PLH}	1.197 + 0.051D _{std}	0.878 + 0.039D _{std}	0.681 + 0.034D _{std}
		t _{PHL}	1.181 + 0.051D _{std}	0.878 + 0.038D _{std}	0.682 + 0.033D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.427 + 0.002N _{std}	0.292 + 0.001N _{std}	0.221 + 0.001N _{std}
		t _{PHL}	0.393 + 0.002N _{std}	0.310 + 0.001N _{std}	0.250 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.433 + 0.001N _{std}	0.346 + 0.001N _{std}
t _{PHL}		0.550 + 0.002N _{std}	0.452 + 0.001N _{std}	0.374 + 0.001N _{std}	
PAD-Z	B	t _{PLH}	0.428 + 0.002N _{std}	0.289 + 0.001N _{std}	0.216 + 0.001N _{std}
		t _{PHL}	0.397 + 0.002N _{std}	0.310 + 0.001N _{std}	0.246 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.435 + 0.001N _{std}	0.345 + 0.001N _{std}
		t _{PHL}	0.557 + 0.002N _{std}	0.457 + 0.001N _{std}	0.376 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.428 + 0.002N _{std}	0.289 + 0.001N _{std}	0.216 + 0.001N _{std}
		t _{PHL}	0.397 + 0.002N _{std}	0.310 + 0.001N _{std}	0.246 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.435 + 0.001N _{std}	0.345 + 0.001N _{std}
		t _{PHL}	0.557 + 0.002N _{std}	0.457 + 0.001N _{std}	0.376 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.243	11.243	11.243
DI	7.652	7.652	7.404
PAD (Receiver Input)	450.708	450.708	450.708
RG	2.001	2.001	2.001
TS	6.542	6.542	6.349
Internal	844.724	846.103	845.441
Cell Units	1 cell	1 cell	1 cell

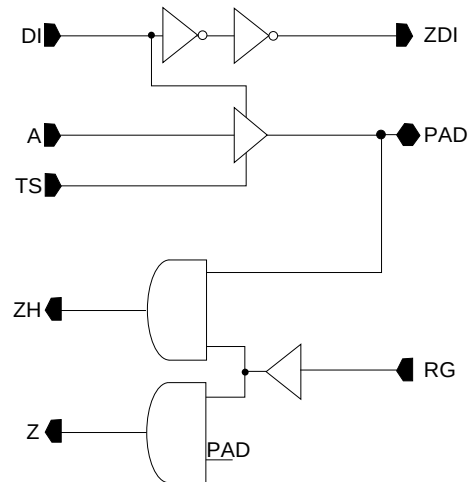
Cell: BC2590T, BC2590T_PM
Function: 2.5V CMOS Test 90 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
RG Receiver gate control
PAD Driver output/receiver input
ZH Hysteresis receiver output
Z Non-hysteresis receiver output
ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.353 + 0.074D _{std}	0.982 + 0.056D _{std}	0.733 + 0.047D _{std}
		t _{PHL}	1.374 + 0.075D _{std}	1.015 + 0.055D _{std}	0.756 + 0.047D _{std}
	B	t _{PLH}	1.209 + 0.073D _{std}	0.924 + 0.056D _{std}	0.731 + 0.047D _{std}
		t _{PHL}	1.311 + 0.073D _{std}	1.018 + 0.054D _{std}	0.806 + 0.045D _{std}
	C	t _{PLH}	1.043 + 0.073D _{std}	0.763 + 0.056D _{std}	0.611 + 0.047D _{std}
		t _{PHL}	1.121 + 0.073D _{std}	0.863 + 0.054D _{std}	0.685 + 0.045D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.291 + 0.001N _{std}	0.220 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.392 + 0.002N _{std}	0.310 + 0.001N _{std}	0.251 + 0.001N _{std}
		t _{PLH}	0.610 + 0.002N _{std}	0.432 + 0.001N _{std}	0.345 + 0.001N _{std}
		t _{PHL}	0.548 + 0.002N _{std}	0.451 + 0.001N _{std}	0.373 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.431 + 0.002N _{std}	0.288 + 0.001N _{std}	0.215 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}
		t _{PLH}	0.619 + 0.002N _{std}	0.434 + 0.001N _{std}	0.344 + 0.001N _{std}
		t _{PHL}	0.556 + 0.002N _{std}	0.456 + 0.001N _{std}	0.376 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.431 + 0.002N _{std}	0.288 + 0.001N _{std}	0.215 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.396 + 0.002N _{std}	0.309 + 0.001N _{std}	0.245 + 0.001N _{std}
		t _{PLH}	0.619 + 0.002N _{std}	0.434 + 0.001N _{std}	0.344 + 0.001N _{std}
		t _{PHL}	0.556 + 0.002N _{std}	0.456 + 0.001N _{std}	0.376 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	10.686	10.686	10.685
DI	7.151	7.151	7.178
PAD (Receiver Input)	326.625	326.625	326.625
RG	2.002	2.002	2.002
TS	6.167	6.167	6.166
Internal	786.000	776.000	771.000
Cell Units	1 cell	1 cell	1 cell

Cell: BC2520PDT, BC2520PDT_PM

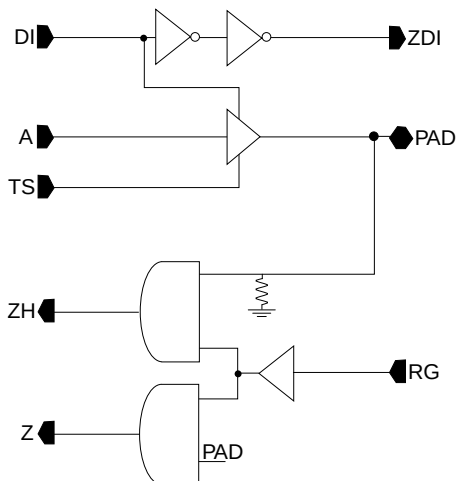
Function: 2.5V CMOS Test 20 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
L	1	0	0

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.649 + 0.021D _{std}	1.194 + 0.016D _{std}	0.879 + 0.013D _{std}
		t _{PHL}	1.623 + 0.023D _{std}	1.177 + 0.016D _{std}	0.871 + 0.013D _{std}
	B	t _{PLH}	1.528 + 0.019D _{std}	1.084 + 0.014D _{std}	0.796 + 0.011D _{std}
		t _{PHL}	1.492 + 0.021D _{std}	1.066 + 0.015D _{std}	0.791 + 0.011D _{std}
	C	t _{PLH}	1.351 + 0.018D _{std}	0.933 + 0.013D _{std}	0.681 + 0.010D _{std}
		t _{PHL}	1.334 + 0.020D _{std}	0.934 + 0.014D _{std}	0.684 + 0.011D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.435 + 0.002N _{std}	0.306 + 0.001N _{std}	0.237 + 0.001N _{std}
		t _{PHL}	0.388 + 0.002N _{std}	0.299 + 0.001N _{std}	0.236 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.620 + 0.002N _{std}	0.448 + 0.001N _{std}	0.363 + 0.001N _{std}
t _{PHL}		0.546 + 0.002N _{std}	0.442 + 0.001N _{std}	0.362 + 0.001N _{std}	
PAD-Z	B	t _{PLH}	0.440 + 0.002N _{std}	0.305 + 0.001N _{std}	0.233 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.625 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.440 + 0.002N _{std}	0.305 + 0.001N _{std}	0.233 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.625 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.277	11.277	11.244
DI	7.659	7.661	7.659
PAD (Receiver Input)	538.042	538.083	538.042
RG	2.002	2.004	2.002
TS	6.503	6.503	6.501
Internal	426.326	417.487	416.071
Cell Units	1 cell	1 cell	1 cell

Cell: BC2535PDT, BC2535PDT_PM

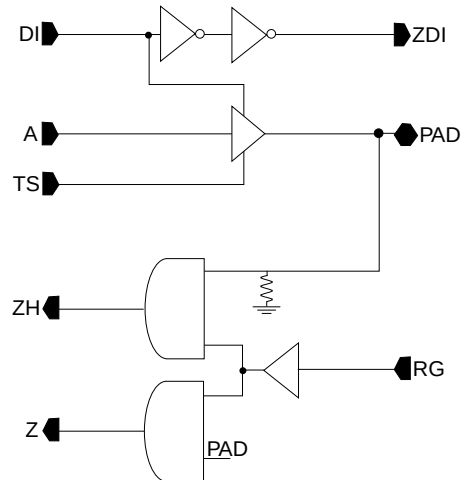
Function: 2.5V CMOS Test 35 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
L	1	0	0



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.619 + 0.031D _{std}	1.177 + 0.023D _{std}	0.867 + 0.019D _{std}
		t _{PHL}	1.585 + 0.032D _{std}	1.151 + 0.023D _{std}	0.853 + 0.019D _{std}
	B	t _{PLH}	1.475 + 0.029D _{std}	1.064 + 0.022D _{std}	0.798 + 0.018D _{std}
		t _{PHL}	1.436 + 0.030D _{std}	1.041 + 0.022D _{std}	0.784 + 0.018D _{std}
	C	t _{PLH}	1.293 + 0.029D _{std}	0.909 + 0.022D _{std}	0.678 + 0.018D _{std}
		t _{PHL}	1.272 + 0.030D _{std}	0.906 + 0.021D _{std}	0.676 + 0.017D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.436 + 0.002N _{std}	0.307 + 0.001N _{std}	0.237 + 0.001N _{std}
		t _{PHL}	0.388 + 0.002N _{std}	0.299 + 0.001N _{std}	0.237 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.620 + 0.002N _{std}	0.449 + 0.001N _{std}	0.363 + 0.001N _{std}
		t _{PHL}	0.547 + 0.002N _{std}	0.442 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
		t _{PHL}	0.393 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.626 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.625 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.265	11.263	11.230
DI	7.661	7.661	7.661
PAD (Receiver Input)	491.583	491.583	491.625
RG	2.002	2.004	2.002
TS	6.503	6.503	6.501
Internal	539.430	539.529	538.205
Cell Units	1 cell	1 cell	1 cell

Cell: BC2550PDT, BC2550PDT_PM

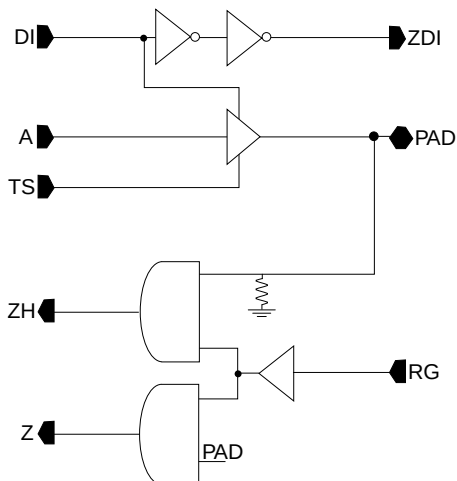
Function: 2.5V CMOS Test 50 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
L	1	0	0

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.584 + 0.041D _{std}	1.159 + 0.032D _{std}	0.860 + 0.027D _{std}
		t _{PHL}	1.549 + 0.042D _{std}	1.127 + 0.031D _{std}	0.837 + 0.026D _{std}
	B	t _{PLH}	1.422 + 0.040D _{std}	1.050 + 0.031D _{std}	0.802 + 0.026D _{std}
		t _{PHL}	1.383 + 0.041D _{std}	1.023 + 0.030D _{std}	0.784 + 0.025D _{std}
	C	t _{PLH}	1.238 + 0.040D _{std}	0.892 + 0.030D _{std}	0.686 + 0.025D _{std}
		t _{PHL}	1.217 + 0.040D _{std}	0.886 + 0.029D _{std}	0.675 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.436 + 0.002N _{std}	0.307 + 0.001N _{std}	0.237 + 0.001N _{std}
		t _{PHL}	0.388 + 0.002N _{std}	0.299 + 0.001N _{std}	0.237 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.620 + 0.002N _{std}	0.449 + 0.001N _{std}	0.363 + 0.001N _{std}
		t _{PHL}	0.547 + 0.002N _{std}	0.442 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.626 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.626 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.277	11.277	11.243
DI	7.661	7.661	7.661
PAD (Receiver Input)	464.083	464.083	464.083
RG	2.002	2.004	2.002
TS	6.503	6.503	6.501
Internal	643.220	645.197	646.386
Cell Units	1 cell	1 cell	1 cell

Cell: BC2565PDT, BC2565PDT_PM

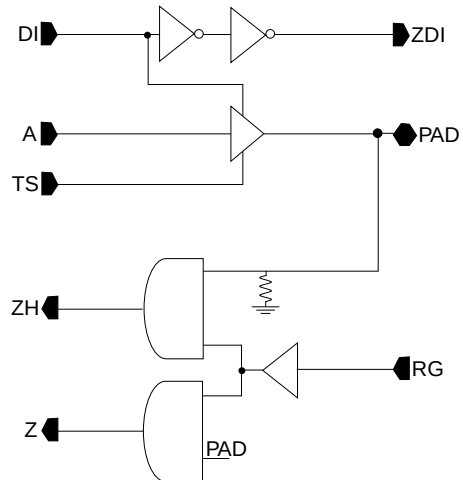
Function: 2.5V CMOS Test 65 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
L	1	0	0



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.564 + 0.052D _{std}	1.148 + 0.040D _{std}	0.858 + 0.034D _{std}
		t _{PHL}	1.549 + 0.051D _{std}	1.113 + 0.039D _{std}	0.830 + 0.033D _{std}
	B	t _{PLH}	1.381 + 0.051D _{std}	1.044 + 0.039D _{std}	0.807 + 0.034D _{std}
		t _{PHL}	1.348 + 0.051D _{std}	1.018 + 0.038D _{std}	0.794 + 0.032D _{std}
	C	t _{PLH}	1.199 + 0.051D _{std}	0.877 + 0.040D _{std}	0.684 + 0.034D _{std}
		t _{PHL}	1.182 + 0.050D _{std}	0.874 + 0.038D _{std}	0.678 + 0.032D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.436 + 0.002N _{std}	0.307 + 0.001N _{std}	0.237 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.388 + 0.002N _{std}	0.299 + 0.001N _{std}	0.237 + 0.001N _{std}
		t _{PLH}	0.620 + 0.002N _{std}	0.449 + 0.001N _{std}	0.363 + 0.001N _{std}
		t _{PHL}	0.547 + 0.002N _{std}	0.443 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PLH}	0.625 + 0.002N _{std}	0.452 + 0.001N _{std}	0.365 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PLH}	0.625 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.277	11.276	11.243
DI	7.661	7.661	7.661
PAD (Receiver Input)	452.625	452.625	452.625
RG	2.002	2.004	2.002
TS	6.503	6.503	6.501
Internal	739.179	741.932	741.667
Cell Units	1 cell	1 cell	1 cell

Cell: BC2590PDT, BC2590PDT_PM

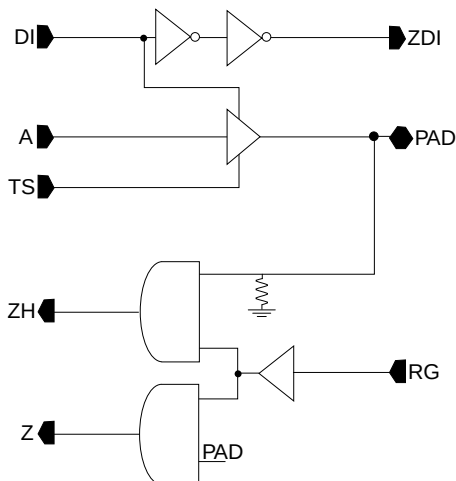
Function: 2.5V CMOS Test 90 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	L	DI
-	0	-	L	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
L	1	0	0

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.361 + 0.074D _{std}	0.981 + 0.057D _{std}	0.729 + 0.048D _{std}
		t _{PHL}	1.371 + 0.073D _{std}	1.001 + 0.054D _{std}	0.740 + 0.045D _{std}
	B	t _{PLH}	1.209 + 0.074D _{std}	0.924 + 0.056D _{std}	0.724 + 0.048D _{std}
		t _{PHL}	1.308 + 0.071D _{std}	1.003 + 0.052D _{std}	0.785 + 0.044D _{std}
	C	t _{PLH}	1.039 + 0.074D _{std}	0.778 + 0.056D _{std}	0.618 + 0.047D _{std}
		t _{PHL}	1.118 + 0.071D _{std}	0.850 + 0.052D _{std}	0.665 + 0.044D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.436 + 0.002N _{std}	0.307 + 0.001N _{std}	0.237 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.388 + 0.002N _{std}	0.299 + 0.001N _{std}	0.237 + 0.001N _{std}
		t _{PLH}	0.620 + 0.002N _{std}	0.449 + 0.001N _{std}	0.363 + 0.001N _{std}
		t _{PHL}	0.547 + 0.002N _{std}	0.442 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PLH}	0.625 + 0.002N _{std}	0.451 + 0.001N _{std}	0.365 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.392 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PLH}	0.625 + 0.002N _{std}	0.451 + 0.001N _{std}	0.365 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.241	11.240	11.241
DI	7.652	7.652	7.661
PAD (Receiver Input)	343.875	343.875	343.875
RG	2.002	2.002	2.002
TS	6.501	6.501	6.500
Internal	716.000	714.000	710.000
Cell Units	1 cell	1 cell	1 cell

Cell: BC2520PUT, BC2520PUT_PM

Function: 2.5V CMOS Test 20 Ohm 3-State CIO w/Pull-Up

Description:

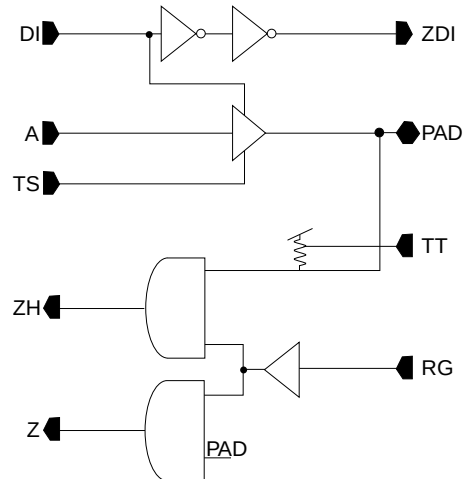
Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (2.5V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled





Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.642 + 0.021D_{std}$	$1.186 + 0.016D_{std}$	$0.874 + 0.012D_{std}$
		t_{PHL}	$1.629 + 0.023D_{std}$	$1.184 + 0.016D_{std}$	$0.876 + 0.013D_{std}$
	B	t_{PLH}	$1.522 + 0.019D_{std}$	$1.080 + 0.014D_{std}$	$0.792 + 0.011D_{std}$
		t_{PHL}	$1.498 + 0.021D_{std}$	$1.071 + 0.015D_{std}$	$0.795 + 0.012D_{std}$
	C	t_{PLH}	$1.348 + 0.018D_{std}$	$0.930 + 0.013D_{std}$	$0.679 + 0.010D_{std}$
		t_{PHL}	$1.338 + 0.020D_{std}$	$0.937 + 0.014D_{std}$	$0.687 + 0.011D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.419 + 0.002N _{std}	0.283 + 0.001N _{std}	0.210 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.403 + 0.002N _{std}	0.322 + 0.001N _{std}	0.263 + 0.001N _{std}
		t _{PLH}	0.604 + 0.002N _{std}	0.425 + 0.001N _{std}	0.336 + 0.001N _{std}
		t _{PHL}	0.561 + 0.002N _{std}	0.465 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.422 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
		t _{PLH}	0.613 + 0.002N _{std}	0.425 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.568 + 0.002N _{std}	0.471 + 0.001N _{std}	0.391 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.422 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
		t _{PLH}	0.613 + 0.002N _{std}	0.425 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.568 + 0.002N _{std}	0.471 + 0.001N _{std}	0.391 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.243	11.243	11.242
DI	7.652	7.652	7.653
PAD (Receiver Input)	537.625	537.625	537.625
RG	2.002	2.002	2.002
TS	6.503	6.503	6.503
TT	4.281	4.281	4.281
Internal	310.808	308.416	308.987
Cell Units	1 cell	1 cell	1 cell

Cell: BC2535PUT, BC2535PUT_PM

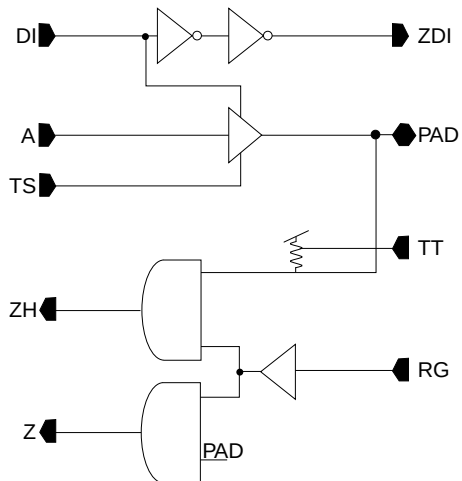
Function: 2.5V CMOS Test 35 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (2.5V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.611 + 0.031D _{std}	1.168 + 0.023D _{std}	0.861 + 0.019D _{std}
		t _{PHL}	1.593 + 0.032D _{std}	1.159 + 0.023D _{std}	0.859 + 0.019D _{std}
	B	t _{PLH}	1.469 + 0.029D _{std}	1.058 + 0.022D _{std}	0.793 + 0.018D _{std}
		t _{PHL}	1.441 + 0.031D _{std}	1.048 + 0.022D _{std}	0.789 + 0.018D _{std}
	C	t _{PLH}	1.290 + 0.028D _{std}	0.906 + 0.021D _{std}	0.675 + 0.018D _{std}
		t _{PHL}	1.275 + 0.030D _{std}	0.910 + 0.021D _{std}	0.680 + 0.018D _{std}



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.420 + 0.002N _{std}	0.283 + 0.001N _{std}	0.210 + 0.001N _{std}
		t _{PHL}	0.403 + 0.002N _{std}	0.322 + 0.001N _{std}	0.263 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.604 + 0.002N _{std}	0.425 + 0.001N _{std}	0.336 + 0.001N _{std}
		t _{PHL}	0.561 + 0.002N _{std}	0.465 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.425 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.425 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.471 + 0.001N _{std}	0.391 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.425 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.425 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.471 + 0.001N _{std}	0.391 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.230	11.244	11.230
DI	7.375	7.652	7.652
PAD (Receiver Input)	491.417	491.417	491.417
RG	2.002	2.002	2.002
TS	6.329	6.504	6.504
TT	4.281	4.281	4.281
Internal	350.400	353.347	352.903
Cell Units	1 cell	1 cell	1 cell

Cell: BC2550PUT, BC2550PUT_PM

Function: 2.5V CMOS Test 50 Ohm 3-State CIO w/Pull-Up

Description:

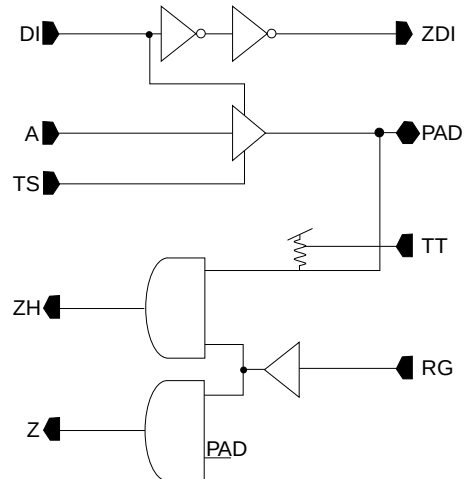
Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (2.5V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled





Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.575 + 0.041D_{std}$	$1.150 + 0.031D_{std}$	$0.853 + 0.026D_{std}$
		t_{PHL}	$1.552 + 0.042D_{std}$	$1.135 + 0.031D_{std}$	$0.844 + 0.026D_{std}$
	B	t_{PLH}	$1.417 + 0.040D_{std}$	$1.044 + 0.030D_{std}$	$0.795 + 0.025D_{std}$
		t_{PHL}	$1.387 + 0.041D_{std}$	$1.030 + 0.030D_{std}$	$0.790 + 0.025D_{std}$
	C	t_{PLH}	$1.238 + 0.039D_{std}$	$0.891 + 0.030D_{std}$	$0.675 + 0.025D_{std}$
		t_{PHL}	$1.220 + 0.041D_{std}$	$0.890 + 0.030D_{std}$	$0.680 + 0.025D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.420 + 0.002N _{std}	0.283 + 0.001N _{std}	0.210 + 0.001N _{std}
		t _{PHL}	0.403 + 0.002N _{std}	0.322 + 0.001N _{std}	0.263 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.604 + 0.002N _{std}	0.425 + 0.001N _{std}	0.336 + 0.001N _{std}
		t _{PHL}	0.562 + 0.002N _{std}	0.465 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.422 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.425 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.472 + 0.001N _{std}	0.391 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.422 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.425 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.472 + 0.001N _{std}	0.391 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.243	11.243	11.242
DI	7.651	7.652	7.651
PAD (Receiver Input)	463.833	463.792	463.833
RG	2.002	2.002	2.002
TS	6.504	6.504	6.504
TT	4.281	4.281	4.281
Internal	387.461	391.004	392.632
Cell Units	1 cell	1 cell	1 cell

Cell: BC2565PUT, BC2565PUT_PM

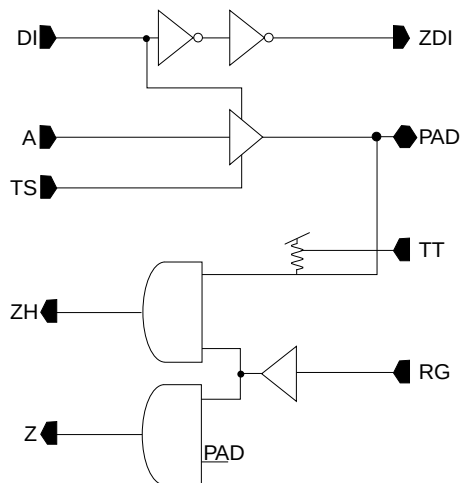
Function: 2.5V CMOS Test 65 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (2.5V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.556 + 0.051D _{std}	1.139 + 0.039D _{std}	0.850 + 0.033D _{std}
		t _{PHL}	1.546 + 0.052D _{std}	1.121 + 0.040D _{std}	0.837 + 0.034D _{std}
	B	t _{PLH}	1.377 + 0.050D _{std}	1.037 + 0.039D _{std}	0.808 + 0.033D _{std}
		t _{PHL}	1.350 + 0.052D _{std}	1.026 + 0.039D _{std}	0.803 + 0.033D _{std}
	C	t _{PLH}	1.197 + 0.050D _{std}	0.875 + 0.039D _{std}	0.677 + 0.033D _{std}
		t _{PHL}	1.181 + 0.051D _{std}	0.879 + 0.039D _{std}	0.683 + 0.033D _{std}



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.420 + 0.002N _{std}	0.283 + 0.001N _{std}	0.210 + 0.001N _{std}
		t _{PHL}	0.403 + 0.002N _{std}	0.322 + 0.001N _{std}	0.263 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.604 + 0.002N _{std}	0.425 + 0.001N _{std}	0.336 + 0.001N _{std}
		t _{PHL}	0.562 + 0.002N _{std}	0.465 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.423 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.426 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.472 + 0.001N _{std}	0.391 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.423 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.426 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.472 + 0.001N _{std}	0.391 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.244	11.243	11.243
DI	7.651	7.652	7.661
PAD (Receiver Input)	452.292	452.333	452.333
RG	2.002	2.002	2.002
TS	6.504	6.504	6.504
TT	4.281	4.281	4.281
Internal	415.121	418.902	418.842
Cell Units	1 cell	1 cell	1 cell

Cell: BC2590PUT, BC2590PUT_PM

Function: 2.5V CMOS Test 90 Ohm 3-State CIO w/Pull-Up

Description:

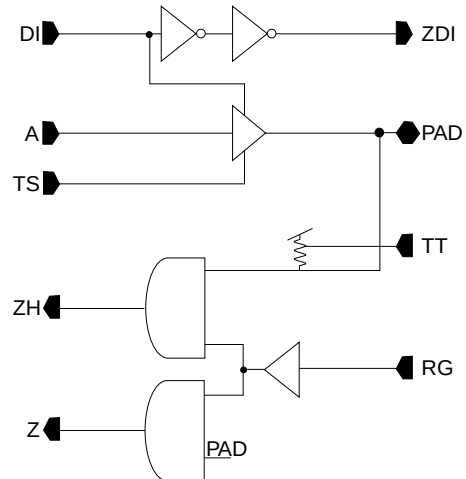
Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (2.5V) through 8k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled





Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.334 + 0.073D _{std}	0.972 + 0.055D _{std}	0.721 + 0.046D _{std}
		t _{PHL}	1.390 + 0.075D _{std}	1.013 + 0.056D _{std}	0.752 + 0.047D _{std}
	B	t _{PLH}	1.207 + 0.072D _{std}	0.918 + 0.055D _{std}	0.714 + 0.046D _{std}
		t _{PHL}	1.307 + 0.074D _{std}	1.013 + 0.054D _{std}	0.801 + 0.046D _{std}
	C	t _{PLH}	1.040 + 0.072D _{std}	0.771 + 0.055D _{std}	0.605 + 0.046D _{std}
		t _{PHL}	1.118 + 0.073D _{std}	0.859 + 0.054D _{std}	0.674 + 0.046D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.420 + 0.002N _{std}	0.283 + 0.001N _{std}	0.210 + 0.001N _{std}
		t _{PHL}	0.403 + 0.002N _{std}	0.323 + 0.001N _{std}	0.263 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.604 + 0.002N _{std}	0.425 + 0.001N _{std}	0.336 + 0.001N _{std}
		t _{PHL}	0.562 + 0.002N _{std}	0.465 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.425 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.426 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.472 + 0.001N _{std}	0.391 + 0.001N _{std}
PAD-Z	C	t _{PLH}	0.425 + 0.002N _{std}	0.279 + 0.001N _{std}	0.204 + 0.001N _{std}
		t _{PHL}	0.408 + 0.002N _{std}	0.323 + 0.001N _{std}	0.260 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.426 + 0.001N _{std}	0.334 + 0.001N _{std}
		t _{PHL}	0.569 + 0.002N _{std}	0.472 + 0.001N _{std}	0.391 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level		
	A	B	C
A	11.241	11.241	11.240
DI	7.661	7.661	7.661
PAD (Receiver Input)	343.750	343.750	343.750
RG	2.002	2.002	2.002
TS	6.503	6.503	6.503
TT	4.281	4.281	4.281
Internal	410.000	412.000	417.000
Cell Units	1 cell	1 cell	1 cell

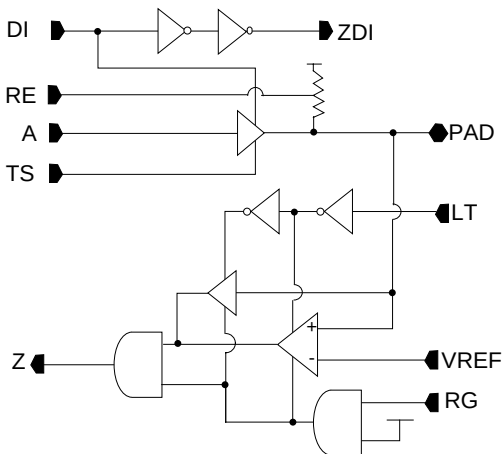
Cell: BGTLDLT, BGTLDLT_PM

Function: Test GTL CIO for Double Termination

Description:

Noninverting bidirectional driver/receiver with three-state control. Output di/dt and performance are chosen by performance level selection. Off-chip termination requires 25Ω to 1.2V or 1.5V (V_{TT}). On-chip termination is provided only for chip testing. Receiver requires (off chip) input reference ($V_{TT} \cdot 2/3$). RG and RI disable differential circuit within the receiver to reduce power consumption. A, TS, and Z must be wired to latches for boundary scan. If RG is not used, it should be tied to V_{dd} .

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RE	Reference enable input
RG	Receiver gate control
LT	DC current gate (I_{dd} test) input
VREF	Voltage reference input
PAD	Driver output/receiver input
Z	Non-hysteresis receiver output
ZDI	Driver inhibit output (DI out)



Driver Truth Table

Inputs				Outputs	
A	TS	DI	RE	PAD	ZDI
-	0	-	-	Hi-Z ¹	DI
-	-	0	-	Hi-Z ¹	DI
1	1	1	0	Hi-Z ¹	DI
0	1	1	0	0	DI
1	1	1	1	1	DI
0	1	1	1	0	DI

¹. PAD is Hi-Z if driver is not externally terminated.

Notes:

- RE = 1 enables on-chip terminator (to V_{dd}).
- Timing model will be based on driver terminated off-chip (25Ω to V_{TT}).
- $V_{TT} = 1.2V$ (GTL); $V_{TT} = 1.5V$ (GTL+).

Receiver Truth Table

Inputs			Output	Comments
PAD	LT	RG	Z	
-	-	0	0	Functional mode (user inhibit)
0 ¹	0	1	0	Functional mode
1 ¹	0	1	1	Functional mode
0 ²	1	1	0	CMOS bypass
1 ²	1	1	1	CMOS bypass

¹. PAD input requires GTL/GTL+ levels.

². PAD input requires CMOS levels.



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.111 + 0.020D_{std}$	$1.336 + 0.019D_{std}$	$1.247 + 0.020D_{std}$
		t_{PHL}	$1.527 + 0.010D_{std}$	$0.929 + 0.007D_{std}$	$0.603 + 0.005D_{std}$
	B	t_{PLH}	$0.674 + 0.018D_{std}$	$0.595 + 0.020D_{std}$	$0.531 + 0.020D_{std}$
		t_{PHL}	$1.056 + 0.008D_{std}$	$0.641 + 0.005D_{std}$	$0.414 + 0.004D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.574 + 0.001N_{std}$	$0.298 + 0.001N_{std}$	$0.193 + 0.001N_{std}$
		t_{PHL}	$0.624 + 0.001N_{std}$	$0.315 + 0.001N_{std}$	$0.206 + 0.001N_{std}$
	B	t_{PLH}	$0.586 + 0.001N_{std}$	$0.294 + 0.001N_{std}$	$0.187 + 0.001N_{std}$
		t_{PHL}	$0.626 + 0.001N_{std}$	$0.314 + 0.001N_{std}$	$0.203 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	8.472	15.963
DI	3.697	3.696
LT	2.892	2.892
PAD (Receiver Input)	371.500	372.833
RE	1.981	1.976
RG	4.733	4.733
TS	2.656	2.656
VREF	218.417	218.417
Internal	337.917	374.629
Cell Units	1 cell	1 cell

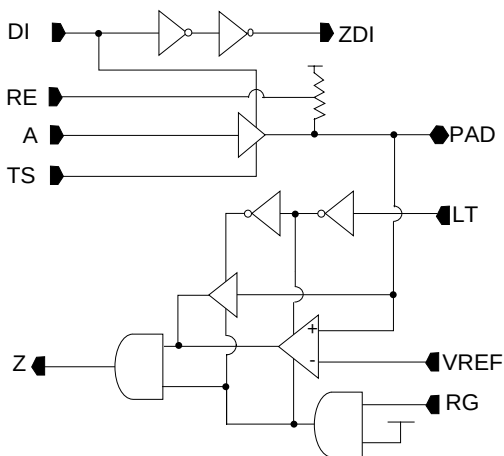
Cell: BGTLSL, BGTLSL_PM

Function: Test GTL CIO for Single Termination

Description:

Noninverting bidirectional driver/receiver with three-state control. Output di/dt and performance are chosen by performance level selection. Off-chip termination requires 50Ω to 1.2V or 1.5V (V_{TT}). On-chip termination is provided only for chip testing. Receiver requires (off chip) input reference ($V_{TT} \cdot 2/3$). RG and RI disable differential circuit within receiver to reduce power consumption. A, TS, and Z must be wired to latches for boundary scan. If RG is not used, it should be tied to Vdd.

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RE	Reference enable input
RG	Receiver gate control
LT	DC current gate (I_{dd} test) input
VREF	Voltage reference input
PAD	Driver output/receiver input
Z	Non-hysteresis receiver output
ZDI	Driver inhibit output (DI out)



Driver Truth Table

Inputs				Outputs	
A	TS	DI	RE	PAD	ZDI
-	0	-	-	Hi-Z ¹	DI
-	-	0	-	Hi-Z ¹	DI
1	1	1	0	Hi-Z ¹	DI
0	1	1	0	0	DI
1	1	1	1	1	DI
0	1	1	1	0	DI

¹. PAD is Hi-Z if driver is not externally terminated.

Notes:

- RE = 1 enables on-chip terminator (to V_{dd}).
- Timing model will be based on driver terminated off-chip (50Ω to V_{TT}).
- $V_{TT} = 1.2V$ (GTL); $V_{TT} = 1.5V$ (GTL+).

Receiver Truth Table

Inputs			Output	Comments
PAD	LT	RG	Z	
-	-	0	0	Functional mode (user inhibit)
0 ¹	0	1	0	Functional mode
1 ¹	0	1	1	Functional mode
0 ²	1	1	0	CMOS bypass
1 ²	1	1	1	CMOS bypass

¹. PAD input requires GTL/GTL+ levels.

². PAD input requires CMOS levels.



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$0.514 + 0.038D_{std}$	$0.462 + 0.042D_{std}$	$0.407 + 0.043D_{std}$
		t_{PHL}	$0.967 + 0.013D_{std}$	$0.632 + 0.009D_{std}$	$0.432 + 0.007D_{std}$
	B	t_{PLH}	$0.439 + 0.038D_{std}$	$0.352 + 0.043D_{std}$	$0.366 + 0.044D_{std}$
		t_{PHL}	$0.730 + 0.011D_{std}$	$0.470 + 0.007D_{std}$	$0.317 + 0.005D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.574 + 0.001N_{std}$	$0.299 + 0.001N_{std}$	$0.192 + 0.001N_{std}$
		t_{PHL}	$0.625 + 0.001N_{std}$	$0.315 + 0.001N_{std}$	$0.209 + 0.001N_{std}$
	B	t_{PLH}	$0.585 + 0.001N_{std}$	$0.294 + 0.001N_{std}$	$0.187 + 0.001N_{std}$
		t_{PHL}	$0.626 + 0.001N_{std}$	$0.314 + 0.001N_{std}$	$0.203 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	14.631	14.035
DI	3.703	3.704
LT	2.892	2.892
PAD (Receiver Input)	440.833	440.917
RE	1.982	1.983
RG	4.733	4.733
TS	2.657	2.657
VREF	218.417	218.417
Internal	374.102	422.796
Cell Units	1 cell	1 cell

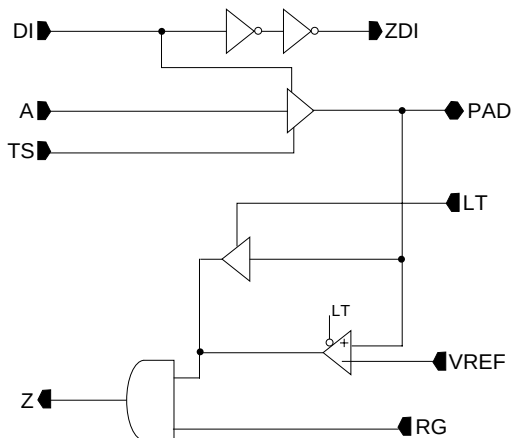
Cell: BHSTL18C1T, BHSTL18C1T_PM

Function: HSTL 1.8V Class 1 Test CIO

Description:

Noninverting bidirectional driver/receiver. Off-chip termination requires 50 ohms to $V_{ddq}/2$, where $V_{ddq} = V_{dd}$. Receiver requires (off-chip) input reference ($V_{ddq}/2$).

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
LT	DC current gate (I_{dd} test) input
RG	Receiver gate control
VREF	Voltage reference input
PAD	Driver output/receiver input
ZDI	Driver inhibit output (DI out)
Z	Receiver output



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	0	-	Hi-Z ¹	DI
-	-	0	Hi-Z ¹	DI
-	1	1	A	DI

¹. PAD is Hi-Z if driver is not externally terminated. PAD is at " $V_{ddq}/2$ " if driver is terminated (off-chip).

Notes:

- Logical "1" = $V_{ddq} = V_{dd} = 1.8V$.
- Timing model will be based on driver terminated off-chip.

Receiver Truth Table

Inputs				Output	Comments
PAD	LT	RG	VREF	Z	
-	-	0	-	0	Test mode
-	-	-	-	0	Test mode
1 ¹	0	1	-	1	Functional mode
0 ²	0	1	-	0	Functional mode
1 ³	1	1	-	1	Bypass mode
0 ⁴	1	1	-	0	Bypass mode

1. PAD input requires HSTL level "high" and $V_{ddq} < V_{dd}$.
2. PAD input requires HSTL level "low."
3. PAD input requires CMOS level "high" and $V_{ddq} = V_{dd}$.
4. PAD input requires CMOS level "low."

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$0.564 + 0.020D_{std}$	$0.448 + 0.016D_{std}$	$0.357 + 0.014D_{std}$
		t_{PHL}	$0.525 + 0.020D_{std}$	$0.407 + 0.015D_{std}$	$0.323 + 0.013D_{std}$
	B	t_{PLH}	$0.473 + 0.018D_{std}$	$0.375 + 0.015D_{std}$	$0.305 + 0.013D_{std}$
		t_{PHL}	$0.430 + 0.019D_{std}$	$0.338 + 0.015D_{std}$	$0.278 + 0.013D_{std}$



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.397 + 0.001N _{std}	0.265 + 0.001N _{std}	0.191 + 0.000N _{std}
		t _{PHL}	0.411 + 0.001N _{std}	0.265 + 0.001N _{std}	0.175 + 0.000N _{std}
	B	t _{PLH}	0.391 + 0.001N _{std}	0.267 + 0.001N _{std}	0.195 + 0.000N _{std}
		t _{PHL}	0.402 + 0.001N _{std}	0.263 + 0.001N _{std}	0.174 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

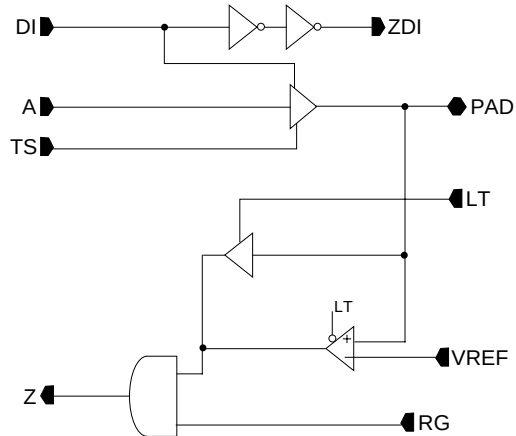
Input Pins	Performance Level	
	A	B
A	24.878	24.903
DI	3.542	3.541
LT	3.080	3.081
PAD (Receiver Input)	357.042	356.042
RG	6.693	6.693
TS	2.984	2.984
VREF	109.358	109.358
Internal	251.635	255.105
Cell Units	1 cell	1 cell

Cell: BHSTL18C2T, BHSTL18C2T_PM
Function: HSTL 1.8V Class 2 Test CIO

Description:

Noninverting bidirectional driver/receiver. Off-chip termination requires 25 ohms to $V_{ddq}/2$, where $V_{ddq} = V_{dd}$. Receiver requires (off-chip) input reference ($V_{ddq}/2$).

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
LT	DC current gate (I_{dd} test) input
RG	Receiver gate control
VREF	Voltage reference input
PAD	Driver output/receiver input
ZDI	Driver inhibit output (DI out)
Z	Receiver output



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	0	-	Hi-Z ¹	DI
-	-	0	Hi-Z ¹	DI
-	1	1	A	DI

¹. PAD is Hi-Z if driver is not externally terminated. PAD is at " $V_{ddq}/2$ " if driver is terminated (off-chip).

Notes:

- Logical "1" = $V_{ddq} = V_{dd} = 1.8V$.
- Timing model will be based on driver terminated off-chip.



Receiver Truth Table

Inputs				Output	Comments
PAD	LT	RG	VREF	Z	
-	-	0	-	0	Test mode
-	-	-	-	0	Test mode
1 ¹	0	1	-	1	Functional mode
0 ²	0	1	-	0	Functional mode
1 ³	1	1	-	1	Bypass mode
0 ⁴	1	1	-	0	Bypass mode

1. PAD input requires HSTL level "high" and $V_{ddq} < V_{dd}$.

2. PAD input requires HSTL level "low."

3. PAD input requires CMOS level "high" and $V_{ddq} = V_{dd}$.

4. PAD input requires CMOS level "low."

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$0.571 + 0.013D_{std}$	$0.466 + 0.011D_{std}$	$0.373 + 0.009D_{std}$
		t_{PHL}	$0.627 + 0.013D_{std}$	$0.462 + 0.010D_{std}$	$0.349 + 0.008D_{std}$
	B	t_{PLH}	$0.524 + 0.011D_{std}$	$0.420 + 0.009D_{std}$	$0.339 + 0.008D_{std}$
		t_{PHL}	$0.505 + 0.012D_{std}$	$0.389 + 0.009D_{std}$	$0.309 + 0.008D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.397 + 0.001N_{std}$	$0.266 + 0.001N_{std}$	$0.192 + 0.000N_{std}$
		t_{PHL}	$0.413 + 0.001N_{std}$	$0.266 + 0.001N_{std}$	$0.174 + 0.000N_{std}$
	B	t_{PLH}	$0.393 + 0.001N_{std}$	$0.267 + 0.001N_{std}$	$0.196 + 0.000N_{std}$
		t_{PHL}	$0.404 + 0.001N_{std}$	$0.265 + 0.001N_{std}$	$0.176 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

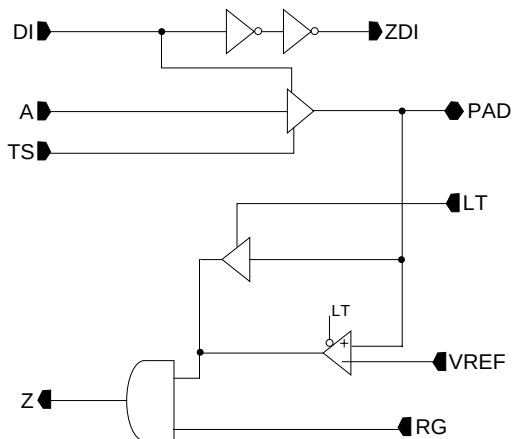
Input Pins	Performance Level	
	A	B
A	19.148	21.023
DI	3.545	3.549
LT	3.093	3.120
PAD (Receiver Input)	399.833	399.875
RG	6.693	6.693
TS	2.975	2.974
VREF	109.358	109.358
Internal	226.908	246.583
Cell Units	1 cell	1 cell

Cell: BHSTLC1T, BHSTLC1T_PM
Function: HSTL 1.5V Class 1 Test CIO

Description:

Noninverting bidirectional driver/receiver.
Off-chip termination requires 50 ohms to $V_{ddq}/2$, where $V_{ddq} = 1.5$. Receiver requires (off-chip) input reference ($V_{ddq}/2$).

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
LT DC current gate (I_{dd} test) input
RG Receiver gate control
VREF Voltage reference input
PAD Driver output/receiver input
ZDI Driver inhibit output (DI out)
Z Receiver output



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	0	-	Hi-Z ¹	DI
-	-	0	Hi-Z ¹	DI
-	1	1	A	DI

¹. PAD is Hi-Z if driver is not externally terminated. PAD is at " $V_{ddq}/2$ " if driver is terminated (off-chip).

Notes:

- Logical "1" = $V_{ddq} = 1.5V$.
- Timing model will be based on driver terminated off-chip.

Receiver Truth Table

Inputs				Output	Comments
PAD	LT	RG	VREF	Z	
-	-	0	-	0	Test mode
-	-	-	-	0	Test mode
1 ¹	0	1	-	1	Functional mode
0 ²	0	1	-	0	Functional mode
1 ³	1	1	-	1	Bypass mode
0 ⁴	1	1	-	0	Bypass mode

1. PAD input requires HSTL level "high" and $V_{ddq} < V_{dd}$.
2. PAD input requires HSTL level "low."
3. PAD input requires CMOS level "high" and $V_{ddq} = V_{dd}$.
4. PAD input requires CMOS level "low."

Note: A VREF signal of 0.75V must be applied through the VHSTLR1_A and VHSTLR2_A cells.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd150} = 1.4V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd150} = 1.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd150} = 1.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$0.533 + 0.019D_{std}$	$0.430 + 0.016D_{std}$	$0.345 + 0.014D_{std}$
		t_{PHL}	$0.496 + 0.019D_{std}$	$0.382 + 0.015D_{std}$	$0.299 + 0.013D_{std}$
	B	t_{PLH}	$0.446 + 0.018D_{std}$	$0.359 + 0.015D_{std}$	$0.295 + 0.013D_{std}$
		t_{PHL}	$0.410 + 0.018D_{std}$	$0.321 + 0.015D_{std}$	$0.261 + 0.013D_{std}$



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.411 + 0.001N _{std}	0.269 + 0.001N _{std}	0.173 + 0.000N _{std}
		t _{PHL}	0.504 + 0.001N _{std}	0.326 + 0.001N _{std}	0.227 + 0.000N _{std}
	B	t _{PLH}	0.412 + 0.001N _{std}	0.269 + 0.001N _{std}	0.171 + 0.000N _{std}
		t _{PHL}	0.501 + 0.001N _{std}	0.333 + 0.001N _{std}	0.234 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	29.783	29.333
DI	3.731	3.731
LT	3.227	3.227
PAD (Receiver Input)	371.167	371.167
RG	7.076	7.075
TS	3.109	3.109
VREF	112.575	112.575
Internal	440.000	436.000
Cell Units	1 cell	1 cell

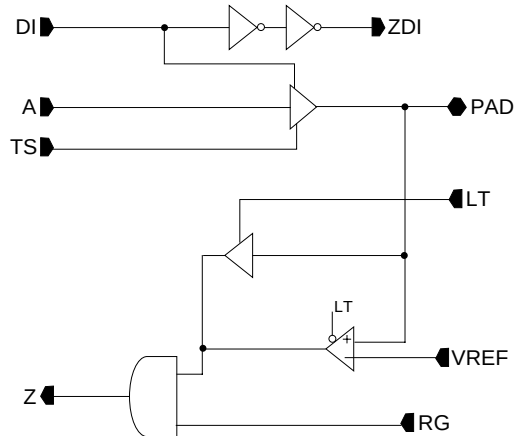
Cell: BHSTLC2T, BHSTLC2T_PM

Function: HSTL 1.5V Class 2 Test CIO

Description:

Noninverting bidirectional driver/receiver.
Off-chip termination requires 25 ohms to $V_{ddq}/2$, where $V_{ddq} = 1.5$. Receiver requires (off-chip) input reference ($V_{ddq}/2$).

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
LT DC current gate (I_{dd} test) input
RG Receiver gate control
VREF Voltage reference input
PAD Driver output/receiver input
ZDI Driver inhibit output (DI out)
Z Receiver output



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	0	-	Hi-Z ¹	DI
-	-	0	Hi-Z ¹	DI
-	1	1	A	DI

¹. PAD is Hi-Z if driver is not externally terminated. PAD is at " $V_{ddq}/2$ " if driver is terminated (off-chip).

Notes:

- Logical "1" = $V_{ddq} = 1.5V$.
- Timing model will be based on driver terminated off-chip.



Receiver Truth Table

Inputs				Output	Comments
PAD	LT	RG	VREF	Z	
-	-	0	-	0	Test mode
-	-	-	-	0	Test mode
1 ¹	0	1	-	1	Functional mode
0 ²	0	1	-	0	Functional mode
1 ³	1	1	-	1	Bypass mode
0 ⁴	1	1	-	0	Bypass mode

1. PAD input requires HSTL level "high" and $V_{ddq} < V_{dd}$.

2. PAD input requires HSTL level "low."

3. PAD input requires CMOS level "high" and $V_{ddq} = V_{dd}$.

4. PAD input requires CMOS level "low."

Note: A VREF signal of 0.75V must be applied through the VHSTLR1_A and VHSTLR2_A cells.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd150} = 1.4V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd150} = 1.5V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd150} = 1.6V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$1.223 + 0.014D_{std}$	$0.841 + 0.013D_{std}$	$0.645 + 0.011D_{std}$
		t_{PHL}	$1.026 + 0.011D_{std}$	$0.706 + 0.008D_{std}$	$0.511 + 0.007D_{std}$
	B	t_{PLH}	$1.006 + 0.011D_{std}$	$0.702 + 0.010D_{std}$	$0.539 + 0.009D_{std}$
		t_{PHL}	$0.902 + 0.010D_{std}$	$0.632 + 0.008D_{std}$	$0.472 + 0.007D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.411 + 0.001N_{std}$	$0.269 + 0.001N_{std}$	$0.173 + 0.000N_{std}$
		t_{PHL}	$0.504 + 0.001N_{std}$	$0.326 + 0.001N_{std}$	$0.227 + 0.000N_{std}$
	B	t_{PLH}	$0.412 + 0.001N_{std}$	$0.269 + 0.001N_{std}$	$0.171 + 0.000N_{std}$
		t_{PHL}	$0.502 + 0.001N_{std}$	$0.333 + 0.001N_{std}$	$0.234 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.221	13.721
DI	3.740	3.739
LT	3.229	3.229
PAD (Receiver Input)	416.042	416.042
RG	7.055	7.075
TS	3.120	3.118
VREF	112.583	112.583
Internal	676.704	687.114
Cell Units	1 cell	1 cell

Cell: BP2520T, BP2520T_PM

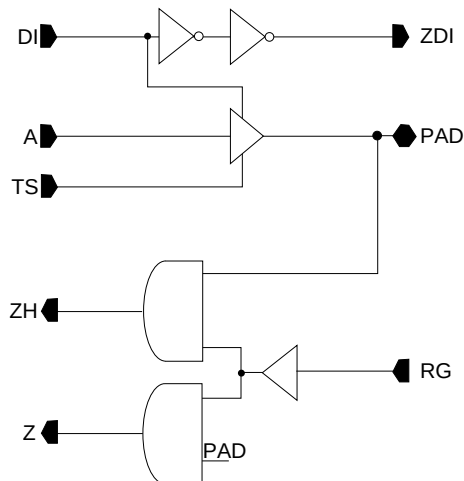
Function: 2.5V (3.3V Tolerant) CMOS Test 20 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses and is tolerant of 3.3V LVTTTL levels. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.519 + 0.021D _{std}	1.044 + 0.015D _{std}	0.756 + 0.012D _{std}
		t _{PHL}	1.560 + 0.026D _{std}	1.115 + 0.018D _{std}	0.835 + 0.014D _{std}
	B	t _{PLH}	1.308 + 0.019D _{std}	0.867 + 0.014D _{std}	0.627 + 0.010D _{std}
		t _{PHL}	1.260 + 0.023D _{std}	0.861 + 0.015D _{std}	0.630 + 0.012D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{Std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.427 + 0.002N _{Std}	0.289 + 0.001N _{Std}	0.215 + 0.001N _{Std}
		t _{PHL}	0.397 + 0.002N _{Std}	0.310 + 0.001N _{Std}	0.246 + 0.001N _{Std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{Std}	0.434 + 0.001N _{Std}	0.345 + 0.001N _{Std}
		t _{PHL}	0.557 + 0.002N _{Std}	0.457 + 0.001N _{Std}	0.376 + 0.001N _{Std}
PAD-Z	B	t _{PLH}	0.427 + 0.002N _{Std}	0.289 + 0.001N _{Std}	0.215 + 0.001N _{Std}
		t _{PHL}	0.397 + 0.002N _{Std}	0.310 + 0.001N _{Std}	0.246 + 0.001N _{Std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{Std}	0.434 + 0.001N _{Std}	0.345 + 0.001N _{Std}
		t _{PHL}	0.557 + 0.002N _{Std}	0.457 + 0.001N _{Std}	0.376 + 0.001N _{Std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	10.626	10.536
DI	7.166	7.180
PAD (Receiver Input)	536.083	536.083
RG	2.001	2.001
TS	6.174	6.172
Internal	495.617	492.604
Cell Units	1 cell	1 cell

Cell: BP2535T, BP2535T_PM

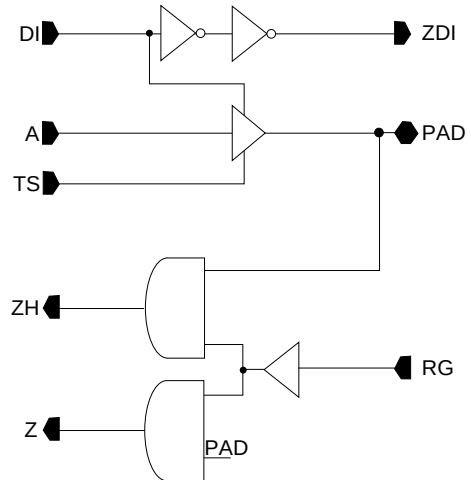
Function: 2.5V (3.3V Tolerant) CMOS Test 35 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses and is tolerant of 3.3V LVTTTL levels. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.491 + 0.030D _{std}	1.029 + 0.022D _{std}	0.745 + 0.018D _{std}
		t _{PHL}	1.530 + 0.033D _{std}	1.096 + 0.024D _{std}	0.822 + 0.019D _{std}
	B	t _{PLH}	1.273 + 0.028D _{std}	0.865 + 0.021D _{std}	0.644 + 0.017D _{std}
		t _{PHL}	1.223 + 0.031D _{std}	0.859 + 0.022D _{std}	0.646 + 0.018D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.436 + 0.002N _{std}	0.307 + 0.001N _{std}	0.237 + 0.001N _{std}
		t _{PHL}	0.388 + 0.002N _{std}	0.299 + 0.001N _{std}	0.237 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.620 + 0.002N _{std}	0.449 + 0.001N _{std}	0.363 + 0.001N _{std}
		t _{PHL}	0.547 + 0.002N _{std}	0.442 + 0.001N _{std}	0.362 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.440 + 0.002N _{std}	0.306 + 0.001N _{std}	0.234 + 0.001N _{std}
		t _{PHL}	0.393 + 0.002N _{std}	0.297 + 0.001N _{std}	0.230 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.626 + 0.002N _{std}	0.451 + 0.001N _{std}	0.364 + 0.001N _{std}
		t _{PHL}	0.554 + 0.002N _{std}	0.446 + 0.001N _{std}	0.362 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	10.590	10.485
DI	7.167	7.187
PAD (Receiver Input)	491.583	491.583
RG	2.001	2.001
TS	6.174	6.172
Internal	631.717	627.852
Cell Units	1 cell	1 cell

Cell: BP2550T, BP2550T_PM

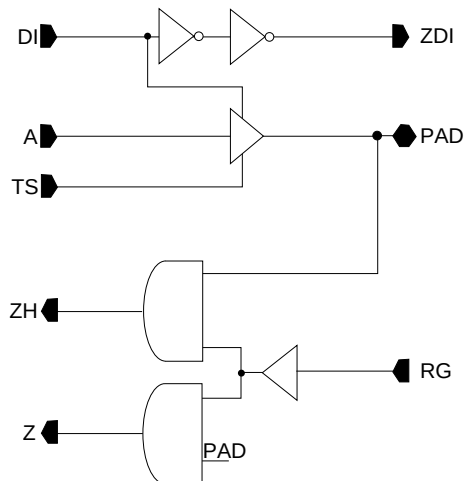
Function: 2.5V (3.3V Tolerant) CMOS Test 50 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses and is tolerant of 3.3V LVTTTL levels. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.457 + 0.040D _{std}	1.014 + 0.030D _{std}	0.737 + 0.025D _{std}
		t _{PHL}	1.495 + 0.043D _{std}	1.069 + 0.031D _{std}	0.804 + 0.026D _{std}
	B	t _{PLH}	1.233 + 0.039D _{std}	0.862 + 0.030D _{std}	0.658 + 0.025D _{std}
		t _{PHL}	1.177 + 0.041D _{std}	0.843 + 0.030D _{std}	0.652 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.292 + 0.001N _{std}	0.221 + 0.001N _{std}
		t _{PHL}	0.393 + 0.002N _{std}	0.310 + 0.001N _{std}	0.250 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.433 + 0.001N _{std}	0.346 + 0.001N _{std}
		t _{PHL}	0.550 + 0.002N _{std}	0.452 + 0.001N _{std}	0.374 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.428 + 0.002N _{std}	0.289 + 0.001N _{std}	0.216 + 0.001N _{std}
		t _{PHL}	0.397 + 0.002N _{std}	0.310 + 0.001N _{std}	0.246 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.435 + 0.001N _{std}	0.345 + 0.001N _{std}
		t _{PHL}	0.557 + 0.002N _{std}	0.457 + 0.001N _{std}	0.376 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	10.627	10.544
DI	7.171	7.155
PAD (Receiver Input)	462.042	462.042
RG	2.001	2.001
TS	6.174	6.172
Internal	757.553	755.480
Cell Units	1 cell	1 cell

Cell: BP2565T, BP2565T_PM

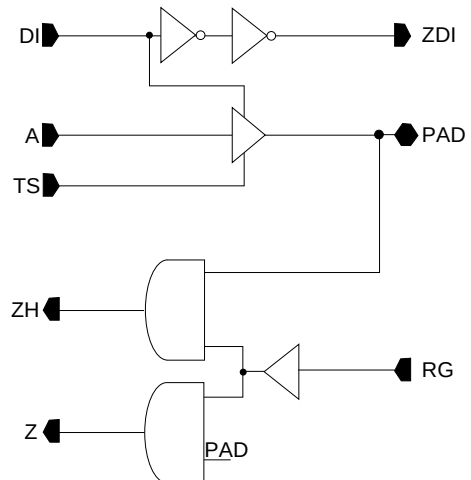
Function: 2.5V (3.3V Tolerant) CMOS Test 65 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses and is tolerant of 3.3V LVTTTL levels. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.437 + 0.052D _{std}	1.000 + 0.040D _{std}	0.733 + 0.034D _{std}
		t _{PHL}	1.449 + 0.054D _{std}	1.048 + 0.041D _{std}	0.792 + 0.034D _{std}
	B	t _{PLH}	1.197 + 0.052D _{std}	0.862 + 0.040D _{std}	0.667 + 0.034D _{std}
		t _{PHL}	1.139 + 0.053D _{std}	0.844 + 0.040D _{std}	0.663 + 0.034D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.427 + 0.002N _{std}	0.292 + 0.001N _{std}	0.221 + 0.001N _{std}
		t _{PHL}	0.393 + 0.002N _{std}	0.310 + 0.001N _{std}	0.250 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{std}	0.433 + 0.001N _{std}	0.346 + 0.001N _{std}
		t _{PHL}	0.550 + 0.002N _{std}	0.452 + 0.001N _{std}	0.374 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.428 + 0.002N _{std}	0.289 + 0.001N _{std}	0.216 + 0.001N _{std}
		t _{PHL}	0.397 + 0.002N _{std}	0.310 + 0.001N _{std}	0.246 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{std}	0.435 + 0.001N _{std}	0.345 + 0.001N _{std}
		t _{PHL}	0.557 + 0.002N _{std}	0.457 + 0.001N _{std}	0.376 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	10.626	10.544
DI	7.168	7.154
PAD (Receiver Input)	450.708	450.708
RG	2.001	2.001
TS	6.174	6.172
Internal	870.873	869.199
Cell Units	1 cell	1 cell

Cell: BP2590T, BP2590T_PM

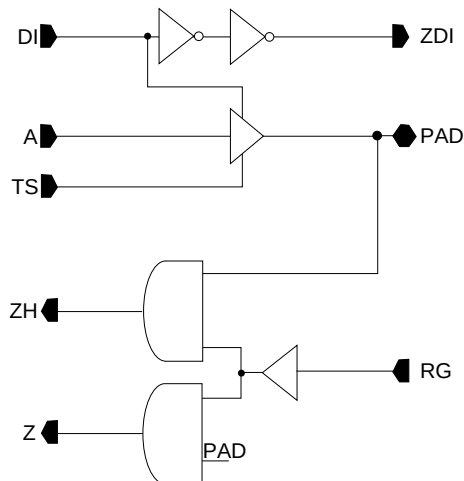
Function: 2.5V (3.3V Tolerant) CMOS Test 90 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V CMOS off-chip bidirectional data buses and is tolerant of 3.3V LVTTTL levels. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.128 + 0.075D _{std}	0.768 + 0.057D _{std}	0.562 + 0.048D _{std}
		t _{PHL}	1.174 + 0.076D _{std}	0.852 + 0.056D _{std}	0.638 + 0.046D _{std}
	B	t _{PLH}	1.065 + 0.075D _{std}	0.759 + 0.057D _{std}	0.610 + 0.048D _{std}
		t _{PHL}	1.182 + 0.075D _{std}	0.915 + 0.054D _{std}	0.733 + 0.046D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{Std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{Std}	0.291 + 0.001N _{Std}	0.220 + 0.001N _{Std}
		t _{PHL}	0.392 + 0.002N _{Std}	0.310 + 0.001N _{Std}	0.251 + 0.001N _{Std}
PAD-ZH		t _{PLH}	0.610 + 0.002N _{Std}	0.432 + 0.001N _{Std}	0.345 + 0.001N _{Std}
		t _{PHL}	0.548 + 0.002N _{Std}	0.451 + 0.001N _{Std}	0.373 + 0.001N _{Std}
PAD-Z	B	t _{PLH}	0.431 + 0.002N _{Std}	0.288 + 0.001N _{Std}	0.215 + 0.001N _{Std}
		t _{PHL}	0.396 + 0.002N _{Std}	0.309 + 0.001N _{Std}	0.245 + 0.001N _{Std}
PAD-ZH		t _{PLH}	0.619 + 0.002N _{Std}	0.434 + 0.001N _{Std}	0.344 + 0.001N _{Std}
		t _{PHL}	0.556 + 0.002N _{Std}	0.456 + 0.001N _{Std}	0.376 + 0.001N _{Std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	10.686	10.687
DI	7.151	7.175
PAD (Receiver Input)	326.625	326.625
RG	2.002	2.002
TS	6.180	6.180
Internal	868.000	875.000
Cell Units	1 cell	1 cell

Cell: BP3320T, BP3320T_PM

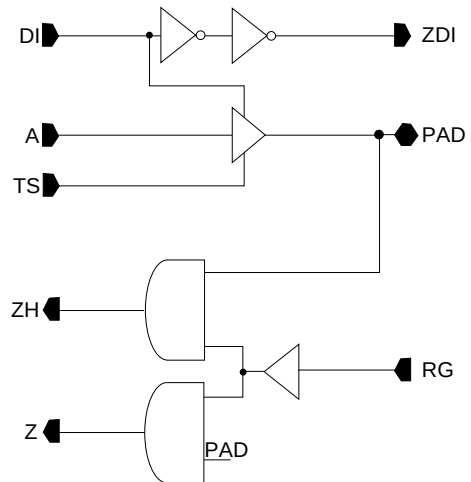
Function: 3.3V LVTTTL (5V Protected) Test 20 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Receiver is 5.0V tolerant. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
RG Receiver gate control
PAD Driver output/receiver input
ZH Hysteresis receiver output
Z Non-hysteresis receiver output
ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.769 + 0.023D _{std}	1.252 + 0.016D _{std}	0.949 + 0.013D _{std}
		t _{PHL}	1.615 + 0.023D _{std}	1.136 + 0.015D _{std}	0.872 + 0.012D _{std}
	B	t _{PLH}	1.588 + 0.022D _{std}	1.092 + 0.016D _{std}	0.823 + 0.013D _{std}
		t _{PHL}	1.424 + 0.022D _{std}	0.974 + 0.014D _{std}	0.736 + 0.011D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.431 + 0.002N _{std}	0.235 + 0.001N _{std}	0.135 + 0.001N _{std}
		t _{PHL}	0.643 + 0.001N _{std}	0.538 + 0.001N _{std}	0.472 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.624 + 0.002N _{std}	0.360 + 0.001N _{std}	0.238 + 0.001N _{std}
		t _{PHL}	0.724 + 0.001N _{std}	0.613 + 0.001N _{std}	0.535 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.420 + 0.002N _{std}	0.227 + 0.001N _{std}	0.128 + 0.001N _{std}
		t _{PHL}	0.630 + 0.001N _{std}	0.529 + 0.001N _{std}	0.464 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.351 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PHL}	0.711 + 0.001N _{std}	0.603 + 0.001N _{std}	0.527 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	12.245	12.245
DI	5.736	5.737
PAD (Receiver Input)	533.625	544.917
RG	2.096	2.096
TS	4.418	4.418
Internal	169.000	166.000
Cell Units	1 cell	1 cell

Cell: BP3335T, BP3335T_PM

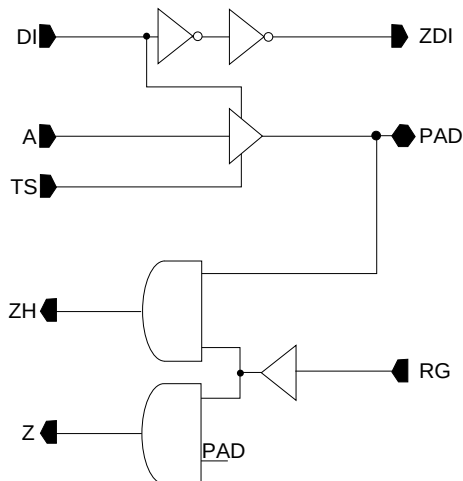
Function: 3.3V LVTTTL (5V Protected) Test 35 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Receiver is 5.0V tolerant. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.650 + 0.031D _{std}	1.155 + 0.023D _{std}	0.863 + 0.019D _{std}
		t _{PHL}	1.513 + 0.031D _{std}	1.053 + 0.022D _{std}	0.800 + 0.018D _{std}
	B	t _{PLH}	1.482 + 0.029D _{std}	1.033 + 0.022D _{std}	0.788 + 0.018D _{std}
		t _{PHL}	1.354 + 0.029D _{std}	0.938 + 0.021D _{std}	0.718 + 0.017D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.246 + 0.001N _{std}	0.152 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.641 + 0.001N _{std}	0.529 + 0.001N _{std}	0.464 + 0.000N _{std}
		t _{PLH}	0.621 + 0.002N _{std}	0.364 + 0.001N _{std}	0.246 + 0.001N _{std}
		t _{PHL}	0.722 + 0.001N _{std}	0.602 + 0.001N _{std}	0.525 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.420 + 0.002N _{std}	0.227 + 0.001N _{std}	0.128 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.630 + 0.001N _{std}	0.529 + 0.001N _{std}	0.464 + 0.000N _{std}
		t _{PLH}	0.613 + 0.002N _{std}	0.351 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PHL}	0.711 + 0.001N _{std}	0.603 + 0.001N _{std}	0.527 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	12.260	12.263
DI	5.740	5.740
PAD (Receiver Input)	533.625	544.917
RG	2.096	2.096
TS	4.511	4.511
Internal	221.000	219.000
Cell Units	1 cell	1 cell



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.549 + 0.041D _{std}	1.096 + 0.031D _{std}	0.824 + 0.026D _{std}
		t _{PHL}	1.427 + 0.042D _{std}	0.985 + 0.030D _{std}	0.744 + 0.025D _{std}
	B	t _{PLH}	1.348 + 0.040D _{std}	0.962 + 0.030D _{std}	0.750 + 0.025D _{std}
		t _{PHL}	1.203 + 0.040D _{std}	0.836 + 0.029D _{std}	0.650 + 0.024D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.246 + 0.001N _{std}	0.152 + 0.001N _{std}
		t _{PHL}	0.641 + 0.001N _{std}	0.529 + 0.001N _{std}	0.464 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.621 + 0.002N _{std}	0.364 + 0.001N _{std}	0.246 + 0.001N _{std}
		t _{PHL}	0.722 + 0.001N _{std}	0.602 + 0.001N _{std}	0.525 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.420 + 0.002N _{std}	0.227 + 0.001N _{std}	0.128 + 0.001N _{std}
		t _{PHL}	0.630 + 0.001N _{std}	0.529 + 0.001N _{std}	0.464 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.351 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PHL}	0.711 + 0.001N _{std}	0.603 + 0.001N _{std}	0.527 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	12.279	12.279
DI	5.740	5.738
PAD (Receiver Input)	533.625	544.917
RG	2.096	2.096
TS	4.511	4.511
Internal	283.000	282.000
Cell Units	1 cell	1 cell

Cell: BP3365T, BP3365T_PM

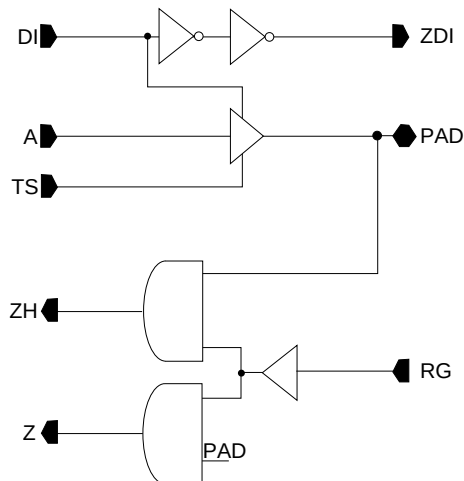
Function: 3.3V LVTTTL (5V Protected) Test 65 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Receiver is 5.0V tolerant. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.425 + 0.054D _{std}	1.017 + 0.041D _{std}	0.770 + 0.034D _{std}
		t _{PHL}	1.300 + 0.054D _{std}	0.902 + 0.039D _{std}	0.684 + 0.033D _{std}
	B	t _{PLH}	1.207 + 0.052D _{std}	0.881 + 0.039D _{std}	0.700 + 0.033D _{std}
		t _{PHL}	1.095 + 0.053D _{std}	0.783 + 0.038D _{std}	0.619 + 0.032D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.246 + 0.001N _{std}	0.152 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.641 + 0.001N _{std}	0.529 + 0.001N _{std}	0.464 + 0.000N _{std}
		t _{PLH}	0.621 + 0.002N _{std}	0.364 + 0.001N _{std}	0.246 + 0.001N _{std}
		t _{PHL}	0.722 + 0.001N _{std}	0.602 + 0.001N _{std}	0.525 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.420 + 0.002N _{std}	0.227 + 0.001N _{std}	0.128 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.630 + 0.001N _{std}	0.529 + 0.001N _{std}	0.464 + 0.000N _{std}
		t _{PLH}	0.613 + 0.002N _{std}	0.351 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PHL}	0.711 + 0.001N _{std}	0.603 + 0.001N _{std}	0.527 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	12.282	12.280
DI	5.737	5.738
PAD (Receiver Input)	533.625	544.917
RG	2.096	2.096
TS	4.511	4.511
Internal	347.000	347.000
Cell Units	1 cell	1 cell

Cell: BP3390T, BP3390T_PM

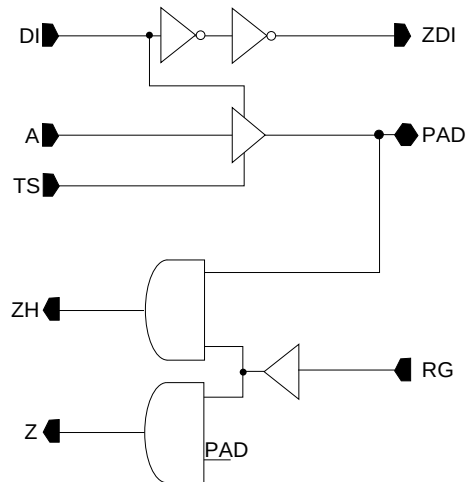
Function: 3.3V LVTTL (5V Protected) Test 90 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTL off-chip bidirectional data buses. Receiver is 5.0V tolerant. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.250 + 0.075D _{std}	0.899 + 0.057D _{std}	0.683 + 0.048D _{std}
		t _{PHL}	1.164 + 0.072D _{std}	0.809 + 0.053D _{std}	0.612 + 0.045D _{std}
	B	t _{PLH}	1.027 + 0.074D _{std}	0.775 + 0.056D _{std}	0.635 + 0.047D _{std}
		t _{PHL}	1.027 + 0.071D _{std}	0.767 + 0.052D _{std}	0.626 + 0.044D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.426 + 0.002N _{std}	0.246 + 0.001N _{std}	0.152 + 0.001N _{std}
		t _{PHL}	0.641 + 0.001N _{std}	0.529 + 0.001N _{std}	0.464 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.621 + 0.002N _{std}	0.364 + 0.001N _{std}	0.246 + 0.001N _{std}
		t _{PHL}	0.722 + 0.001N _{std}	0.602 + 0.001N _{std}	0.525 + 0.000N _{std}
PAD-Z	B	t _{PLH}	0.420 + 0.002N _{std}	0.227 + 0.001N _{std}	0.128 + 0.001N _{std}
		t _{PHL}	0.630 + 0.001N _{std}	0.529 + 0.001N _{std}	0.464 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.613 + 0.002N _{std}	0.351 + 0.001N _{std}	0.230 + 0.001N _{std}
		t _{PHL}	0.711 + 0.001N _{std}	0.603 + 0.001N _{std}	0.527 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	12.279	12.280
DI	5.740	5.740
PAD (Receiver Input)	533.625	544.917
RG	2.096	2.096
TS	4.511	4.511
Internal	868.000	875.000
Cell Units	1 cell	1 cell

Cell: BPCIX3T, BPCIX3T_PM

Function: 3.3V PCI-X/PCI Test 3-State CIO

Description:

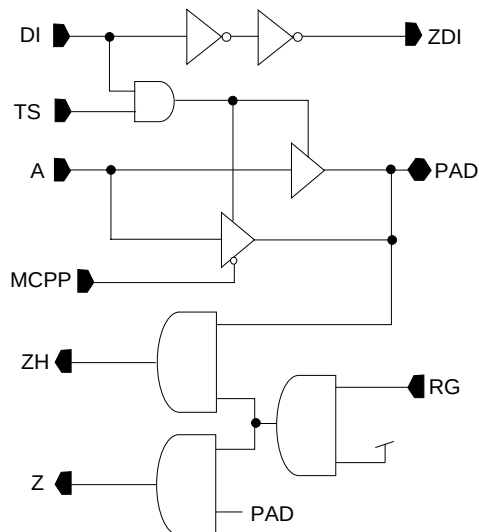
A noninverting three-state test driver/receiver that interfaces 1.8V internal functions with 3.3V PCI-X or PCI off-chip bidirectional data buses. Both non-hysteresis, and hysteresis receiver outputs are provided. The hysteresis output path will have improved noise immunity, but a slightly slower propagation delay. A mode control (MCP) provides a 40 ohm driver impedance for point-to-point applications and a 20 ohm impedance for multi-point applications. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

Refer to the IBM application note *ASIC I/O Test Considerations* for required MCP pin test connections. The application note is available from your IBM representative or at the following URL:

<http://www.chips.ibm.com/techlib/products/asics/appnotes.html>

A	Driver data input
TS	Driver three-state control
DI	Driver inhibit input (DI in)
RG	Receiver gate control
PAD	Driver output/receiver input
Z	Non-hysteresis receiver output
ZH	Noninverting receiver output with hysteresis
ZDI	Driver inhibit output (DI out)
MCP	Driver mode control

Pin Group: (Z,ZH): (0,2)



Driver Mode Control Table

MCP	Driver Mode of Operation
0	Multi-point mode
1	Point-to-point mode

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
-	1	PAD	PAD
Hi-Z	1	X	X

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Driver Propagation Delays (Point-to-Point Mode)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.628 + 0.022D _{std}	1.030 + 0.015D _{std}	0.765 + 0.011D _{std}
		t _{PHL}	1.690 + 0.023D _{std}	1.137 + 0.015D _{std}	0.847 + 0.012D _{std}

Receiver Propagation Delays (Point-to-Point Mode)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.749 + 0.002N _{std}	0.554 + 0.001N _{std}	0.455 + 0.001N _{std}
		t _{PHL}	0.320 + 0.001N _{std}	0.248 + 0.000N _{std}	0.191 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.790 + 0.002N _{std}	0.568 + 0.001N _{std}	0.461 + 0.001N _{std}
		t _{PHL}	0.467 + 0.000N _{std}	0.389 + 0.000N _{std}	0.329 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	19.485
DI	12.138
MCP	3.030
PAD (Receiver Input)	679.917
RG	2.264
TS	12.518
Internal	294.874
Cell Units	1 cell

Cell: BPCIX3PUT, BPCIX3PUT_PM

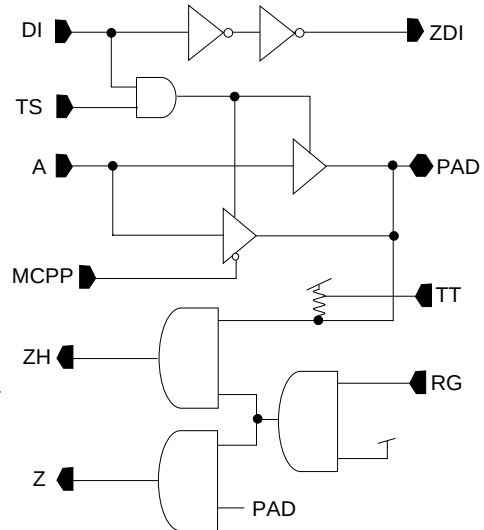
Function: 3.3V PCI-X/PCI Test 3-State CIO w/Pull-Up

Description:

A noninverting three-state test driver/receiver that interfaces 1.8V internal functions with 3.3V PCI-X or PCI off-chip bidirectional data buses. Both non-hysteresis and hysteresis receiver outputs are provided. The hysteresis output path will have improved noise immunity, but a slightly slower propagation delay. A mode control (MCP) provides a 40 ohm driver impedance for point-to-point applications and a 20 ohm impedance for multi-point applications. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} . PAD is pulled up to logic "1" (3.3V) through 14k ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test.

Refer to the IBM application note *ASIC I/O Test Considerations* for required MCP pin test connections. The application note is available from your IBM representative or at the following URL:

<http://www.chips.ibm.com/techlib/products/asics/apnotes.html>



A	Driver data input
TS	Driver three-state control
TT	Pull-Up Resistor enable
DI	Driver inhibit input (DI in)
RG	Receiver gate control
PAD	Driver output/receiver input
Z	Non-hysteresis receiver output
ZH	Noninverting receiver output with hysteresis
ZDI	Driver inhibit output (DI out)
MCP	Driver mode control

Pin Group: (Z,ZH): (0,2)



Driver Mode Control Table

MCPP	Driver Mode of Operation
0	Multi-point mode
1	Point-to-point mode

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
-	1	PAD	PAD
Hi-Z	1	X	X

Driver Propagation Delays (Point-to-Point Mode)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.628 + 0.022D_{std}$	$1.031 + 0.015D_{std}$	$0.765 + 0.011D_{std}$
		t_{PHL}	$1.691 + 0.023D_{std}$	$1.137 + 0.015D_{std}$	$0.847 + 0.012D_{std}$

Receiver Propagation Delays (Point-to-Point Mode)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.745 + 0.002N _{std}	0.549 + 0.001N _{std}	0.450 + 0.001N _{std}
		t _{PHL}	0.325 + 0.001N _{std}	0.254 + 0.000N _{std}	0.198 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.787 + 0.002N _{std}	0.563 + 0.001N _{std}	0.457 + 0.001N _{std}
		t _{PHL}	0.472 + 0.000N _{std}	0.395 + 0.000N _{std}	0.336 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	19.513
DI	12.139
MCPD	3.030
PAD (Receiver Input)	675.000
RG	2.264
TS	12.522
TT	7.313
Internal	294.922
Cell Units	1 cell

Cell: BPCI5T, BPCI5T_PM

Function: 3.3V/5.0V Tolerant, PCI Test 3-State CIO

Description:

A noninverting three-state test driver/receiver that interfaces 1.8V internal functions with 5V PCI off-chip bidirectional data buses. Both non-hysteresis, and hysteresis receiver outputs are provided. The hysteresis output path will have improved noise immunity, but slightly increased delay performance. A, TS, Z, and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

A Driver data input

TS Driver three-state control

DI Driver inhibit input (DI in)

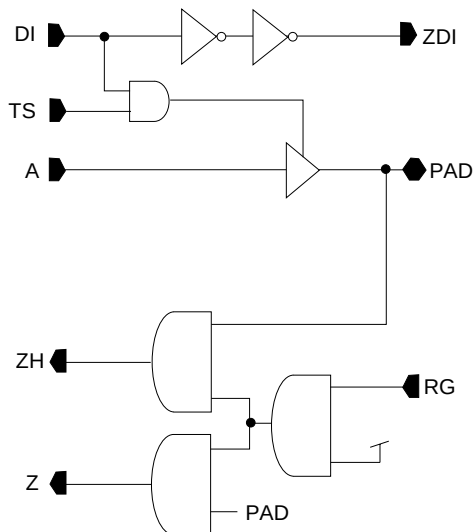
RG Receiver gate control

PAD Driver output/receiver input

Z Non-hysteresis receiver output

ZH Noninverting receiver output with hysteresis

ZDI Driver inhibit output (DI out)



Pin Group: (Z,ZH): (0,2)

Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
-	1	PAD	PAD
Hi-Z	1	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$1.558 + 0.024D_{std}$	$0.982 + 0.017D_{std}$	$0.710 + 0.013D_{std}$
		t_{PHL}	$1.787 + 0.014D_{std}$	$1.183 + 0.009D_{std}$	$0.871 + 0.007D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^{\circ}C$ Process = Fast
PAD-Z	A	t_{PLH}	$1.073 + 0.003N_{std}$	$0.623 + 0.002N_{std}$	$0.429 + 0.001N_{std}$
		t_{PHL}	$0.571 + 0.001N_{std}$	$0.455 + 0.000N_{std}$	$0.378 + 0.000N_{std}$
PAD-ZH		t_{PLH}	$1.249 + 0.002N_{std}$	$0.657 + 0.001N_{std}$	$0.429 + 0.001N_{std}$
		t_{PHL}	$0.719 + 0.000N_{std}$	$0.593 + 0.000N_{std}$	$0.511 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	18.409
DI	6.853
PAD (Receiver Input)	634.667
RG	2.332
RI	3.480
TS	6.771
Internal	1450.000
Cell Units	1 cell

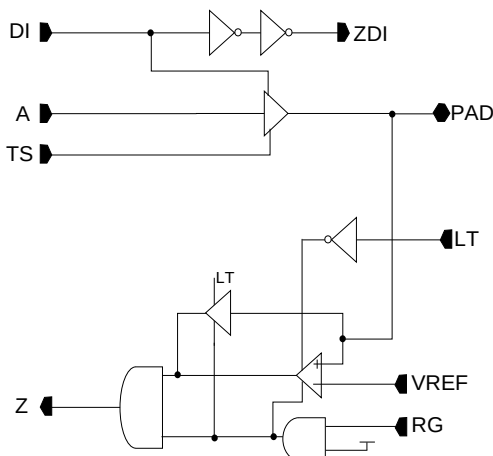
Cell: BSSTL2C1T, BSSTL2C1T_PM

Function: SSTL 2.5V Class 1 Test 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V SSTL2 Class 2 off-chip bidirectional data buses. Driver is designed to provide a minimum 7.6 mA sink/source current at SSTL levels. Input receiver requires reference voltage of $V_{dd250}/2$. A, TS, Z, LT and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- LT I_{ddq} leakage test control
- VREF Reference voltage input
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z ¹	DI
-	0	-	Hi-Z ¹	DI
-	1	1	A	DI

¹. PAD is Hi-Z if driver is not externally terminated. Pad is at V_{TT} ($V_{dd250}/2$) is driver is terminated off chip.

Note: Timing model will be based on driver terminated off-chip.

Receiver Truth Table

Inputs				Output	Comments
PAD	LT	RG	VREF	Z	
-	-	0	-	0	Receiver disabled (no DC current) - user control
0 ¹	1	1	-	0	Bypass test receiver enabled (no DC current)
1 ¹	1	1	-	1	Bypass test receiver enabled (no DC current)
Hi-Z ¹	1	1	-	X	Bypass test receiver enabled (no DC current)
0 ²	0	1	V _{dd250} /2	0	Functional receiver enabled
1 ²	0	1	V _{dd250} /2	1	Functional receiver enabled
Hi-Z ²	0	1	V _{dd250} /2	X	Functional receiver enabled

¹. PAD input requires 2.5V CMOS levels.

². PAD input requires 2.5V SSTL levels.

Note: LT, RG, and RI can all turn off turn off SSTL input differential amplifier DC bias current.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	0.759 + 0.025D _{std}	0.552 + 0.022D _{std}	0.421 + 0.020D _{std}
		t _{PHL}	0.709 + 0.026D _{std}	0.501 + 0.022D _{std}	0.367 + 0.019D _{std}
	B	t _{PLH}	0.727 + 0.024D _{std}	0.530 + 0.021D _{std}	0.404 + 0.019D _{std}
		t _{PHL}	0.667 + 0.026D _{std}	0.473 + 0.021D _{std}	0.348 + 0.019D _{std}



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	1.027 + 0.001N _{std}	0.641 + 0.001N _{std}	0.424 + 0.000N _{std}
		t _{PHL}	1.022 + 0.003N _{std}	0.634 + 0.001N _{std}	0.428 + 0.001N _{std}
	B	t _{PLH}	1.027 + 0.001N _{std}	0.641 + 0.001N _{std}	0.424 + 0.000N _{std}
		t _{PHL}	1.022 + 0.003N _{std}	0.634 + 0.001N _{std}	0.428 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	31.104	34.600
DI	4.845	4.861
LT	3.551	3.551
PAD (Receiver Input)	322.250	322.208
RG	5.568	5.564
TS	2.511	2.501
VREF	109.508	109.508
Internal	585.000	595.000
Cell Units	1 cell	1 cell

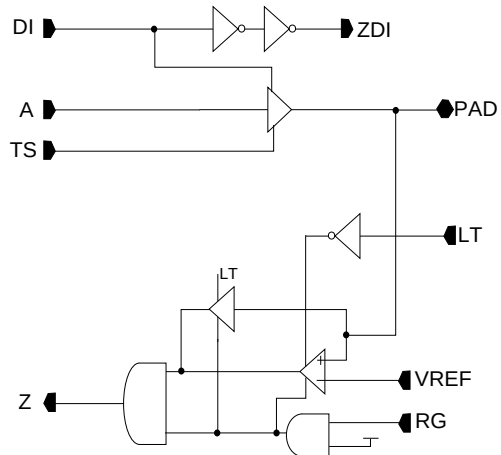
Cell: BSSTL2C2T, BSSTL2C2T_PM

Function: SSTL 2.5V Class 2 Test 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V SSTL2 Class 2 off-chip bidirectional data buses. Driver is designed to provide a minimum 15.2 mA sink/source current at SSTL levels. Input receiver requires reference voltage of $V_{dd250}/2$. A, TS, Z, LT and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- LT I_{ddq} leakage test control
- VREF Reference voltage input
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z ¹	DI
-	0	-	Hi-Z ¹	DI
-	1	1	A	DI

¹. PAD is Hi-Z if driver is not externally terminated. Pad is at V_{TT} ($V_{dd250}/2$) if driver is terminated off chip.

Note: Timing model will be based on driver terminated off-chip.

Receiver Truth Table

Inputs				Output	Comments
PAD	LT	RG	VREF	Z	
-	-	0	-	0	Receiver disabled (no DC current) - user control
0 ¹	1	1	-	0	Bypass test receiver enabled (no DC current)
1 ¹	1	1	-	1	Bypass test receiver enabled (no DC current)
Hi-Z ¹	1	1	-	X	Bypass test receiver enabled (no DC current)
0 ²	0	1	V _{dd250} /2	0	Functional receiver enabled
1 ²	0	1	V _{dd250} /2	1	Functional receiver enabled
Hi-Z ²	0	1	V _{dd250} /2	X	Functional receiver enabled

¹. PAD input requires 2.5V CMOS levels.

². PAD input requires 2.5V SSTL levels.

Note: LT, RG, and RI can all turn off turn off SSTL input differential amplifier DC bias current.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.033 + 0.015D _{std}	0.741 + 0.013D _{std}	0.559 + 0.011D _{std}
		t _{PHL}	1.029 + 0.017D _{std}	0.709 + 0.013D _{std}	0.515 + 0.011D _{std}
	B	t _{PLH}	0.791 + 0.013D _{std}	0.558 + 0.011D _{std}	0.419 + 0.010D _{std}
		t _{PHL}	0.746 + 0.014D _{std}	0.513 + 0.011D _{std}	0.374 + 0.010D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$1.027 + 0.001N_{std}$	$0.641 + 0.001N_{std}$	$0.424 + 0.000N_{std}$
		t_{PHL}	$1.022 + 0.003N_{std}$	$0.634 + 0.001N_{std}$	$0.428 + 0.001N_{std}$
	B	t_{PLH}	$1.027 + 0.001N_{std}$	$0.641 + 0.001N_{std}$	$0.424 + 0.000N_{std}$
		t_{PHL}	$1.022 + 0.003N_{std}$	$0.634 + 0.001N_{std}$	$0.428 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	34.588	34.625
DI	4.843	4.869
LT	3.551	3.551
PAD (Receiver Input)	478.250	478.375
RG	5.566	5.566
TS	2.527	2.526
VREF	109.508	109.517
Internal	786.000	810.000
Cell Units	1 cell	1 cell

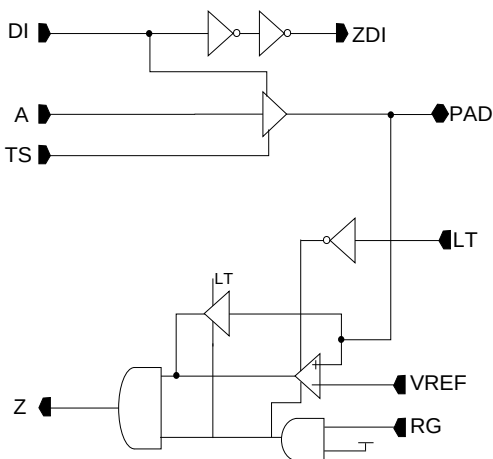
Cell: BSSTL2C50T, BSSTL2C50T_PM

Function: 2.5V SSTL Test 3-State CIO With Half-Strength Driver

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V SSTL2 off-chip bidirectional data buses. Driver is designed for use with transmission line impedances of 45 to 55 ohms. Input receiver requires reference voltage of $V_{dd250}/2$. A, TS, Z, LT and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- LT I_{ddq} leakage test control
- VREF Reference voltage Input
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z ¹	DI
-	0	-	Hi-Z ¹	DI
-	1	1	A	DI

¹. PAD is Hi-Z if driver is not externally terminated. Pad is at V_{TT} ($V_{dd250}/2$) if driver is terminated off chip.

Note: NDR will assume off-chip termination.

Receiver Truth Table

Inputs				Output	Comments
PAD	LT	RG	VREF	Z	
-	-	0	-	0	Receiver disabled (no DC current); user control
0 ¹	1	1	-	0	Bypass test receiver enabled (no DC current)
1 ¹	1	1	-	1	Bypass test receiver enabled (no DC current)
Hi-Z ¹	1	1	-	X	Bypass test receiver enabled (no DC current)
0 ²	0	1	V _{dd250} /2	0	Functional receiver enabled
1 ²	0	1	V _{dd250} /2	1	Functional receiver enabled
Hi-Z ²	0	1	V _{dd250} /2	X	Functional receiver enabled

¹. PAD input requires CMOS levels.

². PAD input requires SSTL level.

Note: LT, RG, and RI can all turn off turn off DC bias current of the SSTL input differential amplifier. VREF is supplied by voltage reference cells VSSTL2R1_A and VSSTL2R2_A.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.089 + 0.041D _{std}	0.776 + 0.031D _{std}	0.581 + 0.026D _{std}
		t _{PHL}	1.209 + 0.045D _{std}	0.807 + 0.032D _{std}	0.564 + 0.026D _{std}
	B	t _{PLH}	0.766 + 0.040D _{std}	0.544 + 0.030D _{std}	0.403 + 0.025D _{std}
		t _{PHL}	0.829 + 0.042D _{std}	0.567 + 0.031D _{std}	0.410 + 0.025D _{std}



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	1.027 + 0.001N _{std}	0.641 + 0.001N _{std}	0.424 + 0.000N _{std}
		t _{PHL}	1.022 + 0.003N _{std}	0.634 + 0.001N _{std}	0.428 + 0.001N _{std}
	B	t _{PLH}	1.027 + 0.001N _{std}	0.641 + 0.001N _{std}	0.424 + 0.000N _{std}
		t _{PHL}	1.022 + 0.003N _{std}	0.634 + 0.001N _{std}	0.428 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	37.758	37.875
DI	4.857	4.849
LT	3.603	3.603
PAD (Receiver Input)	423.833	424.000
RG	5.540	5.540
TS	2.536	2.521
VREF	116.017	115.883
Internal	1410.932	1491.361
Cell Units	1 cell	1 cell

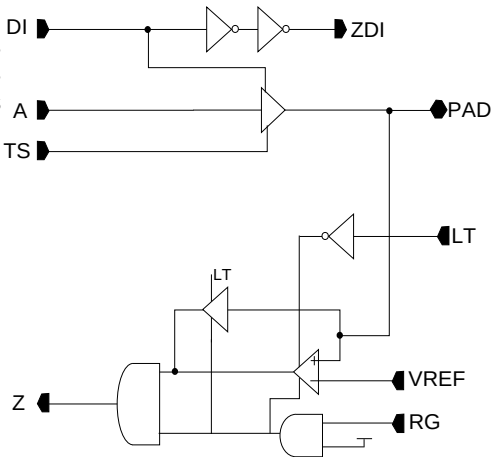
Cell: BSSTL2C56T, BSSTL2C56T_PM

Function: 2.5V SSTL Test 3-State CIO With Half-Strength Driver

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 2.5V SSTL2 off-chip bidirectional data buses. Driver is designed for use with transmission line impedances of 50 to 62 ohms. Input receiver requires reference voltage of $V_{dd250}/2$. A, TS, Z, LT and RG must have a boundary-scan structure. If RG is not used, it should be tied to V_{dd} .

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
RG Receiver gate control
PAD Driver output/receiver input
LT I_{ddq} leakage test control
VREF Reference voltage Input
Z Non-hysteresis receiver output
ZDI Driver inhibit output (DI out)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z ¹	DI
-	0	-	Hi-Z ¹	DI
-	1	1	A	DI

¹. PAD is Hi-Z if driver is not externally terminated. Pad is at V_{TT} ($V_{dd250}/2$) if driver is terminated off chip.

Note: NDR will assume off-chip termination.

Receiver Truth Table

Inputs				Output	Comments
PAD	LT	RG	VREF	Z	
-	-	0	-	0	Receiver disabled (no DC current); user control
0 ¹	1	1	-	0	Bypass test receiver enabled (no DC current)
1 ¹	1	1	-	1	Bypass test receiver enabled (no DC current)
Hi-Z ¹	1	1	-	X	Bypass test receiver enabled (no DC current)
0 ²	0	1	V _{dd250} /2	0	Functional receiver enabled
1 ²	0	1	V _{dd250} /2	1	Functional receiver enabled
Hi-Z ²	0	1	V _{dd250} /2	X	Functional receiver enabled

¹. PAD input requires CMOS levels.

². PAD input requires SSTL level.

Note: LT, RG, and RI can all turn off turn off DC bias current of the SSTL input differential amplifier. VREF is supplied by voltage reference cells VSSTL2R1_A and VSSTL2R2_A.

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.083 + 0.049D _{std}	0.775 + 0.037D _{std}	0.578 + 0.031D _{std}
		t _{PHL}	1.203 + 0.051D _{std}	0.809 + 0.038D _{std}	0.567 + 0.031D _{std}
	B	t _{PLH}	0.760 + 0.047D _{std}	0.544 + 0.036D _{std}	0.405 + 0.031D _{std}
		t _{PHL}	0.824 + 0.049D _{std}	0.566 + 0.036D _{std}	0.410 + 0.030D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^{\circ}C$ Process = Fast
PAD-Z	A	t_{PLH}	$1.027 + 0.001N_{std}$	$0.641 + 0.001N_{std}$	$0.424 + 0.000N_{std}$
		t_{PHL}	$1.022 + 0.003N_{std}$	$0.634 + 0.001N_{std}$	$0.428 + 0.001N_{std}$
	B	t_{PLH}	$1.027 + 0.001N_{std}$	$0.641 + 0.001N_{std}$	$0.424 + 0.000N_{std}$
		t_{PHL}	$1.022 + 0.003N_{std}$	$0.634 + 0.001N_{std}$	$0.428 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	37.758	37.875
DI	4.833	4.848
LT	3.603	3.603
PAD (Receiver Input)	415.917	416.125
RG	5.540	5.540
TS	2.536	2.533
VREF	116.017	116.017
Internal	1412.533	1493.104
Cell Units	1 cell	1 cell

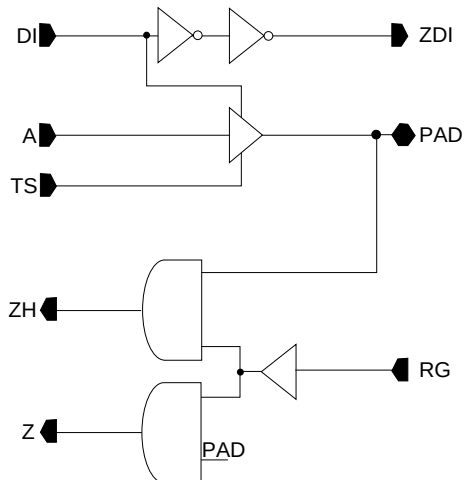
Cell: BT3320T, BT3320T_PM
Function: 3.3V LVTTTL Test 20 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
RG Receiver gate control
PAD Driver output/receiver input
ZH Hysteresis receiver output
Z Non-hysteresis receiver output
ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.644 + 0.024D _{std}	1.177 + 0.017D _{std}	0.889 + 0.014D _{std}
		t _{PHL}	1.485 + 0.024D _{std}	1.041 + 0.016D _{std}	0.788 + 0.013D _{std}
	B	t _{PLH}	1.503 + 0.021D _{std}	1.064 + 0.016D _{std}	0.810 + 0.012D _{std}
		t _{PHL}	1.388 + 0.022D _{std}	0.960 + 0.015D _{std}	0.727 + 0.011D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.280 + 0.002N _{std}	0.167 + 0.001N _{std}	0.097 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.492 + 0.001N _{std}	0.421 + 0.001N _{std}	0.378 + 0.001N _{std}
		t _{PLH}	0.411 + 0.002N _{std}	0.274 + 0.001N _{std}	0.198 + 0.001N _{std}
		t _{PHL}	0.577 + 0.001N _{std}	0.496 + 0.001N _{std}	0.442 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.285 + 0.002N _{std}	0.151 + 0.001N _{std}	0.074 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.493 + 0.001N _{std}	0.431 + 0.001N _{std}	0.388 + 0.000N _{std}
		t _{PLH}	0.418 + 0.002N _{std}	0.264 + 0.001N _{std}	0.182 + 0.001N _{std}
		t _{PHL}	0.578 + 0.001N _{std}	0.508 + 0.001N _{std}	0.453 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.625	11.624
DI	5.398	5.398
PAD (Receiver Input)	534.333	534.333
RG	2.000	2.000
TS	4.289	4.290
Internal	169.215	166.015
Cell Units	1 cell	1 cell

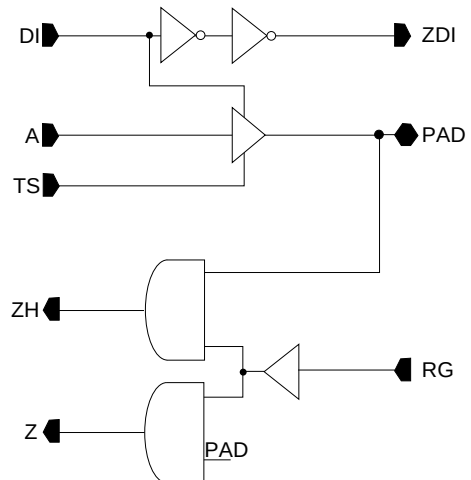
Cell: BT3335T, BT3335T_PM
Function: 3.3V LVTTTL Test 35 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
RG Receiver gate control
PAD Driver output/receiver input
ZH Hysteresis receiver output
Z Non-hysteresis receiver output
ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.616 + 0.031D _{std}	1.163 + 0.024D _{std}	0.883 + 0.019D _{std}
		t _{PHL}	1.470 + 0.031D _{std}	1.037 + 0.022D _{std}	0.790 + 0.018D _{std}
	B	t _{PLH}	1.438 + 0.030D _{std}	1.035 + 0.022D _{std}	0.799 + 0.018D _{std}
		t _{PHL}	1.349 + 0.030D _{std}	0.950 + 0.021D _{std}	0.732 + 0.017D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.280 + 0.002N _{std}	0.167 + 0.001N _{std}	0.097 + 0.001N _{std}
		t _{PHL}	0.492 + 0.001N _{std}	0.421 + 0.001N _{std}	0.378 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.412 + 0.002N _{std}	0.274 + 0.001N _{std}	0.198 + 0.001N _{std}
		t _{PHL}	0.577 + 0.001N _{std}	0.496 + 0.001N _{std}	0.442 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.286 + 0.002N _{std}	0.151 + 0.001N _{std}	0.074 + 0.001N _{std}
		t _{PHL}	0.493 + 0.001N _{std}	0.432 + 0.001N _{std}	0.388 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.418 + 0.002N _{std}	0.264 + 0.001N _{std}	0.182 + 0.001N _{std}
		t _{PHL}	0.579 + 0.001N _{std}	0.508 + 0.001N _{std}	0.453 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.570	11.569
DI	5.396	5.395
PAD (Receiver Input)	457.042	457.042
RG	2.000	2.000
TS	4.289	4.289
Internal	220.760	218.819
Cell Units	1 cell	1 cell

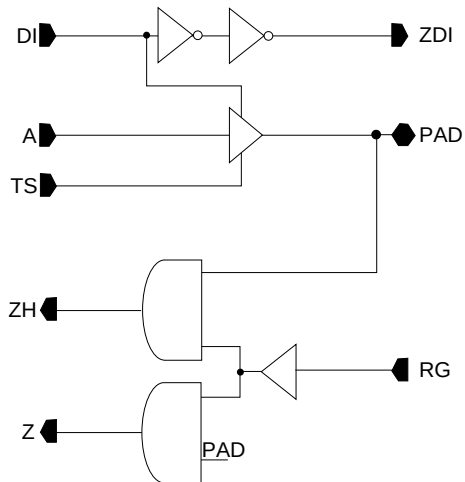
Cell: BT3350T, BT3350T_PM
Function: 3.3V LVTTTL Test 50 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.491 + 0.042D _{std}	1.082 + 0.032D _{std}	0.827 + 0.027D _{std}
		t _{PHL}	1.394 + 0.042D _{std}	0.974 + 0.031D _{std}	0.741 + 0.026D _{std}
	B	t _{PLH}	1.302 + 0.040D _{std}	0.961 + 0.030D _{std}	0.760 + 0.025D _{std}
		t _{PHL}	1.209 + 0.041D _{std}	0.865 + 0.029D _{std}	0.676 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.280 + 0.002N _{std}	0.167 + 0.001N _{std}	0.097 + 0.001N _{std}
		t _{PHL}	0.492 + 0.001N _{std}	0.421 + 0.001N _{std}	0.378 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.412 + 0.002N _{std}	0.274 + 0.001N _{std}	0.198 + 0.001N _{std}
		t _{PHL}	0.577 + 0.001N _{std}	0.496 + 0.001N _{std}	0.442 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.286 + 0.002N _{std}	0.151 + 0.001N _{std}	0.074 + 0.001N _{std}
		t _{PHL}	0.493 + 0.001N _{std}	0.432 + 0.001N _{std}	0.389 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.418 + 0.002N _{std}	0.264 + 0.001N _{std}	0.182 + 0.001N _{std}
		t _{PHL}	0.579 + 0.001N _{std}	0.508 + 0.001N _{std}	0.453 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.635	11.635
DI	5.398	5.397
PAD (Receiver Input)	424.917	425.083
RG	2.000	2.000
TS	4.290	4.290
Internal	282.720	281.639
Cell Units	1 cell	1 cell

Cell: BT3350LVT, BT3350LVT_PM

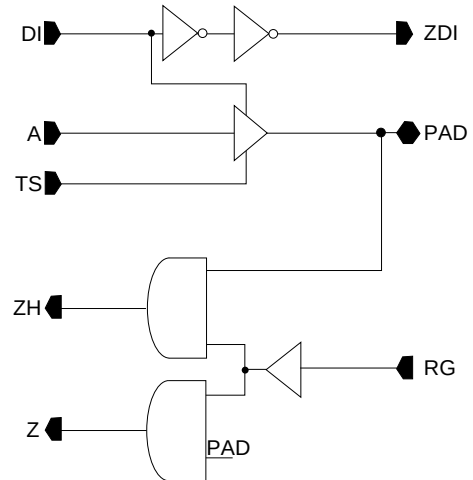
Function: Low Voltage 3.3V LVTTTL Test 50 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces low voltage (as low as 0.9V) internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	2.216 + 0.046D _{std}	1.599 + 0.035D _{std}	1.219 + 0.029D _{std}
		t _{PHL}	2.272 + 0.042D _{std}	1.567 + 0.030D _{std}	1.169 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.312 + 0.001N _{std}	0.166 + 0.001N _{std}	0.088 + 0.000N _{std}
		t _{PHL}	0.600 + 0.001N _{std}	0.484 + 0.000N _{std}	0.423 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.434 + 0.001N _{std}	0.269 + 0.001N _{std}	0.188 + 0.000N _{std}
		t _{PHL}	0.684 + 0.001N _{std}	0.559 + 0.000N _{std}	0.488 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	27.038
DI	5.320
PAD (Receiver Input)	445.292
RG	2.348
TS	4.413
Internal	382.547
Cell Units	1 cell

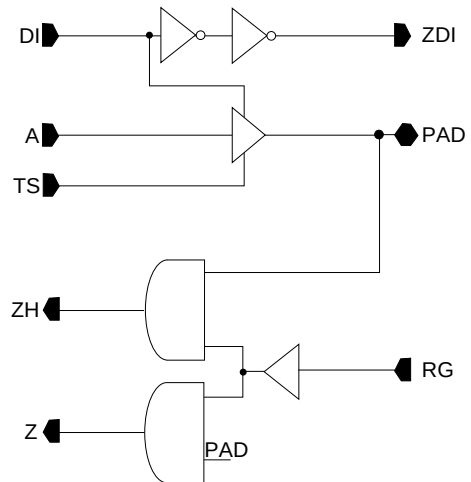
Cell: BT3365T, BT3365T_PM
Function: 3.3V LVTTTL Test 65 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

A Driver data input
TS Driver three-state control
DI Driver inhibit input (DI in)
RG Receiver gate control
PAD Driver output/receiver input
ZH Hysteresis receiver output
Z Non-hysteresis receiver output
ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X



Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.321 + 0.054D _{std}	0.956 + 0.041D _{std}	0.731 + 0.034D _{std}
		t _{PHL}	1.255 + 0.054D _{std}	0.862 + 0.039D _{std}	0.648 + 0.033D _{std}
	B	t _{PLH}	1.115 + 0.053D _{std}	0.833 + 0.040D _{std}	0.675 + 0.034D _{std}
		t _{PHL}	1.106 + 0.053D _{std}	0.795 + 0.038D _{std}	0.620 + 0.033D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.280 + 0.002N _{std}	0.167 + 0.001N _{std}	0.097 + 0.001N _{std}
		t _{PHL}	0.492 + 0.001N _{std}	0.421 + 0.001N _{std}	0.378 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.412 + 0.002N _{std}	0.274 + 0.001N _{std}	0.198 + 0.001N _{std}
		t _{PHL}	0.577 + 0.001N _{std}	0.496 + 0.001N _{std}	0.442 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.285 + 0.002N _{std}	0.151 + 0.001N _{std}	0.074 + 0.001N _{std}
		t _{PHL}	0.494 + 0.001N _{std}	0.432 + 0.001N _{std}	0.389 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.418 + 0.002N _{std}	0.264 + 0.001N _{std}	0.182 + 0.001N _{std}
		t _{PHL}	0.579 + 0.001N _{std}	0.508 + 0.001N _{std}	0.453 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.635	11.636
DI	5.400	5.400
PAD (Receiver Input)	367.917	367.917
RG	2.000	2.000
TS	4.286	4.286
Internal	346.957	346.518
Cell Units	1 cell	1 cell

Cell: BT3390T, BT3390T_PM

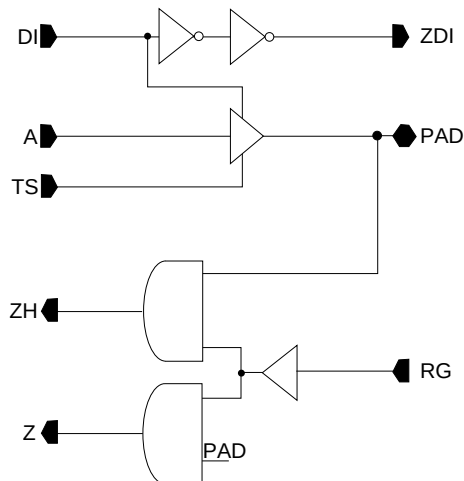
Function: 3.3V LVTTTL Test 90 Ohm 3-State CIO

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Driver Truth Table

Inputs			Outputs	
A	TS	DI	PAD	ZDI
-	-	0	Hi-Z	DI
-	0	-	Hi-Z	DI
-	1	1	A	DI

Receiver Truth Table

Inputs		Outputs	
PAD	RG	Z	ZH
-	0	0	0
0	1	0	0
1	1	1	1
Hi-Z	1	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.215 + 0.075D _{std}	0.882 + 0.057D _{std}	0.678 + 0.048D _{std}
		t _{PHL}	1.179 + 0.073D _{std}	0.800 + 0.054D _{std}	0.598 + 0.045D _{std}
	B	t _{PLH}	1.001 + 0.075D _{std}	0.765 + 0.056D _{std}	0.630 + 0.048D _{std}
		t _{PHL}	1.077 + 0.071D _{std}	0.795 + 0.052D _{std}	0.648 + 0.044D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.280 + 0.002N _{std}	0.167 + 0.001N _{std}	0.097 + 0.001N _{std}
		t _{PHL}	0.492 + 0.001N _{std}	0.421 + 0.001N _{std}	0.378 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.411 + 0.002N _{std}	0.274 + 0.001N _{std}	0.198 + 0.001N _{std}
		t _{PHL}	0.577 + 0.001N _{std}	0.496 + 0.001N _{std}	0.442 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.285 + 0.002N _{std}	0.151 + 0.001N _{std}	0.074 + 0.001N _{std}
		t _{PHL}	0.493 + 0.001N _{std}	0.432 + 0.001N _{std}	0.388 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.418 + 0.002N _{std}	0.264 + 0.001N _{std}	0.182 + 0.001N _{std}
		t _{PHL}	0.578 + 0.001N _{std}	0.508 + 0.001N _{std}	0.453 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.629	11.638
DI	5.395	5.395
PAD (Receiver Input)	330.208	330.208
RG	2.000	2.000
TS	4.286	4.286
Internal	344.000	346.000
Cell Units	1 cell	1 cell

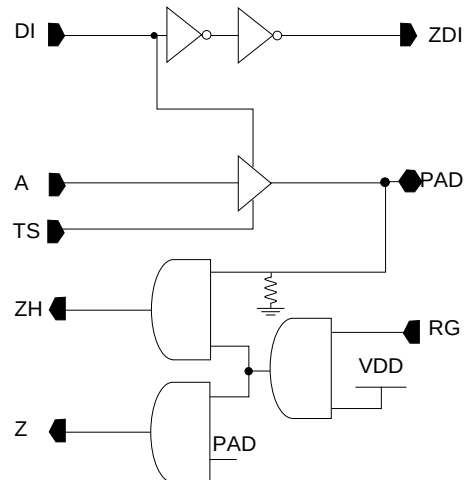
Cell: BT3320PDT, BT3320PDT_PM

Function: 3.3V LVTTL Test 20 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTL off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. If RG is is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in) and I_{ddq} test
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)



Pin Group: (Z, ZH): (0, 2)

Driver Truth Table

Inputs			Outputs		Comments
A	TS	DI	PAD	ZDI	
-	0	-	L	DI	Functional mode
-	-	0	L	DI	Test mode
-	1	1	A	DI	Functional mode



Receiver Truth Table

Inputs		Outputs		Comments
PAD	RG	Z	ZH	
-	0	0	0	Functional mode
0	1	0	0	Functional mode
1	1	1	1	Functional mode

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.647 + 0.024D_{std}$	$1.180 + 0.017D_{std}$	$0.892 + 0.014D_{std}$
		t_{PHL}	$1.478 + 0.024D_{std}$	$1.034 + 0.016D_{std}$	$0.783 + 0.013D_{std}$
	B	t_{PLH}	$1.505 + 0.021D_{std}$	$1.066 + 0.016D_{std}$	$0.810 + 0.012D_{std}$
		t_{PHL}	$1.383 + 0.022D_{std}$	$0.956 + 0.015D_{std}$	$0.724 + 0.011D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.279 + 0.002N _{std}	0.173 + 0.001N _{std}	0.103 + 0.001N _{std}
		t _{PHL}	0.519 + 0.001N _{std}	0.433 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.412 + 0.002N _{std}	0.283 + 0.001N _{std}	0.207 + 0.001N _{std}
		t _{PHL}	0.620 + 0.001N _{std}	0.522 + 0.001N _{std}	0.460 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.284 + 0.002N _{std}	0.158 + 0.001N _{std}	0.080 + 0.001N _{std}
		t _{PHL}	0.521 + 0.001N _{std}	0.443 + 0.001N _{std}	0.397 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.419 + 0.002N _{std}	0.274 + 0.001N _{std}	0.192 + 0.001N _{std}
		t _{PHL}	0.622 + 0.001N _{std}	0.533 + 0.001N _{std}	0.471 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.610	11.609
DI	5.383	5.396
PAD (Receiver Input)	535.042	535.042
RG	2.000	2.000
TS	4.289	4.289
Internal	288.332	278.811
Cell Units	1 cell	1 cell

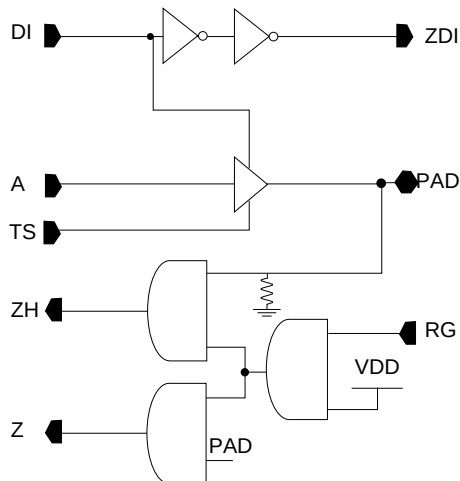
Cell: BT3335PDT, BT3335PDT_PM

Function: 3.3V LVTTTL Test 35 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. If RG is not used, it should be tied to V_{dd}.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in) and I_{ddq} test
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)



Pin Group: (Z, ZH): (0, 2)

Driver Truth Table

Inputs			Outputs		Comments
A	TS	DI	PAD	ZDI	
-	0	-	L	DI	Functional mode
-	-	0	L	DI	Test mode
-	1	1	A	DI	Functional mode

Receiver Truth Table

Inputs		Outputs		Comments
PAD	RG	Z	ZH	
-	0	0	0	Functional mode
0	1	0	0	Functional mode
1	1	1	1	Functional mode

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.619 + 0.032D _{std}	1.167 + 0.024D _{std}	0.887 + 0.019D _{std}
		t _{PHL}	1.463 + 0.031D _{std}	1.030 + 0.022D _{std}	0.784 + 0.018D _{std}
	B	t _{PLH}	1.440 + 0.030D _{std}	1.037 + 0.022D _{std}	0.801 + 0.018D _{std}
		t _{PHL}	1.344 + 0.030D _{std}	0.945 + 0.021D _{std}	0.727 + 0.017D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.279 + 0.002N _{std}	0.173 + 0.001N _{std}	0.103 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.520 + 0.001N _{std}	0.433 + 0.001N _{std}	0.387 + 0.001N _{std}
		t _{PLH}	0.412 + 0.002N _{std}	0.283 + 0.001N _{std}	0.207 + 0.001N _{std}
		t _{PHL}	0.620 + 0.001N _{std}	0.521 + 0.001N _{std}	0.460 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.285 + 0.002N _{std}	0.158 + 0.001N _{std}	0.080 + 0.001N _{std}
PAD-ZH		t _{PHL}	0.521 + 0.001N _{std}	0.444 + 0.001N _{std}	0.397 + 0.000N _{std}
		t _{PLH}	0.419 + 0.002N _{std}	0.274 + 0.001N _{std}	0.192 + 0.001N _{std}
		t _{PHL}	0.622 + 0.001N _{std}	0.533 + 0.001N _{std}	0.471 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.555	11.555
DI	5.378	5.371
PAD (Receiver Input)	457.625	457.625
RG	2.000	2.000
TS	4.289	4.289
Internal	404.454	399.024
Cell Units	1 cell	1 cell

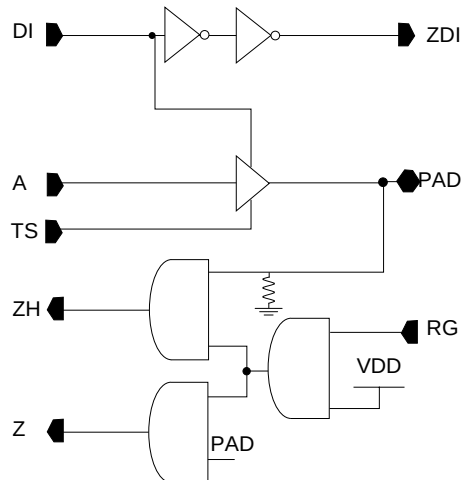
Cell: BT3350PDT, BT3350PDT_PM

Function: 3.3V LVTTL Test 50 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTL off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in) and I_{ddq} test
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)



Pin Group: (Z, ZH): (0, 2)

Driver Truth Table

Inputs			Outputs		Comments
A	TS	DI	PAD	ZDI	
-	0	-	L	DI	Functional mode
-	-	0	L	DI	Test mode
-	1	1	A	DI	Functional mode



Receiver Truth Table

Inputs		Outputs		Comments
PAD	RG	Z	ZH	
-	0	0	0	Functional mode
0	1	0	0	Functional mode
1	1	1	1	Functional mode

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^{\circ}C$ Process = Fast
A-PAD	A	t_{PLH}	$1.525 + 0.041D_{std}$	$1.147 + 0.031D_{std}$	$0.906 + 0.026D_{std}$
		t_{PHL}	$1.410 + 0.041D_{std}$	$1.025 + 0.029D_{std}$	$0.808 + 0.024D_{std}$
	B	t_{PLH}	$1.303 + 0.041D_{std}$	$0.963 + 0.031D_{std}$	$0.763 + 0.026D_{std}$
		t_{PHL}	$1.207 + 0.040D_{std}$	$0.860 + 0.029D_{std}$	$0.671 + 0.024D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.279 + 0.002N _{std}	0.173 + 0.001N _{std}	0.103 + 0.001N _{std}
		t _{PHL}	0.519 + 0.001N _{std}	0.433 + 0.001N _{std}	0.386 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.412 + 0.002N _{std}	0.283 + 0.001N _{std}	0.207 + 0.001N _{std}
		t _{PHL}	0.620 + 0.001N _{std}	0.521 + 0.001N _{std}	0.460 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.284 + 0.002N _{std}	0.158 + 0.001N _{std}	0.080 + 0.001N _{std}
		t _{PHL}	0.521 + 0.001N _{std}	0.444 + 0.001N _{std}	0.397 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.420 + 0.002N _{std}	0.274 + 0.001N _{std}	0.192 + 0.001N _{std}
		t _{PHL}	0.622 + 0.001N _{std}	0.533 + 0.001N _{std}	0.471 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.621	11.620
DI	5.378	5.371
PAD (Receiver Input)	425.792	425.708
RG	2.000	2.000
TS	4.286	4.286
Internal	552.047	548.478
Cell Units	1 cell	1 cell

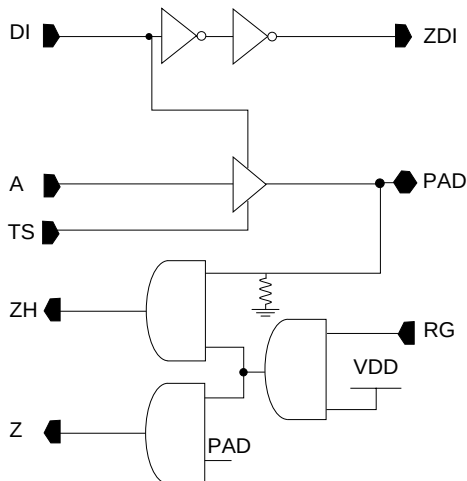
Cell: BT3350LVPDT, BT3350LVPDT_PM

Function: Low Voltage 3.3V LVTTTL Test 50 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces low voltage (as low as 0.9V) internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. If RG is not used, it should be tied to V_{dd}.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in) and I_{ddq} test
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)



Pin Group: (Z, ZH): (0, 2)

Driver Truth Table

Inputs			Outputs		Comments
A	TS	DI	PAD	ZDI	
-	0	-	L	DI	Functional mode
-	-	0	L	DI	Test mode
-	1	1	A	DI	Functional mode

Receiver Truth Table

Inputs		Outputs		Comments
PAD	RG	Z	ZH	
-	0	0	0	Functional mode
0	1	0	0	Functional mode
1	1	1	1	Functional mode

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	2.225 + 0.046D _{std}	1.610 + 0.035D _{std}	1.229 + 0.029D _{std}
		t _{PHL}	2.267 + 0.041D _{std}	1.560 + 0.030D _{std}	1.164 + 0.025D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.325 + 0.001N _{std}	0.186 + 0.001N _{std}	0.110 + 0.000N _{std}
		t _{PHL}	0.596 + 0.001N _{std}	0.471 + 0.000N _{std}	0.407 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.448 + 0.001N _{std}	0.291 + 0.001N _{std}	0.212 + 0.000N _{std}
		t _{PHL}	0.683 + 0.001N _{std}	0.548 + 0.000N _{std}	0.475 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	27.038
DI	5.302
PAD (Receiver Input)	447.708
RG	2.331
TS	4.399
Internal	552.047
Cell Units	1 cell

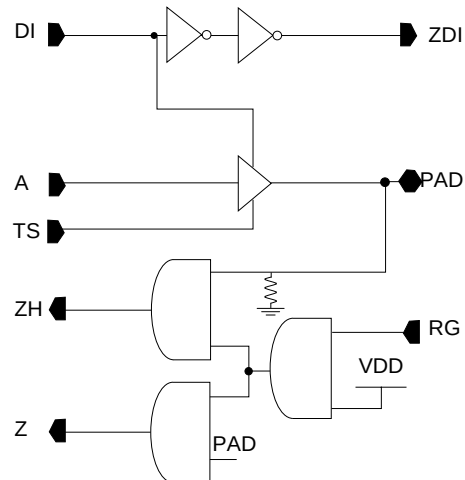
Cell: BT3365PDT, BT3365PDT_PM

Function: 3.3V LVTTL Test 65 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTL off-chip bidirectional data buses. Driver is 65 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in) and I_{ddq} test
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)



Pin Group: (Z, ZH): (0, 2)

Driver Truth Table

Inputs			Outputs		Comments
A	TS	DI	PAD	ZDI	
-	0	-	L	DI	Functional mode
-	-	0	L	DI	Test mode
-	1	1	A	DI	Functional mode



Receiver Truth Table

Inputs		Outputs		Comments
PAD	RG	Z	ZH	
-	0	0	0	Functional mode
0	1	0	0	Functional mode
1	1	1	1	Functional mode

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.324 + 0.054D_{std}$	$0.959 + 0.041D_{std}$	$0.734 + 0.034D_{std}$
		t_{PHL}	$1.249 + 0.053D_{std}$	$0.855 + 0.038D_{std}$	$0.642 + 0.032D_{std}$
	B	t_{PLH}	$1.118 + 0.053D_{std}$	$0.837 + 0.040D_{std}$	$0.682 + 0.034D_{std}$
		t_{PHL}	$1.102 + 0.052D_{std}$	$0.789 + 0.037D_{std}$	$0.622 + 0.031D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.279 + 0.002N _{std}	0.173 + 0.001N _{std}	0.103 + 0.001N _{std}
		t _{PHL}	0.519 + 0.001N _{std}	0.433 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.412 + 0.002N _{std}	0.283 + 0.001N _{std}	0.207 + 0.001N _{std}
		t _{PHL}	0.620 + 0.001N _{std}	0.521 + 0.001N _{std}	0.460 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.284 + 0.002N _{std}	0.158 + 0.001N _{std}	0.080 + 0.001N _{std}
		t _{PHL}	0.521 + 0.001N _{std}	0.444 + 0.001N _{std}	0.397 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.419 + 0.002N _{std}	0.274 + 0.001N _{std}	0.192 + 0.001N _{std}
		t _{PHL}	0.622 + 0.001N _{std}	0.533 + 0.001N _{std}	0.471 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.621	11.621
DI	5.378	5.378
PAD (Receiver Input)	368.708	368.708
RG	2.000	2.000
TS	4.287	4.284
Internal	706.063	704.061
Cell Units	1 cell	1 cell

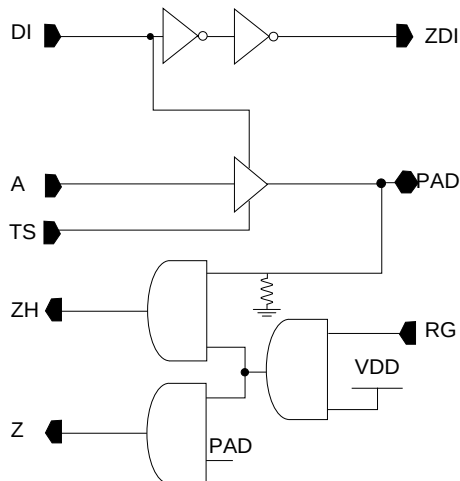
Cell: BT3390PDT, BT3390PDT_PM

Function: 3.3V LVTTTL Test 90 Ohm 3-State CIO w/Pull-Down

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled down to a logic "0" (0.0V) through 8k ohm when the driver is in Hi-Z. If RG is not used, it should be tied to V_{dd} .

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in) and I_{ddq} test
- RG Receiver gate control
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)



Pin Group: (Z, ZH): (0, 2)

Driver Truth Table

Inputs			Outputs		Comments
A	TS	DI	PAD	ZDI	
-	0	-	L	DI	Functional mode
-	-	0	L	DI	Test mode
-	1	1	A	DI	Functional mode

Receiver Truth Table

Inputs		Outputs		Comments
PAD	RG	Z	ZH	
-	0	0	0	Functional mode
0	1	0	0	Functional mode
1	1	1	1	Functional mode

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.217 + 0.076D _{std}	0.885 + 0.058D _{std}	0.681 + 0.049D _{std}
		t _{PHL}	1.172 + 0.071D _{std}	0.792 + 0.052D _{std}	0.591 + 0.043D _{std}
	B	t _{PLH}	0.988 + 0.075D _{std}	0.768 + 0.057D _{std}	0.639 + 0.049D _{std}
		t _{PHL}	1.077 + 0.070D _{std}	0.785 + 0.051D _{std}	0.633 + 0.042D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.279 + 0.002N _{std}	0.173 + 0.001N _{std}	0.103 + 0.001N _{std}
		t _{PHL}	0.519 + 0.001N _{std}	0.433 + 0.001N _{std}	0.387 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.412 + 0.002N _{std}	0.283 + 0.001N _{std}	0.207 + 0.001N _{std}
		t _{PHL}	0.619 + 0.001N _{std}	0.521 + 0.001N _{std}	0.459 + 0.001N _{std}
PAD-Z	B	t _{PLH}	0.284 + 0.002N _{std}	0.158 + 0.001N _{std}	0.080 + 0.001N _{std}
		t _{PHL}	0.521 + 0.001N _{std}	0.444 + 0.001N _{std}	0.397 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.419 + 0.002N _{std}	0.274 + 0.001N _{std}	0.191 + 0.001N _{std}
		t _{PHL}	0.621 + 0.001N _{std}	0.533 + 0.001N _{std}	0.470 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.620	11.623
DI	5.378	5.378
PAD (Receiver Input)	331.125	331.125
RG	2.000	2.000
TS	4.290	4.290
Internal	668.000	672.000
Cell Units	1 cell	1 cell

Cell: BT3320PUT, BT3320PUT_PM

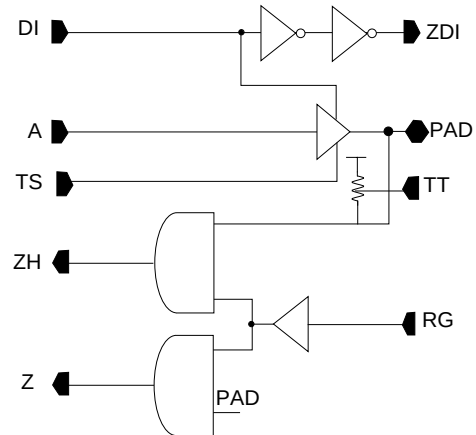
Function: 3.3V LVTTTL Test 20 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 20 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (3.3V) through 8K ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.636 + 0.024D_{std}$	$1.171 + 0.017D_{std}$	$0.885 + 0.014D_{std}$
		t_{PHL}	$1.488 + 0.024D_{std}$	$1.043 + 0.016D_{std}$	$0.790 + 0.013D_{std}$
	B	t_{PLH}	$1.497 + 0.021D_{std}$	$1.060 + 0.015D_{std}$	$0.807 + 0.012D_{std}$
		t_{PHL}	$1.390 + 0.022D_{std}$	$0.962 + 0.015D_{std}$	$0.729 + 0.011D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.269 + 0.002N _{std}	0.153 + 0.001N _{std}	0.082 + 0.001N _{std}
		t _{PHL}	0.502 + 0.001N _{std}	0.433 + 0.001N _{std}	0.392 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.401 + 0.002N _{std}	0.260 + 0.001N _{std}	0.184 + 0.001N _{std}
		t _{PHL}	0.585 + 0.001N _{std}	0.508 + 0.001N _{std}	0.455 + 0.001N _{std}

Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.274 + 0.002N _{std}	0.136 + 0.001N _{std}	0.058 + 0.001N _{std}
		t _{PHL}	0.504 + 0.001N _{std}	0.446 + 0.001N _{std}	0.404 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.408 + 0.002N _{std}	0.249 + 0.001N _{std}	0.166 + 0.001N _{std}
		t _{PHL}	0.586 + 0.001N _{std}	0.522 + 0.001N _{std}	0.468 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.623	11.623
DI	5.395	5.395
PAD (Receiver Input)	536.000	536.167
RG	2.000	2.000
TS	4.289	4.289
TT	8.379	8.373
Internal	169.272	165.996
Cell Units	1 cell	1 cell

Cell: BT3335PUT, BT3335PUT_PM

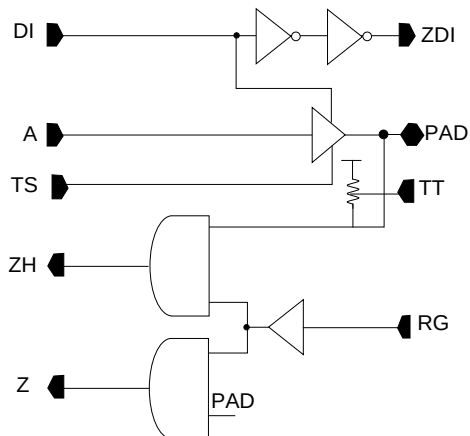
Function: 3.3V LVTTTL Test 35 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 35 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (3.3V) through 8K ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.608 + 0.031D _{std}	1.156 + 0.023D _{std}	0.878 + 0.019D _{std}
		t _{PHL}	1.473 + 0.032D _{std}	1.039 + 0.022D _{std}	0.792 + 0.018D _{std}
	B	t _{PLH}	1.433 + 0.029D _{std}	1.030 + 0.022D _{std}	0.795 + 0.018D _{std}
		t _{PHL}	1.351 + 0.030D _{std}	0.952 + 0.021D _{std}	0.734 + 0.017D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.269 + 0.002N _{std}	0.153 + 0.001N _{std}	0.082 + 0.001N _{std}
		t _{PHL}	0.502 + 0.001N _{std}	0.434 + 0.001N _{std}	0.392 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.401 + 0.002N _{std}	0.260 + 0.001N _{std}	0.184 + 0.001N _{std}
		t _{PHL}	0.585 + 0.001N _{std}	0.507 + 0.001N _{std}	0.455 + 0.001N _{std}



Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.275 + 0.002N _{std}	0.136 + 0.001N _{std}	0.058 + 0.001N _{std}
		t _{PHL}	0.504 + 0.001N _{std}	0.446 + 0.001N _{std}	0.404 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.408 + 0.002N _{std}	0.249 + 0.001N _{std}	0.166 + 0.001N _{std}
		t _{PHL}	0.586 + 0.001N _{std}	0.521 + 0.001N _{std}	0.468 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.570	11.569
DI	5.395	5.396
PAD (Receiver Input)	458.625	458.583
RG	2.000	2.000
TS	4.284	4.287
TT	8.379	8.373
Internal	220.777	218.853
Cell Units	1 cell	1 cell

Cell: BT3350PUT, BT3350PUT_PM

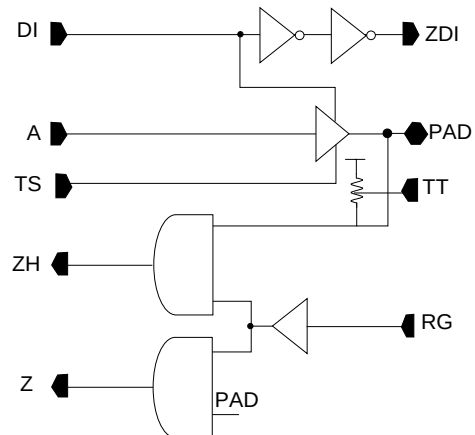
Function: 3.3V LVTTTL Test 50 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (3.3V) through 8K ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.482 + 0.041D_{std}$	$1.074 + 0.031D_{std}$	$0.821 + 0.026D_{std}$
		t_{PHL}	$1.397 + 0.042D_{std}$	$0.977 + 0.031D_{std}$	$0.743 + 0.026D_{std}$
	B	t_{PLH}	$1.297 + 0.040D_{std}$	$0.956 + 0.030D_{std}$	$0.755 + 0.025D_{std}$
		t_{PHL}	$1.213 + 0.041D_{std}$	$0.866 + 0.030D_{std}$	$0.678 + 0.025D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.269 + 0.002N _{std}	0.153 + 0.001N _{std}	0.082 + 0.001N _{std}
		t _{PHL}	0.502 + 0.001N _{std}	0.434 + 0.001N _{std}	0.392 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.401 + 0.002N _{std}	0.260 + 0.001N _{std}	0.184 + 0.001N _{std}
		t _{PHL}	0.585 + 0.001N _{std}	0.507 + 0.001N _{std}	0.455 + 0.001N _{std}

Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.274 + 0.002N _{std}	0.136 + 0.001N _{std}	0.058 + 0.001N _{std}
		t _{PHL}	0.504 + 0.001N _{std}	0.446 + 0.001N _{std}	0.404 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.408 + 0.002N _{std}	0.249 + 0.001N _{std}	0.166 + 0.001N _{std}
		t _{PHL}	0.586 + 0.001N _{std}	0.521 + 0.001N _{std}	0.468 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.635	11.635
DI	5.397	5.396
PAD (Receiver Input)	426.750	426.792
RG	2.000	2.000
TS	4.285	4.286
TT	8.360	8.362
Internal	282.764	281.652
Cell Units	1 cell	1 cell

Cell: BT3350LVPUT, BT3350LVPUT_PM

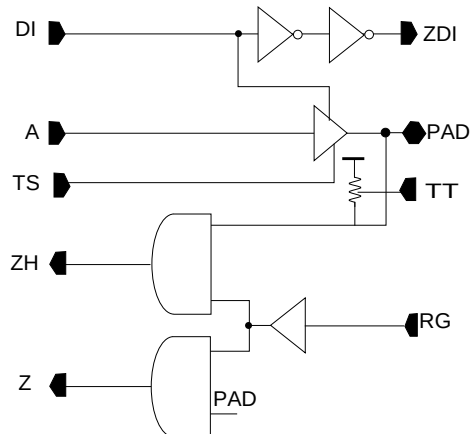
Function: Low Voltage 3.3V LVTTTL Test 50 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces low voltage (as low as 0.9V) internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 50 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (3.3V) through 8K ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	2.191 + 0.045D _{std}	1.579 + 0.034D _{std}	1.204 + 0.029D _{std}
		t _{PHL}	2.274 + 0.042D _{std}	1.569 + 0.031D _{std}	1.171 + 0.026D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.315 + 0.001N _{std}	0.157 + 0.001N _{std}	0.072 + 0.000N _{std}
		t _{PHL}	0.607 + 0.001N _{std}	0.496 + 0.000N _{std}	0.438 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.426 + 0.001N _{std}	0.257 + 0.001N _{std}	0.174 + 0.000N _{std}
		t _{PHL}	0.664 + 0.001N _{std}	0.550 + 0.000N _{std}	0.486 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
A	27.038
DI	5.316
PAD (Receiver Input)	447.292
RG	2.350
TS	4.410
TT	12.477
Internal	382.764
Cell Units	1 cell



Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
A-PAD	A	t_{PLH}	$1.313 + 0.053D_{std}$	$0.949 + 0.040D_{std}$	$0.725 + 0.033D_{std}$
		t_{PHL}	$1.260 + 0.055D_{std}$	$0.864 + 0.040D_{std}$	$0.650 + 0.033D_{std}$
	B	t_{PLH}	$1.114 + 0.052D_{std}$	$0.830 + 0.039D_{std}$	$0.668 + 0.033D_{std}$
		t_{PHL}	$1.107 + 0.054D_{std}$	$0.797 + 0.039D_{std}$	$0.630 + 0.033D_{std}$

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.269 + 0.002N _{std}	0.153 + 0.001N _{std}	0.082 + 0.001N _{std}
		t _{PHL}	0.502 + 0.001N _{std}	0.434 + 0.001N _{std}	0.392 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.401 + 0.002N _{std}	0.260 + 0.001N _{std}	0.184 + 0.001N _{std}
		t _{PHL}	0.585 + 0.001N _{std}	0.507 + 0.001N _{std}	0.455 + 0.001N _{std}

Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.275 + 0.002N _{std}	0.136 + 0.001N _{std}	0.058 + 0.001N _{std}
		t _{PHL}	0.504 + 0.001N _{std}	0.446 + 0.001N _{std}	0.404 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.408 + 0.002N _{std}	0.249 + 0.001N _{std}	0.166 + 0.001N _{std}
		t _{PHL}	0.586 + 0.001N _{std}	0.521 + 0.001N _{std}	0.468 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.631	11.637
DI	5.397	5.397
PAD (Receiver Input)	369.750	369.750
RG	2.000	2.000
TS	4.286	4.285
TT	8.356	8.356
Internal	346.997	346.510
Cell Units	1 cell	1 cell

Cell: BT3390PUT, BT3390PUT_PM

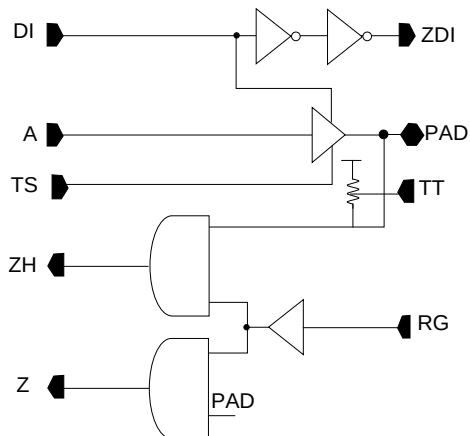
Function: 3.3V LVTTTL Test 90 Ohm 3-State CIO w/Pull-Up

Description:

Noninverting three-state driver/receiver that interfaces 1.8V internal functions with 3.3V LVTTTL off-chip bidirectional data buses. Driver is 90 ohm source-terminated. Output di/dt and performance are chosen by performance level selection. PAD is pulled up to logic "1" (3.3V) through 8K ohm when the driver is in Hi-Z. Pull-up is disabled by TT input during I_{ddq} test.

- A Driver data input
- TS Driver three-state control
- DI Driver inhibit input (DI in)
- RG Receiver gate control
- TT Termination test input
- PAD Driver output/receiver input
- ZH Hysteresis receiver output
- Z Non-hysteresis receiver output
- ZDI Driver inhibit output (DI out)

Pin Group: (Z, ZH): (0, 2)



Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Driver Truth Table

Inputs				Outputs	
TT	A	TS	DI	PAD	ZDI
1	-	-	0	H	DI
1	-	0	-	H	DI
1	-	1	1	A	DI
0	-	-	0	Hi-Z	DI
0	-	0	-	Hi-Z	DI
0	-	1	1	A	DI

Receiver Truth Table

Inputs			Outputs	
PAD	RG	TT	Z	ZH
-	0	-	0	0
0	1	-	0	0
1,H	1	1	1	1
Hi-Z	1	0	X	X

Driver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
A-PAD	A	t _{PLH}	1.206 + 0.073D _{std}	0.875 + 0.055D _{std}	0.672 + 0.046D _{std}
		t _{PHL}	1.179 + 0.074D _{std}	0.800 + 0.054D _{std}	0.599 + 0.046D _{std}
	B	t _{PLH}	0.987 + 0.073D _{std}	0.756 + 0.055D _{std}	0.629 + 0.046D _{std}
		t _{PHL}	1.074 + 0.073D _{std}	0.791 + 0.053D _{std}	0.643 + 0.045D _{std}

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.269 + 0.002N _{std}	0.153 + 0.001N _{std}	0.082 + 0.001N _{std}
		t _{PHL}	0.502 + 0.001N _{std}	0.434 + 0.001N _{std}	0.392 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.400 + 0.002N _{std}	0.260 + 0.001N _{std}	0.184 + 0.001N _{std}
		t _{PHL}	0.584 + 0.001N _{std}	0.507 + 0.001N _{std}	0.454 + 0.001N _{std}



Receiver Propagation Delays (Continued)

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	B	t _{PLH}	0.275 + 0.002N _{std}	0.136 + 0.001N _{std}	0.058 + 0.001N _{std}
		t _{PHL}	0.504 + 0.001N _{std}	0.446 + 0.001N _{std}	0.404 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.407 + 0.002N _{std}	0.249 + 0.001N _{std}	0.166 + 0.001N _{std}
		t _{PHL}	0.586 + 0.001N _{std}	0.521 + 0.001N _{std}	0.468 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level	
	A	B
A	11.635	11.632
DI	5.368	5.374
PAD (Receiver Input)	332.167	332.167
RG	2.000	2.002
TS	4.289	4.288
TT	8.355	8.379
Internal	328.000	334.000
Cell Units	1 cell	1 cell

Cell: IC18T, IC18T_PM

Function: 1.8V CMOS Test Receiver

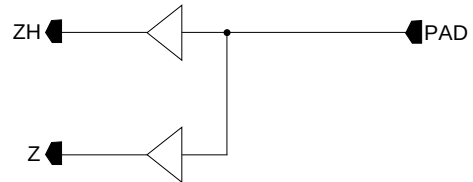
Description:

Stand-alone noninverting receiver that interfaces 1.8V CMOS off-chip unidirectional data buses with 1.8V internal logic.

PAD Receiver input

ZH Hysteresis receiver output

Z Non-hysteresis receiver output



Pin Group: (Z, ZH): (1, 2)

Receiver Truth Table

Input	Outputs	
PAD	ZH	Z
0	0	0
1	1	1
Hi-Z	X	X

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.266 + 0.000N _{std}	0.187 + 0.000N _{std}	0.143 + 0.000N _{std}
		t _{PHL}	0.251 + 0.001N _{std}	0.203 + 0.000N _{std}	0.162 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.462 + 0.000N _{std}	0.335 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.404 + 0.001N _{std}	0.329 + 0.000N _{std}	0.268 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

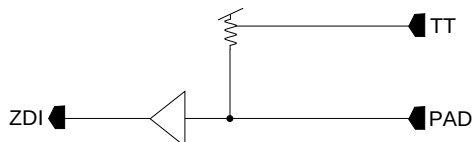
Input Pins	Performance Level
	A
PAD (Receiver Input)	240.583
Internal	76.322
Cell Units	2 cells

Cell: IC18D1PUT, IC18D1PUT_PM

Function: 1.8V CMOS Test DI1 Receiver w/Pull-Up

Description:

Stand-alone noninverting receiver that interfaces 1.8V CMOS off-chip unidirectional data buses with 1.8V internal logic. Serves as first block of DI1 daisy chain. The 8k ohm pull-up resistor is disabled by TT input during I_{ddq} test. Receiver input has hysteresis.



PAD External DI1/driver inhibit input (1st block)

TT Termination test input (TT in)

ZDI Driver inhibit output (DI out)

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Receiver Truth Table

Inputs		Output
PAD	TT	ZDI
0	X	0
1	X	1
Hi-Z	1	1
Hi-Z	0	X

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-ZDI	A	t_{PLH}	$0.435 + 0.000N_{std}$	$0.304 + 0.000N_{std}$	$0.243 + 0.000N_{std}$
		t_{PHL}	$0.417 + 0.001N_{std}$	$0.341 + 0.000N_{std}$	$0.279 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
PAD (Receiver Input)	237.042
TT	1.372
Internal	115.547
Cell Units	2 cells

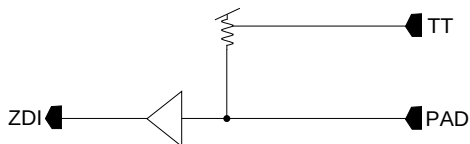


Cell: IC18D2PUT, IC18D2PUT_PM

Function: 1.8V CMOS Test DI2 Receiver w/Pull-Up

Description:

Stand-alone noninverting receiver that interfaces 1.8V CMOS off-chip unidirectional data buses with 1.8V internal logic. Serves as first block of DI2 daisy chain. The 8k ohm pull-up resistor is disabled by TT input during I_{ddq} test. Receiver input has hysteresis.



PAD External DI2/driver inhibit input (1st block)

TT Termination test input (TT in)

ZDI Driver inhibit output (DI out)

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Receiver Truth Table

Inputs		Output
PAD	TT	ZDI
0	X	0
1	X	1
Hi-Z	1	1
Hi-Z	0	X

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-ZDI	A	t_{PLH}	$0.435 + 0.000N_{std}$	$0.304 + 0.000N_{std}$	$0.243 + 0.000N_{std}$
		t_{PHL}	$0.417 + 0.001N_{std}$	$0.341 + 0.000N_{std}$	$0.279 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

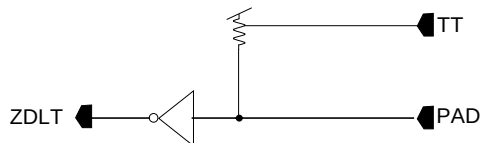
Input Pins	Performance Level
	A
PAD (Receiver Input)	237.042
TT	1.372
Internal	115.547
Cell Units	1 cell

Cell: IC18DLTPUT, IC18DLTPUT_PM

Function: 1.8V Embedded DRAM Leakage Test Receiver w/Pull-Up

Description:

Stand-alone inverting receiver that interfaces 1.8V CMOS off-chip unidirectional data buses with 1.8V internal logic. The 8k ohm pull-up resistor is disabled by TT input during I_{ddq} test. Receiver input has hysteresis.



PAD External DLT inhibit input (1st block)

TT Termination test input (TT in)

ZDLT Driver inhibit output (DLT out)

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Receiver Truth Table

Inputs		Output
PAD	TT	ZDLT
0	X	1
1	X	0
Hi-Z	1	0
Hi-Z	0	X

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-ZDLT	A	t_{PLH}	$0.431 + 0.000N_{std}$	$0.340 + 0.000N_{std}$	$0.273 + 0.000N_{std}$
		t_{PHL}	$0.418 + 0.001N_{std}$	$0.287 + 0.000N_{std}$	$0.224 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

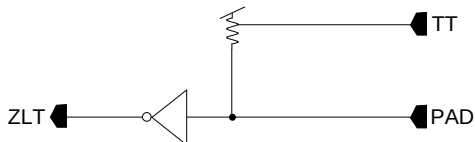
Input Pins	Performance Level
	A
PAD (Receiver Input)	236.167
TT	1.250
Internal	121.309
Cell Units	1 cell

Cell: IC18LTPUT, IC18LTPUT_PM

Function: 1.8V CMOS Leakage Test Receiver w/Pull-Up

Description:

Stand-alone inverting receiver that interfaces 1.8V CMOS off-chip unidirectional data buses with 1.8V internal logic. The 8k ohm pull-up resistor is disabled by TT input during I_{ddq} test. Receiver input has hysteresis.



PAD External LT inhibit input (1st block)

TT Termination test input (TT in)

ZLT Driver inhibit output (LT out)

Pull-Up Receiver Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Receiver Truth Table

Inputs		Output
PAD	TT	ZLT
0	X	1
1	X	0
Hi-Z	1	0
Hi-Z	0	X

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-ZLT	A	t _{PLH}	0.431 + 0.000N _{std}	0.340 + 0.000N _{std}	0.273 + 0.000N _{std}
		t _{PHL}	0.418 + 0.001N _{std}	0.287 + 0.000N _{std}	0.224 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

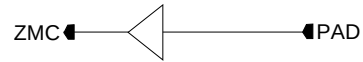
Input Pins	Performance Level
	A
PAD (Receiver Input)	236.167
TT	1.250
Internal	121.309
Cell Units	1 cell

Cell: IC18MCT, IC18MCT_PM

Function: 1.8V CMOS Test Mode Control Receiver

Description:

Stand-alone noninverting receiver that interfaces 1.8V LVTTTL off-chip unidirectional data bus with 1.8V internal logic.



PAD External receiver enable input

ZMC Receiver enable output

Receiver Truth Table

Input	Output
PAD	ZMC
0	0
1	1
Hi-Z	X

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD- ZMC	A	t_{PLH}	$0.431 + 0.000N_{std}$	$0.305 + 0.000N_{std}$	$0.245 + 0.000N_{std}$
		t_{PHL}	$0.416 + 0.001N_{std}$	$0.342 + 0.000N_{std}$	$0.282 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
PAD (Receiver Input)	236.167
Internal	115.932
Cell Units	1 cell



Cell: IC18PDT, IC18PDT_PM

Function: 1.8V CMOS Test Receiver w/Pull-Down

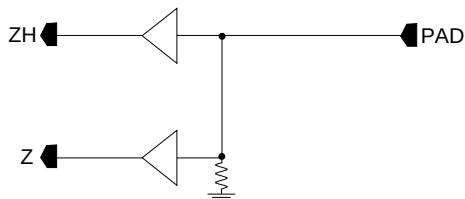
Description:

Stand-alone noninverting receiver that interfaces 1.8V CMOS off-chip unidirectional data buses with 1.8V internal logic. Pull-down is 8k ohm resistor.

PAD Receiver input

ZH Hysteresis receiver output

Z Non-hysteresis receiver output



Pin Group: (Z, ZH): (1, 2)

Receiver Truth Table

Input	Outputs	
PAD	Z	ZH
0	0	0
1	1	1
Hi-Z	0	0

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.275 + 0.000N _{std}	0.202 + 0.000N _{std}	0.159 + 0.000N _{std}
		t _{PHL}	0.246 + 0.001N _{std}	0.192 + 0.000N _{std}	0.149 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.472 + 0.000N _{std}	0.350 + 0.000N _{std}	0.290 + 0.000N _{std}
		t _{PHL}	0.400 + 0.001N _{std}	0.319 + 0.000N _{std}	0.256 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
PAD (Receiver Input)	241.708
Internal	77.800
Cell Units	1 cell

Cell: IC18PUT, IC18PUT_PM

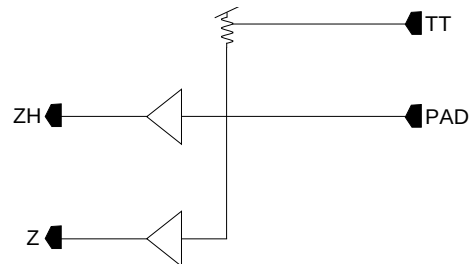
Function: 1.8V CMOS Test Receiver w/Pull-Up

Description:

Stand-alone noninverting receiver that interfaces 1.8V CMOS off-chip unidirectional data buses with 1.8V internal logic. The 8k ohm pull-up resistor is disabled by TT input during I_{ddq} test.

PAD Receiver input
TT Termination test input (TT in)
ZH Hysteresis receiver output
Z Non-hysteresis receiver out

Pin Group: (Z, ZH): (1, 2)



Pull-Up Resistor Truth Table

Input	Output
TT	Resistor
0	Disabled
1	Enabled

Receiver Truth Table

Inputs		Outputs	
PAD	TT	Z	ZH
0	X	0	0
1	X	1	1
Hi-Z	1	1	1
Hi-Z	0	X	X

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.257 + 0.000N _{std}	0.176 + 0.000N _{std}	0.131 + 0.000N _{std}
		t _{PHL}	0.263 + 0.001N _{std}	0.217 + 0.000N _{std}	0.176 + 0.000N _{std}
t _{PLH}		0.455 + 0.000N _{std}	0.325 + 0.000N _{std}	0.262 + 0.000N _{std}	
t _{PHL}		0.416 + 0.001N _{std}	0.343 + 0.000N _{std}	0.282 + 0.000N _{std}	



Capacitance (in units of N_{std}) and Cell Sizes

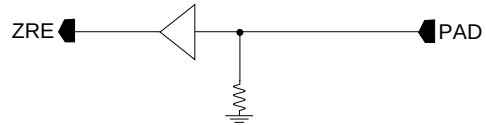
Input Pins	Performance Level
	A
PAD (Receiver Input)	242.167
TT	1.372
Internal	80.144
Cell Units	1 cell

Cell: IC18REPDT, IC18REPDT_PM

Function: 1.8V CMOS Test Reference Enable (RE) Receiver w/Pull-Down

Description:

Stand-alone noninverting receiver that interfaces 1.8V CMOS off-chip unidirectional data bus with 1.8V internal logic. Pull-down resistor is 8k ohm.



PAD External receiver enable input

ZRE Receiver enable output

RE Receiver Truth Table

Input	Output
PAD	ZRE
0	0
1	1
Hi-Z	0

Note: PAD input has a pull-down resistor.

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD- ZRE	A	t_{PLH}	$0.443 + 0.000N_{std}$	$0.322 + 0.000N_{std}$	$0.263 + 0.000N_{std}$
		t_{PHL}	$0.413 + 0.001N_{std}$	$0.334 + 0.000N_{std}$	$0.271 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
PAD (Receiver Input)	237.292
Internal	119.646
Cell Units	1 cell

Cell: IC18RIT, IC18RIT_PM

Function: 1.8V CMOS Test RI/TT Receiver

Description:

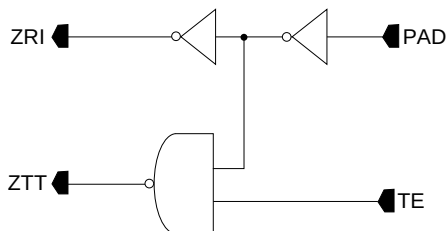
Stand-alone noninverting receiver that interfaces 1.8V CMOS off-chip unidirectional data buses with 1.8V internal logic. Serves as first block of RI daisy chain and TT network. Receiver input has hysteresis. TE input should be fed by TE receiver or tied to "1".

PAD External receiver inhibit input, first RI block.

TE External test enable input

ZRI Receiver inhibit output (RI out), feeding RI daisy chain.

ZTT Termination test output (TT out), feeding TT network.



Receiver Truth Table

Inputs		Outputs	
PAD	TE	ZRI	ZTT
0	0	0	1
1	0	1	1
0	1	0	0
1	1	1	1
Hi-Z	0	X	1
Hi-Z	1	X	X

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-ZRI	A	t _{PLH}	0.432 + 0.000N _{std}	0.306 + 0.000N _{std}	0.244 + 0.000N _{std}
		t _{PHL}	0.418 + 0.001N _{std}	0.345 + 0.000N _{std}	0.282 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

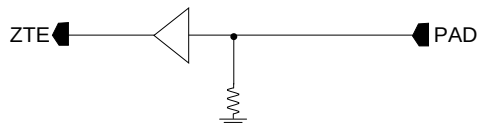
Input Pins	Performance Level
	A
PAD (Receiver Input)	237.500
TE	3.766
Internal	116.138
Cell Units	1 cell

Cell: IC18TEPDT, IC18TEPDT_PM

Function: 1.8V CMOS Test Enable (TE) Receiver w/Pull-Down

Description:

Stand-alone noninverting receiver that interfaces 1.8V CMOS off-chip unidirectional data bus with 1.8V internal logic. Pull-down resistor is 8k ohm.



PAD External receiver enable input

ZTE Test enable output

TE Receiver Truth Table

Input	Output
PAD	ZTE
0	0
1	1
Hi-Z	0

Note: PAD input has a pull-down resistor.

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-ZTE	A	t _{PLH}	0.441 + 0.000N _{std}	0.320 + 0.000N _{std}	0.262 + 0.000N _{std}
		t _{PHL}	0.411 + 0.001N _{std}	0.332 + 0.000N _{std}	0.270 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
PAD (Receiver Input)	237.292
Internal	118.183
Cell Units	1 cell

Cell: IHSTLT, IHSTLT_PM

Function: IHSTL Test Differential Receiver

Description:

Noninverting differential receiver used to receive complementary 1.8V HSTL signals. A differential termination between PAD and PADN inputs is recommended. This receiver requires only a 1.8V V_{dd} supply.

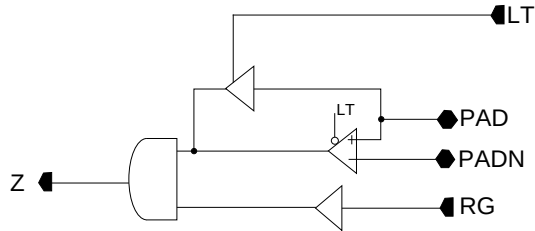
PAD In-phase receiver input

PADN Out-phase receiver input

LT DC current gate (I_{dd} test) input

RG Receiver gate control

Z Receiver output



Receiver Truth Table

Inputs				Output	Comments
PAD	PADN	LT	RG	Z	
-	-	-	0	0	Test mode
0 ¹	1	0	1	0	Function mode
1 ¹	0	0	1	1	Functional mode
1 ¹	1	0	1	X	Functional mode
0 ¹	0	0	1	X	Functional mode
_2	-	1	1	PAD	Bypass mode

¹. PAD input requires HSTL levels.

². PAD input requires CMOS levels.

Usage Notes:

1. Normal receiver operation requires a differential input signal of ± 200 mV around a common mode input signal of 0.90V nominal.
2. During I_{ddq} test, CMOS levels must be applied to PAD.



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V T _j = 125°C Process = Slow	V _{dd} = 1.8V T _j = 25°C Process = Nom.	V _{dd} = 1.95V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.533 + 0.001N _{std}	0.325 + 0.001N _{std}	0.179 + 0.000N _{std}
		t _{PHL}	0.533 + 0.001N _{std}	0.342 + 0.001N _{std}	0.209 + 0.001N _{std}
PADN-Z		t _{PLH}	0.533 + 0.001N _{std}	0.325 + 0.001N _{std}	0.179 + 0.000N _{std}
		t _{PHL}	0.533 + 0.001N _{std}	0.342 + 0.001N _{std}	0.209 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
LT	3.342
PAD (Receiver Input)	195.458
PADN (Receiver Input)	196.083
RG	7.409
Internal	60.417
Cell Units	2 cells

Cell: ILVDST, ILVDST_PM

Function: 1.8V LVDS Wide Common Mode Test Receiver

Description:

Noninverting differential receiver that interfaces between off-chip unidirectional LVDS data buses and 1.8V internal logic. An off-chip differential terminator of 100 ohm between PAD and PADN inputs is required when interfacing with an OLVDS buffer. Receiver has wide input common mode ranging from 0V to V_{dd} supply.

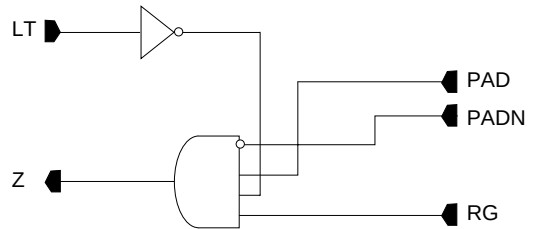
RG Receiver gate control

LT DC current gate (I_{dd} test) input

PAD In-phase receiver in

PADN Out-phase receiver in

Z Receiver out



Receiver Truth Table

Inputs				Output	Comments
PAD	PADN	LT	RG	Z	
0	1	0	1	0	Functional mode
1	0	0	1	1	Functional mode
1	1	0	1	X	Functional mode
0	0	0	1	X	Functional mode
-	-	0	0	0	Functional mode/test mode (receiver power off)
-	-	1	1	PAD	I_{ddq} test/burn-in
-	-	1	0	0	I_{ddq} test/burn-in

Usage Notes:

1. Receiver can accommodate a very wide common mode ranging from V_{dd} to 0V. Minimum input swing requires ± 100 mV around the common mode voltage. See "LVDS Receiver DC Specifications" on page 124 for more details.
2. During I_{ddq} test, CMOS signal must be applied to PAD input while PADN is left floating.



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.544 + 0.001N_{std}$	$0.326 + 0.001N_{std}$	$0.202 + 0.001N_{std}$
		t_{PHL}	$0.547 + 0.001N_{std}$	$0.335 + 0.001N_{std}$	$0.210 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

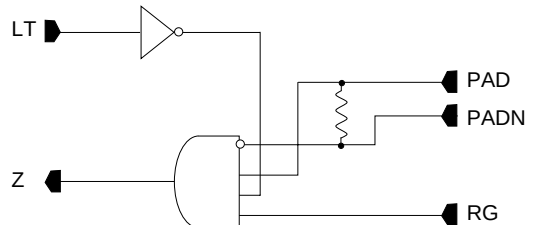
Input Pins	Performance Level
	A
LT	11.893
PAD (Receiver Input)	188.971
PADN (Receiver Input)	186.354
RG	16.237
Internal	136.609
Cell Units	2 cells

Cell: ILVDSDT, ILVDSDT_PM

Function: 1.8V LVDS Wide Common Mode Test Receiver w/Terminator

Description:

Noninverting differential receiver that interfaces between off-chip unidirectional LVDS data buses and 1.8V internal logic. An on-chip differential terminator of 100 ohm between PAD and PADN inputs is provided. Receiver has wide input common mode ranging from 0V to V_{dd} supply.



RG Receiver gate control
 LT DC current gate (I_{dd} test) input
 PAD In-phase receiver in
 PADN Out-phase receiver in
 Z Receiver out

Receiver Truth Table

Inputs				Output	Comments
PAD	PADN	LT	RG	Z	
0	1	0	1	0	Functional mode
1	0	0	1	1	Functional mode
1	1	0	1	X	Functional mode
0	0	0	1	X	Functional mode
-	-	0	0	0	Functional mode/test mode (receiver power off)
-	-	1	1	PAD	I_{ddq} test/burn-in
-	-	1	0	0	I_{ddq} test/burn-in

Usage Notes:

1. Receiver can accommodate a very wide common mode ranging from V_{dd} to 0V. Minimum input swing requires ± 50 mV around the common mode voltage. See "LVDS Receiver DC Specifications" on page 124 for more details.
2. On-chip terminator tolerance is approximately $\pm 26\%$ over process range and temperature range between 0°C to 100°C.
3. During I_{ddq} test, CMOS signal must be applied to PAD input, while PADN is left floating.



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.547 + 0.001N_{std}$	$0.327 + 0.001N_{std}$	$0.203 + 0.001N_{std}$
		t_{PHL}	$0.550 + 0.001N_{std}$	$0.336 + 0.001N_{std}$	$0.211 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
LT	11.893
PAD (Receiver Input)	204.167
PADN (Receiver Input)	198.000
RG	16.230
Internal	138.569
Cell Units	2 cells

Cell: IP25T, IP25T_PM

Function: 2.5V CMOS (3.3V Tolerant) Test Receiver

Description:

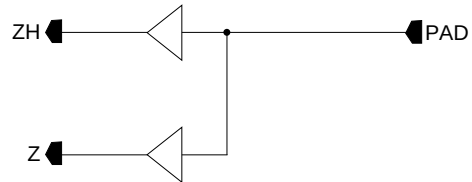
Stand-alone noninverting receiver that interfaces 2.5V off-chip unidirectional data buses with 1.8V internal logic and is tolerant of 3.3V LVTTTL levels.

PAD Receiver input

ZH Hysteresis receiver output

Z Non-hysteresis receiver output

Pin Group: (Z, ZH): (1, 2)



Receiver Truth Table

Input	Outputs	
PAD	ZH	Z
0	0	0
1	1	1

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.434 + 0.002N _{std}	0.294 + 0.001N _{std}	0.222 + 0.001N _{std}
		t _{PHL}	0.394 + 0.002N _{std}	0.311 + 0.001N _{std}	0.251 + 0.001N _{std}
PAD-ZH		t _{PLH}	0.622 + 0.002N _{std}	0.434 + 0.001N _{std}	0.346 + 0.001N _{std}
		t _{PHL}	0.551 + 0.002N _{std}	0.451 + 0.001N _{std}	0.373 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
PAD (Receiver Input)	138.575
Internal	46.02
Cell Units	1 cell

Cell: IP25D1T, IP25D1T_PM

Function: 2.5V CMOS (3.3V Tolerant) Test DI1 Receiver

Description:

Stand-alone noninverting receiver that interfaces 2.5V off-chip unidirectional data buses with 1.8V internal logic and is tolerant of 3.3V LVTTTL levels. Serves as first block of DI1 daisy chain. Receiver input has hysteresis.



PAD External DI1/driver inhibit input (1st block)

ZDI Driver inhibit output (DI out)

Receiver Truth Table

Input	Output
PAD	ZDI
0	0
1	1

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-ZDI	A	t _{PLH}	0.611 + 0.002N _{std}	0.420 + 0.001N _{std}	0.331 + 0.001N _{std}
		t _{PHL}	0.539 + 0.002N _{std}	0.439 + 0.001N _{std}	0.360 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
PAD (Receiver Input)	130.708
Internal	61.742
Cell Units	2 cells

Cell: IP25D2T, IP25D2T_PM

Function: 2.5V CMOS (3.3V Tolerant) Test DI2 Receiver

Description:

Stand-alone noninverting receiver that interfaces 2.5V off-chip unidirectional data buses with 1.8V internal logic and is tolerant of 3.3V LVTTTL levels. Serves as first block of DI2 daisy chain. Receiver input has hysteresis.



PAD External DI2/driver inhibit input (1st block)

ZDI Driver inhibit output (DI out)

Receiver Truth Table

Input	Output
PAD	ZDI
0	0
1	1

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^\circ C$ Process = Fast
PAD-ZDI	A	t_{PLH}	$0.611 + 0.002N_{std}$	$0.420 + 0.001N_{std}$	$0.331 + 0.001N_{std}$
		t_{PHL}	$0.539 + 0.002N_{std}$	$0.439 + 0.001N_{std}$	$0.360 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

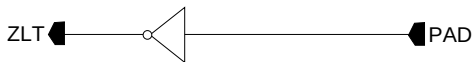
Input Pins	Performance Level
	A
PAD (Receiver Input)	130.708
Internal	61.741
Cell Units	2 cells

Cell: IP25LTT, IP25LTT_PM

Function: 2.5V CMOS (3.3V Tolerant) Leakage Test Receiver

Description:

Stand-alone inverting receiver that interfaces 2.5V off-chip unidirectional data buses with 1.8V internal logic and is tolerant of 3.3V LVTTTL levels. Receiver input has hysteresis.



PAD External LT inhibit input

ZLT Driver inhibit output (LT out)

Receiver Truth Table

Input	Output
PAD	ZLT
0	1
1	0

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-ZLT	A	t _{PLH}	0.751 + 0.002N _{std}	0.586 + 0.001N _{std}	0.473 + 0.001N _{std}
		t _{PHL}	0.615 + 0.002N _{std}	0.417 + 0.001N _{std}	0.325 + 0.001N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

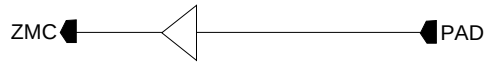
Input Pins	Performance Level
	A
PAD (Receiver Input)	130.821
Internal	64.510
Cell Units	1 cell

Cell: IP25MCT, IP25MCT_PM

Function: 2.5V CMOS (3.3V Tolerant) Test Mode Control Receiver

Description:

Stand-alone noninverting receiver that interfaces 2.5V off-chip unidirectional data buses with 1.8V internal logic and is tolerant of 3.3V LVTTTL levels. Receiver input has hysteresis.



PAD External receiver mode control input

ZMC Mode control output

Receiver Truth Table

Input	Output
PAD	ZMC
0	0
1	1

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^{\circ}C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^{\circ}C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^{\circ}C$ Process = Fast
PAD- ZMC	A	t_{PLH}	$0.605 + 0.002N_{std}$	$0.420 + 0.001N_{std}$	$0.333 + 0.001N_{std}$
		t_{PHL}	$0.534 + 0.002N_{std}$	$0.436 + 0.001N_{std}$	$0.359 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
PAD (Receiver Input)	130.062
Internal	61.865
Cell Units	1 cell

Cell: IP25RET, IP25RET_PM

Function: 2.5V CMOS (3.3V Tolerant) Test Reference Enable Receiver

Description:

Stand-alone noninverting receiver that interfaces 2.5V off-chip unidirectional data buses with 1.8V internal logic and is tolerant of 3.3V LVTTTL levels. Receiver input has hysteresis.



PAD External receiver enable input

ZRE Receiver enable output

Receiver Truth Table

Input	Output
PAD	ZRE
0	0
1	1
Hi-Z	0

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^\circ C$ Process = Fast
PAD- ZRE	A	t_{PLH}	$0.605 + 0.002N_{std}$	$0.420 + 0.001N_{std}$	$0.333 + 0.001N_{std}$
		t_{PHL}	$0.535 + 0.002N_{std}$	$0.436 + 0.001N_{std}$	$0.359 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
PAD (Receiver Input)	130.062
Internal	70.000
Cell Units	1 cell

Cell: IP25RIT, IP25RIT_PM

Function: 2.5V CMOS (3.3V Tolerant) Test RI/TT Receiver

Description:

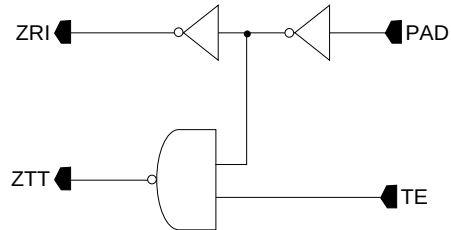
Stand-alone noninverting receiver that interfaces 2.5V off-chip unidirectional data buses with 1.8V internal logic and is tolerant of 3.3V LVTTTL levels. Serves as first block of the RI daisy chain and TT network. Receiver input has hysteresis. TE input should be fed by TE receiver or tied to "1."

PAD External receiver inhibit input, first RI block

TE External test enable input

ZRI Receiver inhibit output (RI out), feeding RI daisy chain

ZTT Termination test output (TT out), feeding TT network.



Receiver Truth Table

Inputs		Outputs	
PAD	TE	ZRI	ZTT
0	0	0	1
1	0	1	1
0	1	0	0
1	1	1	1
Hi-Z	0	X	1
Hi-Z	1	X	X

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd250} = 2.3V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd250} = 2.5V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd250} = 2.7V T _j = 0°C Process = Fast
PAD-ZRI	A	t _{PLH}	0.615 + 0.002N _{std}	0.425 + 0.001N _{std}	0.335 + 0.001N _{std}
		t _{PHL}	0.541 + 0.002N _{std}	0.443 + 0.001N _{std}	0.364 + 0.001N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
PAD (Receiver Input)	133.504
TE	10.830
Internal	67.988
Cell Units	1 cell

Cell: IP33T, IP33T_PM

Function: 5.0V Tolerant 3.3V LVTTL Test Receiver

Description:

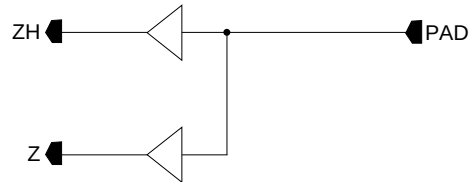
Stand-alone noninverting receiver that interfaces to 3.3V or 5.0V LVTTL off-chip unidirectional data buses with internal logic.

PAD Receiver input

ZH Hysteresis receiver output

Z Non-hysteresis receiver output

Pin Group: (Z, ZH): (1, 2)



Receiver Truth Table

Input	Outputs	
PAD	ZH	Z
0	0	0
1	1	1

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-Z	A	t _{PLH}	0.384 + 0.002N _{std}	0.209 + 0.001N _{std}	0.118 + 0.001N _{std}
		t _{PHL}	0.596 + 0.001N _{std}	0.492 + 0.001N _{std}	0.432 + 0.000N _{std}
PAD-ZH		t _{PLH}	0.584 + 0.002N _{std}	0.330 + 0.001N _{std}	0.213 + 0.001N _{std}
		t _{PHL}	0.675 + 0.001N _{std}	0.564 + 0.001N _{std}	0.492 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
PAD (Receiver Input)	124.087
Internal	49.961
Cell Units	1 cell

Cell: IP33D1T, IP33D1T_PM

Function: 5.0V Tolerant 3.3V LVTTTL Test D1 Receiver

Description:

Stand-alone noninverting receiver that interfaces to 3.3V or 5.0V LVTTTL off-chip unidirectional data buses with internal logic. Serves as first block of DI1 daisy chain. Receiver input has hysteresis.



PAD External DI1/driver inhibit input (1st block)

ZDI Driver inhibit output (DI out)

Receiver Truth Table

Input	Output
PAD	ZDI
0	0
1	1

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-ZDI	A	t _{PLH}	0.592 + 0.002N _{std}	0.331 + 0.001N _{std}	0.212 + 0.001N _{std}
		t _{PHL}	0.660 + 0.001N _{std}	0.562 + 0.001N _{std}	0.494 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

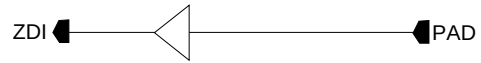
Input Pins	Performance Level
	A
PAD (Receiver Input)	147.408
Internal	95.350
Cell Units	1 cell

Cell: IP33D2T, IP33D2T_PM

Function: 5.0V Tolerant 3.3V LVTTTL Test D2 Receiver

Description:

Stand-alone noninverting receiver that interfaces to 3.3V or 5.0V LVTTTL off-chip unidirectional data buses with internal logic. Serves as first block of DI2 daisy chain. Receiver input has hysteresis.



PAD External DI2/driver inhibit input (1st block)

ZDI Driver inhibit output (DI out)

Receiver Truth Table

Input	Output
PAD	ZDI
0	0
1	1

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
PAD-ZDI	A	t_{PLH}	$0.592 + 0.002N_{std}$	$0.331 + 0.001N_{std}$	$0.212 + 0.001N_{std}$
		t_{PHL}	$0.660 + 0.001N_{std}$	$0.562 + 0.001N_{std}$	$0.494 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

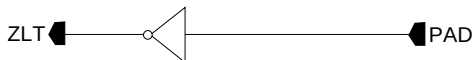
Input Pins	Performance Level
	A
PAD (Receiver Input)	147.408
Internal	95.350
Cell Units	1 cell

Cell: IP33LTT, IP33LTT_PM

Function: 5.0V Tolerant 3.3V LVTTL Leakage Test Receiver

Description:

Stand-alone inverting receiver that interfaces to 3.3V or 5.0V LVTTL off-chip unidirectional data buses with internal logic. Receiver input has hysteresis.



PAD External LT inhibit input

ZLT Driver inhibit output (LT out)

Receiver Truth Table

Input	Output
PAD	ZLT
0	1
1	0

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-ZLT	A	t _{PLH}	0.902 + 0.002N _{std}	0.724 + 0.001N _{std}	0.617 + 0.001N _{std}
		t _{PHL}	0.481 + 0.001N _{std}	0.272 + 0.001N _{std}	0.176 + 0.000N _{std}

Capacitance (in units of N_{std}) and Cell Sizes

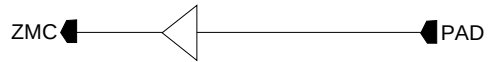
Input Pins	Performance Level
	A
PAD (Receiver Input)	147.475
Internal	120.936
Cell Units	1 cell

Cell: IP33MCT, IP33MCT_PM

Function: 5.0V Tolerant 3.3V LVTTL Test Mode Control Receiver

Description:

Stand-alone noninverting receiver that interfaces to 3.3V or 5.0V LVTTL off-chip unidirectional data buses with internal logic. Receiver input has hysteresis.



PAD External receiver mode control input

ZMC Mode control output

Receiver Truth Table

Input	Output
PAD	ZMC
0	0
1	1

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
PAD- ZMC	A	t_{PLH}	$0.589 + 0.002N_{std}$	$0.333 + 0.001N_{std}$	$0.218 + 0.001N_{std}$
		t_{PHL}	$0.660 + 0.001N_{std}$	$0.551 + 0.001N_{std}$	$0.482 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
PAD (Receiver Input)	146.633
Internal	61.332
Cell Units	1 cell

Cell: IP33RET, IP33RET_PM

Function: 5.0V Tolerant 3.3V LVTTTL Test Reference Enable Receiver

Description:

Stand-alone noninverting receiver that interfaces to 3.3V or 5.0V LVTTTL off-chip unidirectional data buses with 1.8V internal logic. Receiver input has hysteresis.



PAD External receiver enable input

ZRE Receiver enable output

Receiver Truth Table

Input	Output
PAD	ZRE
0	0
1	1
Hi-Z	0

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd330} = 3.0V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd330} = 3.3V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd330} = 3.6V$ $T_j = 0^\circ C$ Process = Fast
PAD-ZRE	A	t_{PLH}	$0.589 + 0.002N_{std}$	$0.334 + 0.001N_{std}$	$0.218 + 0.001N_{std}$
		t_{PHL}	$0.661 + 0.001N_{std}$	$0.551 + 0.001N_{std}$	$0.483 + 0.001N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
PAD (Receiver Input)	146.633
Internal	82.000
Cell Units	1 cell

Cell: IP33RIT, IP33RIT_PM

Function: 5.0V Tolerant 3.3V LVTTTL Test RI/TT Receiver

Description:

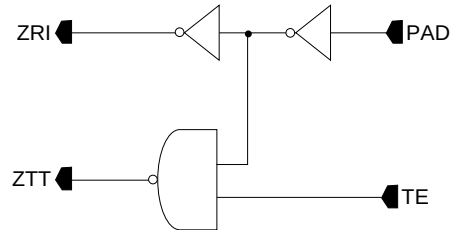
Stand-alone noninverting receiver that interfaces to 3.3V or 5.0V LVTTTL off-chip unidirectional data buses with internal logic. Serves as first block of RI and TT daisy chain. Receiver input has hysteresis. TE input should be fed by TE receiver or tied to "1."

PAD External receiver inhibit input, first RI block

TE External test enable input

ZRI Receiver inhibit output (RI out), feeding RI daisy chain

ZTT Termination test output (TT out), feeding TT daisy chain



Receiver Truth Table

Inputs		Outputs	
PAD	TE	ZRI	ZTT
0	0	0	1
1	0	1	1
0	1	0	0
1	1	1	1
Hi-Z	0	X	1
Hi-Z	1	X	X

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N _{std})		
			V _{dd} = 1.65V V _{dd330} = 3.0V T _j = 125°C Process = Slow	V _{dd} = 1.8V V _{dd330} = 3.3V T _j = 25°C Process = Nom.	V _{dd} = 1.95V V _{dd330} = 3.6V T _j = 0°C Process = Fast
PAD-ZRI	A	t _{PLH}	0.631 + 0.002N _{std}	0.351 + 0.001N _{std}	0.226 + 0.001N _{std}
		t _{PHL}	0.686 + 0.001N _{std}	0.581 + 0.001N _{std}	0.508 + 0.000N _{std}



Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
PAD (Receiver Input)	151.333
TE	7.407
Internal	128.506
Cell Units	1 cell

Cell: IPECLT, IPECLT_PM

Function: 1.8V/2.5V PECL Test Differential Receiver

Description:

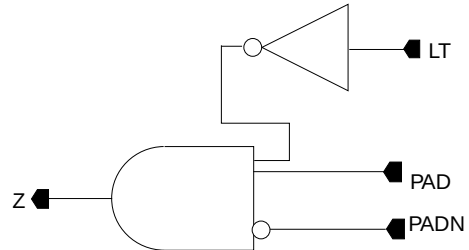
Noninverting differential receiver used to receive complementary ECL signals referenced to V_{dd250} (2.5V nominal) supply. All pins exclusive of PAD and PADN are referenced to the Vdd supply (1.8V nominal). A differential termination of 100 ohms between PAD and PADN inputs is recommended.

PAD In-phase drive in

PADN Out-phase driver in

LT DC current gate (I_{dd} test) input

Z Receiver out



Receiver Truth Table

Inputs			Outputs	Comments
PAD	PADN	LT	Z	
0	1	0	0	Functional mode
1	0	0	1	Functional mode
1	1	0	X	Functional mode
0	0	0	X	Functional mode
-	-	1	PAD	Leakage test

Usage Notes:

1. Normal receiver operation requires a differential input signal of ± 400 mV around a common mode input signal of 2.0V nominal.
2. If the input to the receiver is unknown state (Hi-Z), then the output is indeterminate.
3. During I_{ddq} test, 2.5V CMOS levels must be applied to PAD.



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.558 + 0.001N_{std}$	$0.365 + 0.001N_{std}$	$0.256 + 0.001N_{std}$
		t_{PHL}	$0.595 + 0.001N_{std}$	$0.394 + 0.000N_{std}$	$0.278 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
LT	2.735
PAD (Receiver Input)	233.500
PADN (Receiver Input)	229.500
Internal	139.550
Cell Units	2 cells

Refer to "PECL Receiver Specifications" on page 134 for more information.

Cell: IPECLDT, IPECLDT_PM

Function: 1.8V/2.5V PECL Test Differential Receiver

Description:

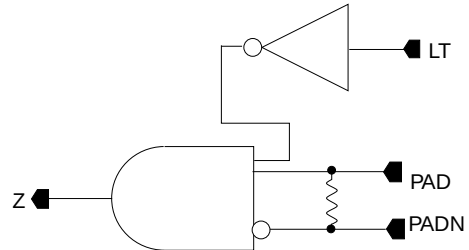
Noninverting differential receiver used to receive complementary ECL signals referenced to V_{dd250} (2.5V nominal) supply. All pins exclusive of PAD and PADN are referenced to the Vdd supply (1.8V nominal). A differential termination of 100 ohms is inserted between PAD and PADN.

PAD In-phase drive in

PADN Out-phase driver in

LT DC current gate (I_{dd} test) input

Z Receiver out



Receiver Truth Table

Inputs			Outputs	Comments
PAD	PADN	LT	Z	
0	1	0	0	Functional mode
1	0	0	1	Functional mode
1	1	0	X	Functional mode
0	0	0	X	Functional mode
-	-	1	PAD	Leakage test

Usage Notes:

1. Normal receiver operation requires a differential input signal of ± 400 mV around a common mode input signal of 2.0V nominal.
2. If the input to the receiver is unknown state (Hi-Z), then the output is indeterminate.
3. During I_{ddq} test, 2.5V CMOS levels must be applied to PAD.



Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.558 + 0.001N_{std}$	$0.365 + 0.001N_{std}$	$0.256 + 0.001N_{std}$
		t_{PHL}	$0.595 + 0.001N_{std}$	$0.394 + 0.000N_{std}$	$0.278 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
LT	2.735
PAD (Receiver Input)	233.500
PADN (Receiver Input)	229.500
Internal	139.550
Cell Units	2 cells

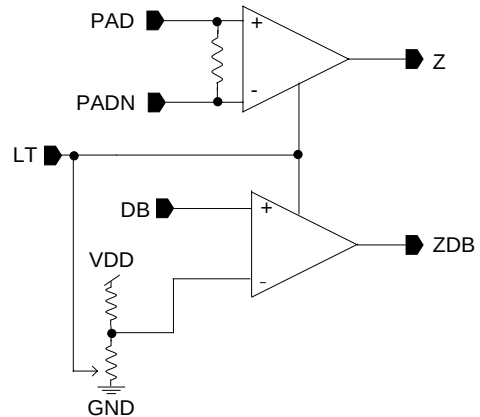
Refer to "PECL Receiver Specifications" on page 134 for more information.

Cell: IPECLDBDT, IPECLDBDT_PM

Function: 1.8V/2.5V PECL Test Differential Receiver w/Termination and PLL Delay Balance

Description:

Noninverting differential receiver used to receive complementary ECL signals referenced to V_{dd250} (2.5V nominal) supply. A second matching single-ended delay block is intended for use with PLLs. The path from DB to ZDB tracks the delay of the PAD/PADN to Z block. All pins exclusive of PAD and PADN are referenced to the V_{dd} supply (1.8V nominal). A differential termination of 100 ohms is inserted between PAD and PADN. The LT pin disables DC current during I_{dd} test.



PAD In-phase drive in

PADN Out-phase driver in

DB Delay block input

LT DC current gate (I_{dd} test) input

Z Receiver out

ZDB Delay block output

Receiver Truth Table

Inputs			Output	Comments
PAD	PADN	LT	Z	
0	1	0	0	Functional mode
1	0	0	1	Functional mode
1	1	0	X	Functional mode
0	0	0	X	Functional mode
-	-	1	PAD	Leakage test

Block Delay Truth Table

Inputs		Output	Comments
DB	LT	ZDB	
0	0	0	Functional mode
1	0	1	Functional mode
-	1	DB	Leakage test

Usage Notes:

1. Normal receiver operation requires a differential input signal of ± 400 mV around a common mode input signal of 2.0V nominal.
2. If the input to the receiver is unknown state (Hi-Z), then the output is indeterminate.
3. During I_{ddq} test, CMOS levels must be applied to PAD.
4. During I_{ddq} test, CMOS levels must be applied to DB.

Receiver Propagation Delays

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (N_{std})		
			$V_{dd} = 1.65V$ $V_{dd250} = 2.3V$ $T_j = 125^\circ C$ Process = Slow	$V_{dd} = 1.8V$ $V_{dd250} = 2.5V$ $T_j = 25^\circ C$ Process = Nom.	$V_{dd} = 1.95V$ $V_{dd250} = 2.7V$ $T_j = 0^\circ C$ Process = Fast
PAD-Z	A	t_{PLH}	$0.557 + 0.001N_{std}$	$0.367 + 0.001N_{std}$	$0.258 + 0.001N_{std}$
		t_{PHL}	$0.596 + 0.001N_{std}$	$0.397 + 0.000N_{std}$	$0.281 + 0.000N_{std}$

Capacitance (in units of N_{std}) and Cell Sizes

Input Pins	Performance Level
	A
DB	21.554
LT	2.735
PAD (Receiver Input)	254.667
PADN (Receiver Input)	251.375
Internal	679.994
Cell Units	2 cells

For more information, see “Other Driver and Receiver Specifications” on page 118.

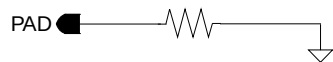
Standard Cell Programmable I/O

Cell: GND_PM_A

Function: Programmable Ground

Description:

The programmable ground is used to allow designated signal pads to be directly connected to ground. When placed in any of the designated I/O cells on an image, it automatically hardwires the ground bus to the signal pad associated with that I/O cell.

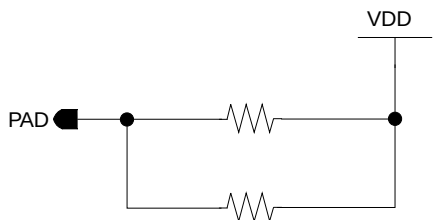


Cell: VDD_PM_A

Function: Programmable 1.8 Volt V_{dd}

Description:

The programmable V_{dd} is used to allow designated signal pads to be directly connected to V_{dd} . When placed in any of the designated I/O cells on an image, it automatically hardwires the V_{dd} bus to the signal pad associated with that I/O cell.

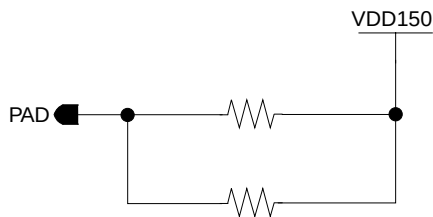


Cell: VDD150_PM_A

Function: Programmable 1.5 Volt V_{dd}

Description:

The programmable V_{dd150} is used to allow designated signal pads to be directly connected to V_{dd150} . When placed in any of the designated I/O cells on an image, it automatically hardwires the V_{dd150} bus to the signal pad associated with that I/O cell.

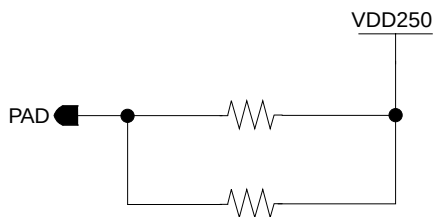


Cell: VDD250_PM_A

Function: Programmable 2.5 Volt V_{dd}

Description:

The programmable V_{dd} is used to allow designated signal pads to be directly connected to V_{dd250} . When placed in any of the designated I/O cells on an image, it automatically hardwires the V_{dd250} bus to the signal pad associated with that I/O cell.

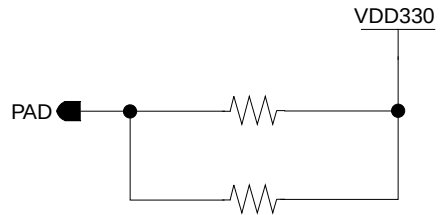


Cell: VDD330_PM_A

Function: Programmable 3.3 Volt V_{dd}

Description:

The programmable V_{dd330} is used to allow designated signal pads to be directly connected to V_{dd330} . When placed in any of the designated I/O cells on an image, it automatically hardwires the V_{dd330} bus to the signal pad associated with that I/O cell.



Glossary

ABIST	Array built-in self-test used in compilable SRAMs.
AFR	Average failure rate (0.0 hours to 40 kPOH) in FITs.
ASIC	Application-specific integrated circuit.
boundary-scan	A design methodology to allow testability of high pin count packages with a low number of primary inputs and outputs.
burn-in	Exercising the circuitry in a high temperature and voltage environment.
cell unit	A unit of area. A cell unit is 1 x 12 wiring channels for non-I/O cells; 120 x 576 for area array I/O cells or 96 x 576 for perimeter I/O cells. Each wiring channel is 0.56 μm wide.
compilable SRAM	A static random access memory circuit that can be compiled to fit size requirements.
DFT	Design-for-test.
DP	Data path.
DSF	Deterministic stuck-fault test.
EFR	Early failure rate (0.0 hours to 1 year of use) in FITs.
EOL	End of life.
FIT	Failures in time; equivalent to ppm/kPOH.
GA	Gate array, an array of background cells that are personalized using only the metal levels of the process.
HyperBGA	High-performance ball grid array

I_{ddq}	Quiescent power supply current.
I/O	Input or output.
internal cells	All cells except I/Os. This includes all primitive cells, all complex cells, all unique cells, and all latch cells. Also referred to as <i>internal logic</i> .
JTAG	Joint Test Action Group. Consortium of companies and universities that defined the IEEE 1149.1 boundary scan standard.
lead	A package input or output.
library	The collection of cells and macros representing the circuits offered by SA-27E.
lm	Last level metal.
LSSD	Level-sensitive scan design: a test methodology supported by SA-27E designs.
macro	A large circuit that can be placed on the chip image; a <i>compilable SRAM</i> or <i>compilable register array</i> , for example.
mz	Last level metal.
nontest I/O	A chip input or output buffer that must be connected to a latch for boundary-scan.
pad	In an input/output cell, the output pin of a driver, and/or the input to the receiver.
pin	A terminal or I/O port on a cell, or a package lead.
PLL	Phase-locked loop.
POH	Power on hours.
RPCT	Reduced pin count testing.
SC	Standard cell, a circuit personalized with diffusion and metal.

test I/O	A chip input or output buffer that does not need to be connected to a latch. This includes all test I/O used for boundary-scan test.
WRP	Weighted random pattern (for test).

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