PROJECT MAC

February 8, 1973

Computer Systems Research Division

Request for Comments No. 8

ASYNCHRONOUS BIT SERIAL INTERFACE -- PRELIMINARY SPECIFICATION

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date 2/12/73

1. General Description

For some time it has been clear that a replacement for the current Multics interface (the GIMPSPIF) to the ARPA Network IMP (Interface Message Processor) would be necessary for use with the 6180 system.

The principal reason for this was the necessity of using a "Distant Host Interface" arrangement since the IMP is to remain at 545 Technology Square whereas Multics will reside in building 39. It has also been concluded that a distant interface will be necessary even when a new IMP is installed in building 39. In addition, it was deemed necessary that the new interface run in a full duplex mode, thereby allowing simultaneous read and write operations.

I am currently designing and building such an interface to be called the Asynchronous Bit Serial Interface (ABSI). Like the GIMPSPIF, the new interface will communicate with Multics via a Common Peripheral Interface (CPI) as defined in Honeywell document number 43A130524, and to the IMP as defined in Bolt Beranek and Newman report 1822. Unlike the GIMPSPIF, two CPI type channels will be needed to allow full duplex operation. One will be used for write operations (HOST to IMP) and the other for read operations (IMP to HOST). The new interface will use the "two way handshake" procedure (see BBN-1822) for communicating with the IMP. The timing will be made slow enough to meet distant host interface requirements but it will be capable of running with either a local or distant interface. This will allow a theoretical maximum transfer rate of about 800,000 bits/sec. in each direction. The ABSI will attempt to meet as closely as possible the CPI specifications. All known exceptions are summarized in section 5 below. It is expected that the interface will operate with any Honeywell 6000 series IOM Common Peripheral Channels.

The following description assumes that the reader is familiar with BBN-1822 and the Common Peripheral Channel specifications and operation. No attempt is made to duplicate the information contained there.

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2. Operation

The new interface will accept the following commands on the "Write Channel":

OPCODE (octal)	MEANING
00	REQUEST STATUS
11	WRITE (start output)
20	HOST UP
40	RESET STATUS
60	HOST DOWN

The "Read Channel" will accept:

OPCODE (octal)	MEANING
00	REQUEST STATUS
01	READ (start input)
40	RESET STATUS

The device code sent as part of the command sequence will be ignored although its parity will be checked.

2.1 Request Status (00 on either channel)

This command will return the same status as the previous command on the same channel. Previous COMMAND REJECT status, however, will be ignored so that if COMMAND REJECT status is received in reply to REQUEST STATUS, it indicates that there was an error in the transmission of the REQUEST STATUS command itself. Note that the status stored may indicate the substatus IMP DOWN even if the IMP has since come up. To correctly obtain the current IMP up/down status, RESET STATUS (see section 2.5) should be used. (A similar condition exists for the substatus HOST DOWN.)

2.2 Read (01 on the read channel)

This command will start reading a message from the IMP. It will terminate under any of the following conditions:

1. The LAST IMP BIT line is received along with a data bit.
2. The host up/down relay is changed to the down state by either of the following:
   a) the manual HOST DOWN pushbutton on the interface
   b) the HOST DOWN command on the write channel

3. The IMP goes down (according to its up/down relay).
4. The channel decided to terminate the command.
   Note that terminate will not actually happen until just after a complete character (6 bits) has been transmitted to the channel. Possible causes are:
   a) The storage buffer indicated in the DATA DCW has been filled and there are no additional DATA DCW's.
   b) The channel is "masked" by the software (see the IOM specifications).
   c) Some other condition occurs which causes masking, such as a second "connect" to the channel before the first list has completed.
5. A "reset" signal is received. This may be created by the manual pushbutton on the ABSI, by disconnection of either of the IOM channels from the interface, by initializing the IOM controlling the channels, or by loss of power to either of the IOM channels. Note that all transmissions are aborted immediately and no status is stored. When the "reset" level is removed, the channel will be ready to accept a new command no matter what it previous state was. The "reset" condition also forces the host up/down relay to open (i.e., HOST DOWN).

In normal operation, only cases 1 (COMPLETE MESSAGE, no errors) and 4a (INCOMPLETE MESSAGE, no errors) should occur. If the latter occurs, the termination status will be READY with substatus INCOMPLETE MESSAGE. The message may be reconstructed by appending the data read by the next READ command to the end of the current data. Unlike the GIMPSPIF, the READY FOR NEXT IMP BIT line is not raised until a read command is issued. Thus there is no way to determine that the IMP has a message waiting until a READ command is issued. It is expected that the software will normally keep a READ command pending at all times that the system is in operation. The expected method for aborting such a read command is to issue a HOST DOWN command on the write channel. If this fails, the HOST DOWN pushbutton on the ABSI should be used. If this also fails, the RESET pushbutton on the ABSI should be tried.

2.3 Write (11 on the write channel)

This command starts writing a message to the IMP. Normally termination will be done only on end of message condition in the buffer. Note, however, that any of the conditions listed in section 2.2 above for aborting the READ command, also apply (except obviously 1 and 2b). The LAST HOST BIT level will

be sent with the last bit transmitted only if termination is caused by the channel rather than the ABSI. Also note that termination under conditions 4b and 4c (the channel becoming masked) will take place only after the next character (6 bits) has been sent to the IMP.

2.4 Host Up (20 on the write channel)

This command causes the HOST MASTER READY line to be connected to the HOST READY TEST line by closing a relay. The software must make sure that no READ or WRITE command is issued to either channel until the relay has had a chance to settle. The delay involved is not here specified, because relay specifications may vary. It is believed, however, that the programmer may assume 100 msec. to be sufficient. This command may be simulated at any time by the manual HOST UP pushbutton.

2.5 Reset Status (40 on either channel)

This command is identical to REQUEST STATUS, except that any resettable status condition from the previous command will be reset. Note that a RESET STATUS command is effectively executed before any command (other than REQUEST STATUS). Resettable status is defined as:

1. any DATA ALERT condition
2. INCOMPLETE MESSAGE substatus
3. IMP DOWN substatus if the IMP is no longer down
4. HOST DOWN substatus if the system is no longer down

2.6 Host Down (60 on the write channel)

This command will open the relay closed by the HOST UP command. If a READ operation is taking place on the read channel, it will be aborted when that channel sees the relay open. It is possible the HOST DOWN command will not take effect if followed too closely by a HOST UP command (i.e., the relay doesn't get a chance to open). Whenever the relay is open (or opening), READ and WRITE commands will be rejected with the status COMMAND REJECT and the substatus HOST DOWN. The HOST DOWN command may be simulated at any time by the manual HOST DOWN pushbutton.

3. Special Interrupts

If the host up/down relay is in the up condition when the IMP comes up (closes its IMP READY relay) then a "special interrupt" will be sent on the READ channel.

4. Status

The following status codes have been defined for the ABSI:

Major Status	Substatus	Meaning
x000		Ready
	xx1xxx	IMP Down
	x1xxxx	HOST Down
	1xxxxx	Incomplete Message
x011		Data Alert
	xxx1xx	Parity Error
	xx1xxx	IMP Down
	x1xxxx	HOST Down
	1xxxxx	Incomplete Message
x101		Command Reject
	xxxxx1	Invalid Operation Code
	xxx1xx	Parity Error in Command Sequence
	xx1xxx	IMP Down
	x1xxxx	HOST Down
	1xxxxx	Incomplete Message
1xxx		Read/Write Command in Progress

Any substatus condition may occur simultaneously with any of the other substatus conditions under the same major status. If this occurs, the appropriate substatus codes will be merged to form the substatus returned.

4.1 Ready Status

The READY status indicates that the channel is ready to accept a command and that no (unreset) errors occurred in the previous command to the channel.

4.1.1 IMP Down Substatus (READY)

The IMP DOWN substatus indicates that the IMP READY relay is open (i.e., the IMP READY TEST line is not connected to the IMP MASTER READY line.) Note, however, that once this bit comes on (i.e., the IMP goes down) it stays on until it is reset by a command other than REQUEST STATUS (e.g., RESET STATUS). Note that this relay, like the host up/down relay, is subject to bounce and so it would be a good idea to wait for the relay to settle before rechecking the status. One could also wait for the special interrupt which says the IMP is up (see section 3 above), but this may be unreliable if one does not carefully consider race conditions. A "timeout" on waiting for the interrupt would therefore be suggested.

4.1.2 Host Down Substatus (READY)

The HOST DOWN substatus indicates in a similar manner that host up/down relay has been, is, or is becoming open.

4.1.3 Incomplete Message Substatus (READY)

The INCOMPLETE MESSAGE substatus may occur only on the READ channel. It indicates that termination occurred before the LAST IMP BIT level was received. Since no bits are lost when this occurs, the entire message may be reconstructed by appending the data read by the next READ command to that read by the most recent READ command.

4.2 Data Alert Status

This status is stored if an error has occurred during the transfer of data in the appropriate direction. Any error will cause the channel to abort the current operation immediately.

4.2.1 Parity Error Substatus (DATA ALERT)

Note that the READ channel will indicate a parity error in the channel status rather than the normal status field since this error is detected by the channel rather than the ABSI. Therefore PARITY ERROR substatus can occur only on the WRITE channel. It indicates that a character has been received from the IOM channel with bad parity. The WRITE command is aborted and the LAST HOST BIT level is not sent to the IMP.

The software may thus indicate to the IMP that this message should be ignored by flashing the HOST UP line (waiting appropriate times for relay closure/opening) and then exchanging a reset sequence with the IMP. (Note that this error recovery procedure will also abort any pending read operations when the HOST DOWN command is executed.)

A much less drastic method for causing the IMP to discard the message in error would be to immediately WRITE a second message whose length is greater than the maximum message length (256 words, for instance, is greater than the current maximum length of 8096 bits). Since the previous WRITE did not have a LAST HOST BIT level sent, this second message will be appended to the first, forcing it to be discarded by the IMP. The original message may then be rewritten as if nothing had happened (assuming no further PARITY ERROR's occur).

It should be noted that the PARITY ERROR substatus normally will happen only if a logic gate fails and so it may actually be reasonable to consider such an error fatal.

4.2.2 IMP Down Substatus (DATA ALERT)

IMP DOWN substatus indicates that the IMP went down at some time during the Read/Write operation. Data may have been lost.

4.2.3 Host Down Substatus (DATA ALERT)

HOST DOWN substatus indicates that the host up/down relay become open (e.g., the HOST DOWN pushbutton was pushed) during the Read/Write operation. Data may have been lost.

4.2.4 Incomplete Message Substatus (DATA ALERT)

INCOMPLETE MESSAGE substatus is solely an indication of whether the LAST IMP BIT level was received before the operation terminated. (It occurs on the READ channel only). This information is actually of little use since data may have been lost due to the error which caused the DATA ALERT status. INCOMPLETE MESSAGE substatus will always occur in conjunction with either HOST DOWN or IMP DOWN when the major status is DATA ALERT.

4.3 Command Reject Status

COMMAND REJECT status indicates that the command could not be accepted for some reason.

4.3.1 Invalid Operation Code Substatus (COMMAND REJECT)

INVALID OPERATION CODE substatus indicates that the command code received by the ABSI was not one of the legal commands for that channel.

4.3.2 Parity Error in Command Sequence Substatus (COMMAND REJECT)

PARITY ERROR IN COMMAND SEQUENCE indicates that either the device code (which is otherwise ignored) or the command code received by the ABSI had bad parity. The command is not executed even if the code is legal.

4.3.3 IMP Down Substatus (COMMAND REJECT)

For all operations except READ and WRITE, this substatus can occur only in conjunction with one of the above two command transmission errors. In this case this status is described in section 4.1.1 above.

For READ and WRITE operations, this substatus indicates that the command could not be initiated because the IMP READY relay is open. Due to timing considerations in the ABSI, the fact that this status is returned does not indicate that the IMP is still down. Therefore, one should do a RESET STATUS command to verify that the IMP is really down. If the RESET STATUS command indicates that it is up, the READ or WRITE command should be reattempted.

4.3.4 Host Down Substatus (COMMAND REJECT)

This substatus is analogous to IMP DOWN substatus in section 4.3.3 above.

4.3.5 Incomplete Message (COMMAND REJECT)

This substatus can only occur in conjunction with one of the two command transmission errors in section 4.3.1 and 4.3.2 above. It is otherwise analogous to the substatus of the same name, described in section 4.2.4 above (and is likewise nearly useless). Note that in this case it refers to the previous READ/WRITE operation, not the rejected one.

4.4 Read/Write Command in Progress

This status indicates that a READ/WRITE command was properly received. It may be returned together with the termination status after a READ/WRITE command has completed (either normally or abnormally). This status is often called CHANNEL/PERIPHERAL SUBSYSTEM BUSY.

5. Exceptions and Assumptions

This section describes all the known assumptions concerning the interfaces with the CPI type channels and with the IMP. Also noted are any exceptions to the specifications.

5.1 Restriction on EDT Transmission on the Write Channel

The WRITE channel must know when it is writing the last bit to the IMP so that it can assert the LAST HOST BIT level. In order to avoid extra buffering and a large increase in complexity, it is necessary that the EDT strobe arrive no more than 4 μsec after the WRITE CLOCK TO PERIPHERAL strobe. This is in spite of the section on Write Command Termination (section 4.3.3, sheet 32) of 43A130524. Honeywell document 43A177715 (the IOM specifications) section A2.3.4.3 states, however, that the IOM CPC sends the EDT .5μsec after the WRITE CLOCK TO PERIPHERAL and so there should be no problem. Since the ABSI is intended for use only with the 6000 IOM, no problems are foreseen.

5.2 Restriction on EDT Transmission on the Read Channel

The READ Channel must know whether the most recent character sent to the channel is to be the last character before it can read the next character from the IMP (because we have decided to eliminate read-ahead which is an unjustifiable complexity). As defined in 43A130524 the EDT strobe may arrive an arbitrary time after the READ CLOCK TO PERIPHERAL strobe. Clearly the ABSI must make some restriction on how long it will wait before reading the next character. For this reason a delay gate with delay time n is used.

The current IOM Common Peripheral Channel villates the standard in 43A130524. It sends the EDT instead of the last READ CLOCK TO PERIPHERAL, rather than after it. The ABSI will work equally well with this situation, and in fact could be simplified. The delay gate has been retained, however, for compatibility, although the capacitance has been set to give a delay time of roughly n=0. Thus, if the channel is changed later to meet the standard, the ABSI may be made compatible simply by changing the capacitance to give a reasonable waiting time.

5.3 Lack of Transfer Timing Error Detection

In spite of section 6.2 (sheet 52) of 43A130524, no provision is made for detecting TRANSFER TIMING ERRORs. This is because the asynchronous nature of the ABSI makes such detection unnecessary; its inclusion would only add nearly useless logic to the interface.

5.4 Definition of Data Transmission Time

In many places 43A130524 specifies times as "sufficient time ...to set ... receivers". It is assumed that 1μsec. is more than sufficient to cover all skew, cable length, and settling time considerations.

5.5 Minimum Buffering Requirements

Section 6.5 of 43A130524 specifies a minimum buffering capability of two characters for the WRITE channel. Only one is provided. Since the ABSI is asynchronous, no problem except a very slight speed loss should be encountered.

5.6 Maintenance Requirements

Section 6.6 of 43A130524 is not met in that neither a Running Hour Clock nor full off-line test facilities have been provided. It is expected that at least an IOM will be available for testing (via the IOM maintenance panel).

5.7 Voltage Levels for the Distant Interface

BBN-1822 specifies ± .5 volt signals for the distant interface connections; the drivers used are closer to ± .75 volt. BBN indicates that this should cause no problem (and, in fact, is probably better).

6. Physical Characteristics

The ABSI is implemented on a single 12" x 12" Honeywell MQX type circuit board. Communication with the two CPI channels is through the two free-edge connectors (one channel on each connector). Communication with the IMP is through the backpanel, using slip over connectors on the backpanel wire-wrap pins. It is required that -5v. be provided to the board through backpanel in addition to the +5v. and ground normally provided. -5v. is not normally connected to the backpanel although it is available in the power supply. A standard wire exists for making the connection. It is expected that the ABSI will work in any slot providing such power and backpanel connections. In particular, it may be mounted in either a 6000 IOM or a DataNet 355 IOM payload slot.

The logic used is Honeywell 500 series (similar to Sylvania SUHL II) with the exception of the distant interface drivers and receivers which are 400 series logic and are similar to the TI SN75108-110 group of integrated circuits.