BB.1

Glossary
Glossary:

Process Control Block:

A stack, stored in the process data segment (p.v.) which is used to store the process state on internal interrupts and faults, and to perform calls while handling interrupts and faults.

S. A. Soloman
6/26/80
Glossary

**External Interrupt:**

An interrupt which comes from an I/O device or other equipment attached to the system. (c/w Internal interrupt)

**Internal Interrupt:**

An interrupt triggered by the operating system directly and directed at the process running on the interrupted processor.

J. M. Salts
6/7/66
Processor Stack:

A stack, stored in the processor data segment (g.v.) used to store the processor state on interrupts, and to perform calls while handling interrupts.
Glossary

Traffic Control:

A term used to describe the operations personnel, interrupts and fault management, scheduling and dispatching.
Glossary

Meter

A term used to describe a core storage cell which is used to accumulate resource usage measurements.

J.A. Saltz
6/7/66
Glossary:

**Inhibit:**

A mode of processor operation in which interrupts (and some faults) are not recognized accepted; they are remembered until the processor leaves the inhibit mode.

**Mask:**

Create a condition such that certain interrupts will be inhibited when they occur. To place a temporary inhibition on selected interrupt sources, see inhibit.

(See Inhibit.)

G. H. Saltz
6/17/66
Glossary:

Interrupt:

The response of a processor to an arbitrarily timed external signal. (cf. fault)

Fault:

The response of a processor to a condition arising within the processor as a result of program execution. (cf. interrupt)

(Note: On the 68000 processor, certain interrupt conditions (connect and power down) are implemented using fault handling; the processor manual describes these as faults.)

J.A. Schildt
6/7/86
System Initialization:

Execution of a sequence of programs which load and initialize a complete running version of Multics, starting with a clear core memory.

A system initialization may or may not include a secondary storage reload.

System Restart:

Execution of a sequence of programs which re-initialize a complete running version of Multics, starting with a booted core memory. System restart may include an effort to salvage whatever information possible from the data base stored in core memory. System restart may be an appropriate action, for example, following a transient hardware fault which causes the system to "hang up".
Standard Section

Processor Identification Number:

An 18-bit string which uniquely identifies the processor. It is composed of an 8-bit type code and a 10-bit serial number concatenated in that order. A 645 processor has type code 001. Other processors will be assigned type codes as necessary.

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J.A. Saltzer
Glossary

Processor Hardware tag:

A wired-in register which identifies the processor. Ideally, it contains the Processor Identification Number. On a 68000 processor the Processor Hardware tag is a 3-bit register.

6/7/86
J.A. Saltzer
Calendar Time:

A signed 71-bit (double-word) integer giving the number of microseconds since 0000 GMT, Jan. 1, 1901.

Calendar Clock:

A centrally located hardware register which contains the current Calendar Time. It is incremented once per microsecond.
Unique Binary Identifier:

A 70-bit string which, by virtue of its method of construction, is guaranteed to be different from every other 70-bit string so constructed. It is composed of the least 52 least significant bits of the current calendar time concatenated with the 18 bits of the current processor number identification number.
Unique ASCII Identifier:

An 11-character string which, by virtue of its method of construction, is guaranteed to be different from every other 11-character string so constructed. It is constructed by converting a unique binary identifier (q.v.) to an integer in the base 89.

The possible values of each digit will be represented by the 94 upper and lower case ASCII graphics, less the vowels A, E, I, O, and U, in a listing sequence.

(Leaving out the vowels guarantees that no random obscenities will be generated.)

<table>
<thead>
<tr>
<th>Remainder in 89</th>
<th>ASCII graphic</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>!</td>
</tr>
<tr>
<td>1</td>
<td>&quot;</td>
</tr>
<tr>
<td>2</td>
<td>#</td>
</tr>
</tbody>
</table>

etc.
Glossary

Execution Timer:

A clock which counts the number of memory cycles used by a processor. A hardware execution timer measures the number of cycles used by the processor for all operations. This hardware timer is used by the supervisor to simulate a processor execution model for every process.