TO: MSPM Distribution

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This BC.1.01 contains several minor typographical corrections, and the addition of a comment about bulk input/output devices.

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Identification

Minimum Configurations and Configuration Restrictions for Multics Operation on the GE-645
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Purpose

This section lists all known restrictions on possible GE-645 hardware configurations which must be observed in order for Multics to 1) operate at all, 2) operate well, and 3) operate continuously. All the restrictions indicated here are reflected in assumptions made by Multics software. Some restrictions may be doubly enforced by hardware limitations also--no distinction is made.

Minimum Configuration (suitable for testing only)

The following items represent the minimum GE-645 hardware configuration on which a Multics supervisor can sustain operation:

- 1. 1 645 Processor
- 2. 1 GIOC containing
 - a. 1 bootload adapter
 - b. 1 communication line adapter
 - c. 1 common peripheral (tape) adapter
- 3. 1 System Controller
- 4. 1 System Clock
- 5. 192K words of addressable memory
- 6. 2 Magnetic Tape Drives (7 or 9 channel)
- 7. 1 Model 37 Teletype or 2741 console
- 8. 1 DSU-10 Disk Storage unit or 1 EMU-302 Drum system

A reel of magnetic tape containing the Multics system is also needed, as well as a supply of blank magnetic tape reels for file system backup.

Note:

It is not suggested that a completely minimum system is either balanced or useful; this list merely serves as a guide to minimum equipment which allows a Multics supervisor to operate at all.

<u>Performance Considerations</u>

As indicated in the note at the end of the above list, the minimum configuration listed above will technically support the Multics supervisor. However, such a minimum system may only be useful for brief tests or experiments because of performance considerations. Although it is recognized that performance aspects of the system vary both with progressive tuning of the supervisor design, and with specific applications or specialized requirements, the following considerations are suggested in configuring a minimum practical system.

- 1. Currently, 256K words of addressable memory are required to avoid excessive paging activity.
- 2. 1 EMU-302 drum system is required to keep secondary storage access from being a limiting bottleneck.
- The number of system controllers must be no fewer than the number of Processors plus the number of MDU-200 drum systems, to avoid excessive interference in access to core memory. If one or more GIOC's are to be driven near their capacity, one additional system controller is needed.
- 4. Some consideration should be given to attachment of additional input/output devices to provide I/O capacity beyond that of the operator's teletype. Interactive users will require additional teletypes. For bulk input and output and batch type usage, one might include line printers, card readers and punches, and magnetic tape capacity beyond the 2 drives required by the system.

Continuous Operation

The configurations listed above do not take into account any attempt to obtain continuous operation. Although Multics is not yet capable of dynamic reconfiguration, which is a prerequisite for true continuous operation, one can describe a somewhat larger minimum hardware complement necessary to allow operation with only brief stops for reconfiguration in case of trouble and preventive maintenance.

If the hardware complement is reduced below this larger complement, preventive maintenance or a single hardware failure can force operation to be discontinued until maintenance is completed or the failure is repaired.

Minimum Configuration for Continuous operation:

- 1. 2 645 processors
- 2. 2 GIOC's, each outfitted as above
- 2 system controllers
- 4. 2 system clocks
- 5. Sufficient core memory that failure of 1 controller will leave at least 192K words of core memory in working controllers. (e.g., 4 64K controllers, 3 128K controllers, or 2 192K controllers)
- 6. 4 Magnetic Tape Drives (7 or 9 channel)
- 7. 2 Model 37 Teletype or 2741 typewriter consoles.
- 8. 2 DSU-10 Disk storage units, or 2 EMU-302 Drum systems, or 1 of each.

(As before, this minimum is technically capable of operating continuously, but may be neither balanced nor useful in a practical sense. As an example, for a 2-processor system to operate near capacity a larger quantity of core memory might be indicated. Also, the above minimum continuous configuration does not consider the question of performance when operating with a partial configuration during preventive maintenance or repair).

Restrictions

The term "all" and "every" used below (e.g. <u>all</u> processors) generally refer to all subject items being used in a logical system with a Multics supervisor in control. It is possible to operate two (or more) Multics supervisors independently on logically independent but electrically connected equipment, provided only that sufficient equipment is available to meet minimum hardware requirements of all of the logical systems. In such cases, the restrictions listed here apply to "all" the equipment within each logical system.

- 1. Every processor must be a control processor for some system controller. It follows that there must be at least as many system controllers as processors. This implication is inconsequential: if there were more processors than system controllers, memory access interference would wash out all of the excess processor capacity.
- 2. Every active device (processor, GIOC, drum) must be able to access every memory location in every system controller. In addition, every active device must use the same address for any given memory location. It follows that cable connections, port selection logic panels and interlace settings on all active devices must be identical.
- 2a. Every processor must be able to address all system clocks, using the same address. (Applicable only to Prototype Clock; this requirement is taken care of by 2, above, when a Production Clock is used.)
- 3. At least one GIOC must contain a bootload channel preset with the program described in section BC.4.01.
- 4. All processors must have the same value in their "processor base address" switches.
- 5. All GIOC's must have "GIOC base address" settings which are different. Similarly for Drums.
- 6. All System Controllers which are interlaced into a group must contain identical amounts of memory.
- 7. If Prototype System Clocks are used, all clock controllers must be given higher priority than all other system controllers.

One performance consideration turns up as a restriction on allowable configurations: to avoid excessive interference in access to core memory, at least 2 - way interlace must be used at all times.