Identification

Fault-Interrupt Hardware Interface
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Purpose

This section provides the specification for the segment which interfaces Multics with the fault-interrupt hardware of the GE-645 processors. This segment, the Processor Base Segment, is a system-wide data base that is shared by all processes running under the same version of Multics.

Hardware Considerations

Each of the 32 faults included in the GE-645 fault repertoire has a corresponding pair of instructions, the fault vector pair, which the processor executes automatically when it generates the fault. The 32 fault vector pairs constitute the processor fault vector, a 64-word block of core memory whose base address is determined by switch settings on the processor maintenance panel. Each of the 32 fault vector pairs has a 5-bit fault code (00000-11111) which the processor uses to locate the fault vector pair for that fault. The 32 fault vector pairs are arranged within the fault vector by increasing fault codes.

Each GE-645 system controller contains 32 execute interrupt cells and a mask register for each of the cells. When an execute interrupt cell is set on by some active device and the associated mask register enables its recognition, the system controller sends an interrupt signal to its control processor. Each of the 32 execute interrupt cells has a corresponding pair of instructions, the interrupt vector pair, which the processor executes automatically when it receives the interrupt signal. The 32 interrupt vector pairs form the 64-word interrupt vector table for that system controller.

Since a GE-645 system may have up to 8 system controllers (prototype clocks are treated as system controllers here), there may be up to 8 interrupt vector tables. The base location of an interrupt vector table is determined by the setting of the processor base switches and the port number (A-H) to which the system controller is attached. The 64-word block of core memory whose base location is given by the processor base switches is occupied by the processor fault vector. Successive 64-word blocks following the fault vector are occupied by the interrupt vector tables for the system controllers attached to ports A, B, ..., H, respectively.

When the GE-645 processor control unit detects a fault condition or accepts an interrupt, it takes a "snapshot" of its internal status and aborts the entire processor. At the end of the abort cycle, the processor executes the processor fault or interrupt

vector pair that corresponds to the condition causing the fault
or interrupt. It is important to note that the instruction pair
executed as a result of the fault or interrupt must execute with
the "inhibit interrupts" bit on if further interrupts are to be
prevented.

Discussion

During Multics system initialization, the fault and interrupt
vector pairs are set by the fault and interrupt initializers
(MSPM Sections BL.9.01 and BL.9.02) to store the processor
control unit in a safe place and to transfer control to the
appropriate procedure for handling the fault or interrupt.
(Usually, the processor control unit is stored in the process
concealed stack or the processor stack and control is transferred
to the fault interceptor or the interrupt interceptor.)   In
general, the fault and interrupt vector pairs are of the
following form.

```
      even
      inhibit          on
      scu              a,*      control unit into safe place
      tra              b,*      transfer to entry point
```

Two points should be noted.   First, the fault and interrupt
vectors are relocated by the processor base switches; the fault
and interrupt initializers must know the **absolute** core address
contained in the processor base switches.   Second, the fault and
interrupt vector instruction pairs reference segments that belong
   the running process, indirectly, through 72-bit ITS-pointers.
The fault and interrupt initializers must know the **absolute** core
address of the ITS-pointers in order to correctly fabricate the
fault and interrupt vector pairs.

During its execution, the bootstrap program (MSPM Section
BL.4.01) determines the absolute core address contained in the
processor base switches and creates the processor base segment
and its associated entry in the Segment Loading Table.   This
allows the fault and interrupt initializers to reference the
fault and interrupt vectors and associated ITS-pointers by name
and rely on the standard addressing mechanism to supply the
proper absolute address.   The layout of the processor base
segment is as follows:

<fault_vector>|0   base location of fault vector

<fault_vector>|64*i   (i = 1, 2, ..., 8) base location of
                      interrupt vector for system controller i

<fault_vector>|64*9   base location of block containing
                   ITS-pointers used by TRA instructions
                   in fault vector

<fault_vector>|64*10   base location of block containing
                         ITS-pointers used by TRA instructions
                         in interrupt vectors

<fault_vector>|64*11   base location of block containing
                         ITS-pointers used by SCU instructions
                         in fault and interrupt vectors