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Identification

System Controller Addressing Segment
Harlow Frick

Purpose

Instructions which access registers in system controllers (i.e., interrupt cell, interrupt mask, calendar clock and alarm clock registers) do so by execution of a register manipulating instruction (i.e., SMIC, SMCM, RMCM, RCCL, or LACL) with an address which, after appending, port selection, and interlace, turns out to lie in the correct system controller. A programmer cannot know what address to use without detailed information about the current hardware configuration. The System Controller Addressing Segment (SCAS) is constructed at initialization or reconfiguration time in such a way as to guarantee that necessary absolute addresses are found at predictable positions in it.

The only intended use for SCAS is reference by ITS pairs in the System Communication Segment (BK.4.01) and the Clock Addressing Segment (BK.4.03). Therefore, only system programmers who initialize or modify the System Communication Segment or the Clock Addressing Segment need be aware that SCAS exists; others need read no further.

Discussion

SCAS contains one 64 word page for each system controller. The pages are slave access, read-only data, in all rings. Since these pages are expected to be referenced only by instructions which access system controller registers, rather than memory locations, the contents are irrelevent unless accessed by mistake. Data in the pages will in fact be initialized to a characteristic pattern to help debugging of programs which read the data by mistake, but users should not make any use of this fact.

SCAS also contains a page table word (PTW) for each prototype system clock. However, pages defined by PTWs for prototype system clocks do not, in fact, exist because prototype system clocks are housed in system controllers which do not contain any memory. An attempt to access memory, using a prototype system clock PTW, will result in a parity fault.

Only the first eight PTWs of SCAS are used. The first PTW is for the system controller or prototype system clock connected to port A of all processors, the second PTW is for processor ports B, etc. PTWs for unused processor ports, and for the 9th through 64th PTWs, will generate a no access fault if referenced.

Pointers in the System Communication Segment and the Clock Addressing Segment reference PTWs in SCAS by means of ITS pairs having the following format:

SCAS segment no.	ITS
n*64	

where n is the index into the SCAS page table.