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Identification

Initialization Constants Table
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Purpose

The initialization constants table is a data base used exclusively by the Multics initializer. It contains information which is generated early in the initialization sequence and which is used later in the sequence. The table thus acts as a convenient storage area and saves the necessity of transferring the information from one procedure to the other until it is needed.

This section contains a short description of the contents of the table followed by an EPL declaration for the table.

Contents of the Initialization Constants Table

1. The correspondence between processor tags and memory ports, referenced by tags. (tag.port)

2. The contents (bits 1-35) of the processor data switches. (switches)

3. The base address (bootload_cpu_base) of the bootload processor. This defines the base location of the fault vector. (BK.1.04)

4. The base address of the GIOC (bootload_gioc_base). This address defines the base location of all the mailboxes used by the bootload GIOC.

5. The memory port number of the bootload GIOC. (bootload_gioc_port)

6. Processor tag (bootload_cpu_tag). This is the unique 3-bit number associated with the bootload processor. (See BC.3.01)

7. The GIOC Channel number at which the operator's teletype is located.

8. Calendar time of the issue of the Multics System Tape (sys_date). This date will be filled in by the Multics System Tape Generator (MSTG).

9. The index of the controller which directs interrupts to the bootload cpu (i_bootload_contr). This is provided by mmct_init_2 and used by scas_init and by mailbox_1_init.

10. The index of the controller where the interrupts from the second gioc are directed (i_interrupt_contr). It is provided by mmct_init_2 and used by scas_init and by mailbox_1_init.

11. Information about interrupts for scs_hlr_init, provided by scs_init. (scs_ut).

EPL Declaration

```
dcl 1 initialization_constants$tag ext,
      2 port (0:7) bit(3),     /*port number of processor tag*/

      initialization_constants$switches bit(35) ext,
                               /*contents of processor data
                                 switches 1-35*/

      initialization_constants$bootload_cpu_ptr ptr ext,
                               /*base address of bootload
                                 processor*/

      initialization_constants$bootload_gioc_ptr ptr ext,
                               /*base address of bootload gioc*/

      initialization_constants$bootload_gioc_port fixed bin(3)ext,
                               /*port number of bootload gioc*/

      initialization_constants$bootload_cpu_tag fixed bin (3) ext,
                               /*processor tag number*/

      initialization_constants$op_telet_ch_no fixed bin (9) ext,
                               /*gioc channel number*/

      initialization_constants$sys_date bit(72) ext,
                               /*date of system tape issue*/

      initialization_constants$i_bootload_contr fixed bin (17)ext,
                               /*index of controller directing
                                 interrupts to bootload cpu*/

      initialization_constants$i_interrupt_contr fixed bin(17)ext,
                               /*index of controller where
                                 interrupts from second gioc are
                                 directed*/

      initialization_constants$scs_ut (0:31) bit (12) ext;
                               /*info about interrupts for
                                 scs_hlr_init*/
```