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Identification

Overview of Off-line Test and Diagnostic Operation
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Purpose

This section is included as a reference which describes the off-line T and D system currently in use at prototype 645 installations.

Introduction

The off-line T and D system is contained on two reels of magnetic tape, one containing the Prototype 645 Processor and Memory T and D, and the other containing the Prototype 645 Peripheral T and D. The contents and operation of these two tapes are described in the following two sections.

Prototype 645 Processor and Memory T and D

Each of the following programs is normally executed in the sequence listed. Execution time is about two minutes plus an additional three hours if the random instruction sequence test is allowed to run to completion.

1. Configuration/Boot Load Program (GEFIG) 645/GIOC

This program provides a common program and procedure for boot loading and making configuration table changes for both the processor memory and I/O T and D system tapes using the 645/GIOC.

The GEFIG program is contained in one binary record on tape (boot record) and one binary card. The binary card is used only when configuration table updating or tape generation is required. The binary card is not required for normal system testing.

The tape record contains the actual configuration table and all programs necessary for updating the table via card reader or console and either continuing the system test or generating a new system tape with updated configuration table.

2. Confidence Records

The confidence records pretest a subset of instructions and basic operations required for further programmed testing of the processor. An error occurring in this test causes the processor to halt. Error information is limited to panel displays and supporting documentation.

3. Utility Package

Control Program for all following Processor/Memory tests. The Utility Package loads in individual test programs and transfers control to them on sensing a transfer record. It includes:

1. Fault and interrupt processing routines
2. Input/Output subroutine
3. A selective memory dump
4. A general error routine
5. A program tape update routine
6. A search for test option

4. Repertoire Tests

The major portion of the 645 instruction repertoire is tested in the "Repertoire" test. Error information consists of printouts showing the command, test number, register in error, erroneous result and the expected result, plus all of the data used to set up the test.

5. Special Tests

The "Special" tests cover hardware functions concerned with address modification, Master/Slave modes of processor operation, conditions of instruction overlap, and automatic faulting. Error information for special tests consists of a statement of the function which failed and detailed information of the test parameters.

6. 645 Special Tests

All remaining 645 functions are tested in this group of tests. Error information consists of printouts showing pertinent parameters associated with the test which failed. Most of these tests are so complicated that the printed error information does not sufficiently tell what happened. Therefore a detailed prose description of each test is provided to familiarize the debugger with a test when it fails.

7. System Controller Test

A memory system survey is first made which determines the number of system controllers, their size and speed, size of execute interrupt registers, and processor address reassign switch settings for visual verification. This survey is then followed by a complete test of the available controller registers and their functions.

8. Memory Core Test

Complete core tests for both linear select and coincident current core stacks are included. The test automatically adjusts itself to any system controller configuration and proceeds to test all core locations, or testing may be selected for a specific core configuration.

9. 645 Random Instruction Sequence Test

The purpose of this program is to confirm that instructions perform independently of preceding and following instructions. The following steps summarize the program operation.

a. Seven instructions are generated in a pseudo-random sequence. Certain of the instruction repertoire are excluded and all instructions causing a transfer of program control are forced to the following adjacent memory address. Instructions 3 and 6 have controlled IT indexing.

b. All program accessible registers, indicators and accumulators are initialized to unique values. The string of instructions is first executed from adjacent memory addresses and, the gross results stored.

c. Next comes a second initialization, followed by execution of the instructions from isolated memory addresses and storage of the gross results.

d. Finally the results are compared and any unforeseen difference causes an error printout.

e. Steps a, through d, are repeated (using 7 different instructions) until the program is terminated. SW 8 causes termination.

Prototype 645 Peripheral I and D

Normal operation consists of booting in GEFIG (previously described in this section) which reads and transfers control to the Monitor. The operator then makes console requests in order to execute one or several test programs. The Monitor executes entirely in absolute mode while the test programs are usually executed in slave mode. The primary purpose of this tape is for testing peripheral devices and the GIOC. The running time is approximately 5 minutes for level 1, 2 minutes for level 2, and 5 to 10 minutes for level 3. The following programs are on the tape:

1. GEFIG (previously described in this section)

2. Control Program (Monitor 5)

3. Slave mode peripheral device tests organized as follows:

   Level 1 - Simple peripheral device tests.

   There is one level 1 program for each common peripheral device and one for the EMM. Each program may operate singly or in a multiprogrammed environment with other level 1 or level 3 programs.

   Level 2 - Comprehensive EMM Test.

   Operates in uniprogram environment. Complete logical test of EMM, except that read and write operation is only on the first and last two EMM sectors.

   Level 3 - Comprehensive peripheral device tests.

   There is one level 3 program for each common peripheral plus one for the EMM. Each program may be executed singly or in a multiprogrammed environment with other level 3 or Level 1 programs.

   Level 4 - Timing Tests.

   One for each common peripheral plus one for the EMM. Must operate in uniprogram environment.

   Level 5 - Manual Intervention Tests.

   One for each common peripheral plus one for the EMM. Level 5 tests for the DSU and EMM read and write on the entire device. Also, several Level 5 programs are provided for testing GIOC communications channels.

4. GIOC Test

   The GIOC test runs in absolute mode and is written in the following seven series. Total running time varies depending on the test sequence selected but is usually between 2 and 10 minutes.

   a. 100 Series - Test GIOC Controller only.

   Checks exhaust status storage from CPW for all combinations of connect channels and status channels. Checks the correct operation of status control words in various combinations and some control word faults. Total of 85, subtests.

   b. 200 Series - Test controller and communications adapter.

Checks terminate and internal status storage for all combinations of connect and status channels. Checks functions of List Service and some of the DCW's associated with IOC simulation. Total of 61, sub-tests.

c. 300 Series - Test controller and communications adapter with back-to-back cable.

Checks external status storage for all combinations of connect and status channels. Checks all Data Control Word functions except control character and character match. Total of 47, sub-tests.

d. 400 Series - Test controller and communications adapter with two channels connected with back-to-back cables.

Checks data transfer and the remaining Data Control Word functions. Total of 20 sub-tests.

e. 500 Series - Command functional test for Communications adapter with back-to-back cable.

Checks status received from all combinations of command bits. Provides the capability of requesting a particular command for scoping purposes. Total of 3, sub-tests.

f. 600 Series - Test Controller and indirect common peripheral adapter.

Checks data transfer and status using a printer. Checks all functions of multiple record mode and various combinations of even, odd address locations and word tallys. Total of 22 sub-tests.

g. 700 Series - Test controller and direct common peripheral adapter. Same as the 600 Series with the addition of magnetic tape. Total of 25 sub-tests.

5. Utility programs including the following:

a. Program Tape Maintenance Routine

b. TDL - Test and Diagnostic Language compiler which accepts, compiles, and executes input only from the operators console or a card reader. (Similar to DIAL described in section BR.2.00.)