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**EDUCATION** **Ph.D. in Electrical Engineering**, August 2012  
*Stanford University*  
**M.Sc. in Electrical Engineering**, April 2009  
*Stanford University*  
**International Exchange ECE Student**, 2006–2007  
*University of Wisconsin-Madison*  
**Telecommunication Engineering Degree**, August 2007  
*Technical University of Madrid (UPM), Spain*

**HONORS AND AWARDS** IEEE Micro Top Picks Award – 2021  
Louis D. Smullin ('39) Award for Excellence in Teaching – 2020  
Google Faculty Research Award – 2019  
Inducted to MICRO Hall of Fame – 2018  
Two IEEE Micro Top Picks Honorable Mentions – 2017  
IEEE Micro Top Picks Award – 2016  
Best Paper Award at MICRO-48 – 2015  
NSF CAREER Award – 2015  
Google Faculty Research Award – 2014, 2015 (awarded twice)  
TIBCO Career Development Professorship, 2012-2015 – Cambridge, 2012  
IEEE Micro Top Picks Award – 2012  
Hewlett-Packard Stanford School of Engineering Fellowship 2009-2012 – Stanford, 2009  
Spanish National Award in Telecommunication Engineering, third place (awarded among top graduating students of all Spanish universities) – Madrid, 2009  
Fundacion Caja Madrid Fellowship for graduate studies 2007–2009 – Madrid, 2007  
Vodafone Spain Scholarship for U.S. exchange students – Madrid, 2006  
Best first-cycle (first three-year) academic record of the School of Telecommunication Engineering at UPM award – Madrid, 2005  
Government of Madrid Excellent Academic Performance Scholarship – Madrid, 2002–2006 (awarded four times)

**WORK EXPERIENCE** **Associate Professor with Tenure**, July 2019–present  
**Associate Professor without Tenure**, July 2017–June 2019  
**Assistant Professor**, September 2012–June 2017  
*Electrical Engineering and Computer Science Department, Massachusetts Institute of Technology, Cambridge MA*  
**Research Assistant**, June 2008–August 2012  
*Computer Systems Laboratory, Stanford University, Stanford CA*  
**Software Engineering Intern**, October–November 2011  
*Cluster Management Group, Google Inc., Mountain View CA*

**Graduate Technical Intern**, June–September 2010

*MPR-PAR, Intel Labs, Santa Clara CA*

**Research Assistant**, February–August 2007

*Computer Science Department, University of Wisconsin-Madison, Madison WI*

**TEACHING  
EXPERIENCE**

Instructor (with Joel S. Emer and Mengjia Yan), 6.823 “Computer System Architecture,” MIT EECS, Spring 2021, Spring 2020, Spring 2019, Spring 2017, Spring 2016, Spring 2015, Spring 2014

Instructor (with Chris J. Terman, Silvina Hanono Wachman, and Arvind), 6.004 “Computation Structures,” MIT EECS, Fall 2020, Fall 2019, Fall 2018, Spring 2018, Fall 2017, Fall 2015, Fall 2014, Fall 2013

Instructor (with Joel S. Emer), 6.888 “Parallel and Heterogeneous Computer Architecture,” MIT EECS, Spring 2013

Instructor (recitations), 6.004 “Computation Structures,” MIT EECS, Fall 2012

Teaching Assistant, EE382A “Advanced Processor Architecture,” Stanford University, Spring 2009

**CONFERENCE  
PAPERS**

Yifan Yang, Joel S. Emer, **Daniel Sanchez**, “SpZip: Architectural Support for Effective Data Compression In Irregular Applications”, In *Proc. of the 48th International Symposium in Computer Architecture (ISCA-48)*, June 2021

Ajay Brahmakshatriya, Emily Furst, Victor Ying, Claire Hsu, Changwan Hong, Max Ruttenberg, Yunming Zhang, Tommy Jung, Dustin Richmond, Michael Taylor, Julian Shun, Mark Oskin, **Daniel Sanchez**, Saman Amarasinghe, “Taming the Zoo: A Unified Graph Compiler Framework for Novel Architectures”, In *Proc. of the 48th International Symposium in Computer Architecture (ISCA-48)*, June 2021

Po-An Tsai, Andres Sanchez, Christopher W. Fletcher, **Daniel Sanchez**, “Leaking Secrets Through Compressed Caches”, In *IEEE Micro’s Top Picks from the Computer Architecture Conferences*, May/June 2021

Guowei Zhang, Nithya Attaluri, Joel S. Emer, **Daniel Sanchez**, “Gamma: Leveraging Gustavson’s Algorithm to Accelerate Sparse Matrix Multiplication”, In *Proc. of the 26th international conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-26)*, April 2021

Quan M. Nguyen, **Daniel Sanchez**, “Pipette: Improving Core Utilization on Irregular Applications through Intra-Core Pipeline Parallelism”, In *Proc. of the 53rd annual IEEE/ACM international symposium on Microarchitecture (MICRO-53)*, October 2020

Charles E. Leiserson, Neil C. Thompson, Joel S. Emer, Bradley C. Kuszmaul, Butler W. Lampson, **Daniel Sanchez**, Tao B. Schardl, “Theres plenty of room at the Top: What will drive computer performance after Moore’s law?”, *Science*, 368(1079), June 2020

Victor A. Ying, Mark C. Jeffrey, **Daniel Sanchez**, “T4: Compiling Sequential Code for Effective Speculative Parallelization in Hardware”, In *Proc. of the 47th International Symposium in Computer Architecture (ISCA-47)*, June 2020

Maleen Abeydeera, **Daniel Sanchez**, “Chronos: Efficient Speculative Parallelism for Accelerators”, In *Proc. of the 25th international conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-25)*, March 2020

Po-An Tsai, Andres Sanchez, Christopher W. Fletcher, **Daniel Sanchez**, “Safecracker: Leaking Secrets Through Compressed Caches”, In *Proc. of the 25th international conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-25)*, March 2020 (*selected for IEEE Micros Top Picks special issue of “most significant papers in computer architecture based on novelty and long-term impact” from 2020*)

Elliot Lockerman, Axel Feldmann, Mohammad Bakhshalipour, Alexandru Stanescu, Shashwat Gupta, **Daniel Sanchez**, Nathan Beckmann, “Livia: Data-Centric Computing Throughout the

- Memory Hierarchy”, In *Proc. of the 25th international conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-25)*, March 2020
- Anurag Mukkara, Nathan Beckmann, **Daniel Sanchez**, “PHI: Architectural Support for Synchronization- and Bandwidth-Efficient Commutative Scatter Updates”, In *Proc. of the 52nd annual IEEE/ACM international symposium on Microarchitecture (MICRO-52)*, October 2019
- Guowei Zhang, **Daniel Sanchez**, “Leveraging Caches to Accelerate Hash Tables and Memoization”, In *Proc. of the 52nd annual IEEE/ACM international symposium on Microarchitecture (MICRO-52)*, October 2019
- Po-An Tsai, **Daniel Sanchez**, “Compress Objects, Not Cache Lines: An Object-Based Compressed Memory Hierarchy”, In *Proc. of the 24th international conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-XXIV)*, April 2019
- Anurag Mukkara, Nathan Beckmann, Maleen Abeydeera, Xiaosong Ma, **Daniel Sanchez**, “Exploiting Locality in Graph Analytics through Hardware-Accelerated Traversal Scheduling”, In *Proc. of the 51th annual IEEE/ACM international symposium on Microarchitecture (MICRO-51)*, October 2018
- Po-An Tsai, Yee Ling Gan, **Daniel Sanchez**, “Rethinking the Memory Hierarchy for Modern Languages”, In *Proc. of the 51th annual IEEE/ACM international symposium on Microarchitecture (MICRO-51)*, October 2018
- Po-An Tsai, Changping Chen, **Daniel Sanchez**, “Adaptive Scheduling for Systems with Asymmetric Memory Hierarchies”, In *Proc. of the 51th annual IEEE/ACM international symposium on Microarchitecture (MICRO-51)*, October 2018
- Mark C. Jeffrey, Victor A. Ying, Suvinay Subramanian, Hyun Ryong Lee, Joel Emer, **Daniel Sanchez**, “Harmonizing Speculative and Non-Speculative Execution in Architectures for Ordered Parallelism”, In *Proc. of the 51th annual IEEE/ACM international symposium on Microarchitecture (MICRO-51)*, October 2018
- Xiangyao Yu, Yu Xia, Andrew Pavlo, **Daniel Sanchez**, Larry Rudolph, Srinivas Devadas, “Sundial: Harmonizing Concurrency Control and Caching in a Distributed OLTP Database Management System”, In *Proc. of the VLDB Endowment (PVLDB)*, June 2018
- Nosayba El-Sayed, Anurag Mukkara, Po-An Tsai, Harshad Kasture, Xiaosong Ma, **Daniel Sanchez**, “KPart: A Hybrid Cache Partitioning-Sharing Technique for Commodity Multicores,” In *Proc. of the 24th international symposium on High Performance Computer Architecture (HPCA-24)*, February 2018
- Xu Ji, Chao Wang, Nosayba El-Sayed, Xiaosong Ma, Youngjae Kim, Sudharshan Vazhkudai, Wei Xue, **Daniel Sanchez**, “Understanding Object-level Memory Access Patterns Across the Spectrum: Are HPC Applications Any Different?,” In *Proc. of the 2017 ACM/IEEE International Conference on High Performance Computing, Networking, Storage and Analysis (SC17)*, November 2017
- Sabrina Neuman, Jason Miller, **Daniel Sanchez**, Srinivas Devadas, “Using Application-Level Thread Progress Information to Manage Power and Performance,” In *Proc. of the 35th IEEE International Conference on Computer Design (ICCD-35)*, November 2017
- Po-An Tsai, Nathan Beckmann, **Daniel Sanchez**, “Nexus: A New Approach to Replication in Distributed Shared Caches,” In *Proc. of the 26th international conference on Parallel Architectures and Compilation Techniques (PACT-26)*, September 2017
- Maleen Abeydeera, Suvinay Subramanian, Mark C. Jeffrey, Joel Emer, **Daniel Sanchez**, “SAM: Optimizing Multithreaded Cores for Speculative Parallelism,” In *Proc. of the 26th international conference on Parallel Architectures and Compilation Techniques (PACT-26)*, September 2017
- Suvinay Subramanian, Mark C. Jeffrey, Maleen Abeydeera, Hyun-Ryong Lee, Victor Ying, Joel Emer, **Daniel Sanchez**, “Fractal: An Execution Model for Fine-Grain Nested Speculative Parallelism,” In *Proc. of the 44th annual International Symposium in Computer Architecture (ISCA-44)*, June 2017

- Po-An Tsai, Nathan Beckmann, **Daniel Sanchez**, “Jenga: Sidestepping the Performance-Energy Tradeoff through Software-Defined Cache Hierarchies,” In *Proc. of the 44th annual International Symposium in Computer Architecture (ISCA-44)*, June 2017
- Nathan Beckmann, **Daniel Sanchez**, “Maximizing Cache Performance Under Uncertainty,” In *Proc. of the 23rd international symposium on High Performance Computer Architecture (HPCA-23)*, February 2017
- Mark C. Jeffrey, Suvinay Subramanian, Maleen Abeydeera, Joel Emer, **Daniel Sanchez**, “Data-Centric Execution of Speculative Parallel Programs,” In *Proc. of the 49th annual IEEE/ACM international symposium on Microarchitecture (MICRO-49)*, October 2016 (*IEEE Micro’s Top Picks 2016 Honorable Mention*)
- Guowei Zhang, Virginia Chiu, **Daniel Sanchez**, “Exploiting Semantic Commutativity in Hardware Speculation,” In *Proc. of the 49th annual IEEE/ACM international symposium on Microarchitecture (MICRO-49)*, October 2016 (*IEEE Micro’s Top Picks 2016 Honorable Mention*)
- Harshad Kasture, **Daniel Sanchez**, “TailBench: A Benchmark Suite and Evaluation Methodology for Latency-Critical Applications,” In *Proc. of the IEEE International Symposium on Workload Characterization (IISWC)*, September 2016 (*best paper nominee*)
- Mark C. Jeffrey, Suvinay Subramanian, Cong Yan, Joel Emer, **Daniel Sanchez**, “Unlocking Ordered Parallelism with the Swarm Architecture,” In *IEEE Micro’s Top Picks from the Computer Architecture Conferences*, May/June 2016
- Xiangyao Yu, Andrew Pavlo, **Daniel Sanchez**, Srinivas Devadas, “TicToc: Time-Traveling Optimistic Concurrency Control,” In *Proc. of the 2016 ACM SIGMOD/PODS conference*, June 2016
- Anurag Mukkara, Nathan Beckmann, **Daniel Sanchez**, “Whirlpool: Improving Dynamic Cache Management with Static Data Classification,” In *Proc. of the 21st international conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-XXI)*, April 2016
- Nathan Beckmann, **Daniel Sanchez**, “Modeling Cache Performance Beyond LRU,” In *Proc. of the 22nd international symposium on High Performance Computer Architecture (HPCA-22)*, March 2016
- Guowei Zhang, Webb Horn, **Daniel Sanchez**, “Exploiting Commutativity to Reduce the Cost of Updates to Shared Data in Cache-Coherent Systems,” In *Proc. of the 48th annual IEEE/ACM international symposium on Microarchitecture (MICRO-48)*, December 2015 (*Best Paper Award*)
- Mark C. Jeffrey, Suvinay Subramanian, Cong Yan, Joel Emer, **Daniel Sanchez**, “A Scalable Architecture for Ordered Parallelism,” In *Proc. of the 48th annual IEEE/ACM international symposium on Microarchitecture (MICRO-48)*, December 2015 (*selected for IEEE Micro’s Top Picks special issue of “most significant papers in computer architecture based on novelty and long-term impact” from 2015*)
- Harshad Kasture, Davide B. Bartolini, Nathan Beckmann, **Daniel Sanchez**, “Rubik: Fast Analytical Power Management for Latency-Critical Systems,” In *Proc. of the 48th annual IEEE/ACM international symposium on Microarchitecture (MICRO-48)*, December 2015
- Christina Delimitrou, **Daniel Sanchez**, Christos Kozyrakis, “Tarcil: Reconciling Scheduling Speed and Quality in Large Shared Clusters,” In *Proc. of the Sixth ACM Symposium on Cloud Computing (SOCC)*, August 2015
- Nathan Beckmann, Po-An Tsai, **Daniel Sanchez**, “Scaling Distributed Cache Hierarchies through Computation and Data Co-Scheduling,” In *Proc. of the 21st international symposium on High Performance Computer Architecture (HPCA-21)*, February 2015 (*best paper award nominee*)
- Nathan Beckmann, **Daniel Sanchez**, “Talus: A Simple Way to Remove Cliffs in Cache Performance,” In *Proc. of the 21st international symposium on High Performance Computer Architecture (HPCA-21)*, February 2015
- Harshad Kasture, **Daniel Sanchez**, “Ubik: Efficient Cache Sharing with Strict QoS for Latency-

Critical Workloads,” In *Proc. of the 19th international conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-XIX)*, March 2014

Nathan Beckmann, **Daniel Sanchez**, “Jigsaw: Scalable Software-Defined Caches,” In *Proc. of the 22nd international conference on Parallel Architectures and Compilation Techniques (PACT-22)*, September 2013

**Daniel Sanchez**, Christos Kozyrakis, “ZSim: Fast and Accurate Microarchitectural Simulation of Thousand-Core Systems,” In *Proc. of the 40th annual International Symposium in Computer Architecture (ISCA-40)*, June 2013

**Daniel Sanchez**, Christos Kozyrakis, “Scalable and Efficient Fine-Grained Cache Partitioning with Vantage,” In *IEEE Micro’s Top Picks from the Computer Architecture Conferences*, May/June 2012

**Daniel Sanchez**, Christos Kozyrakis, “SCD: A Scalable Coherence Directory with Flexible Sharer Set Encoding,” In *Proc. of the 18th international symposium on High Performance Computer Architecture (HPCA-18)*, February 2012

**Daniel Sanchez**, David Lo, Richard M. Yoo, Jeremy Sugerman, Christos Kozyrakis, “Dynamic Fine-Grain Scheduling of Pipeline Parallelism,” In *Proc. of the 20th international conference on Parallel Architectures and Compilation Techniques (PACT-20)*, October 2011

**Daniel Sanchez**, Christos Kozyrakis, “Vantage: Scalable and Efficient Fine-Grain Cache Partitioning,” In *Proc. of the 38th annual International Symposium in Computer Architecture (ISCA-38)*, June 2011 (selected for *IEEE Micro’s Top Picks special issue of “most significant papers in computer architecture based on novelty and long-term impact” from 2011*)

**Daniel Sanchez**, Christos Kozyrakis, “The ZCache: Decoupling Ways and Associativity,” In *Proc. of the 43rd annual IEEE/ACM international symposium on Microarchitecture (MICRO-43)*, December 2010

George Michelogiannakis, **Daniel Sanchez**, William J. Dally, Christos Kozyrakis, “Evaluating Bufferless Flow Control for On-Chip Networks,” In *Proc. of the 4th ACM/IEEE international symposium on Networks-on-Chip (NOCS-2010)*, May 2010 (best paper award candidate)

**Daniel Sanchez**, Richard M. Yoo, Christos Kozyrakis, “Flexible Architectural Support for Fine-Grain Scheduling,” In *Proc. of the 15th international conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-XV)*, March 2010

**Daniel Sanchez**, Luke Yen, Mark D. Hill, Karthikeyan Sankaralingam, “Implementing Signatures for Transactional Memory,” In *Proc. of the 40th annual IEEE/ACM international symposium on Microarchitecture (MICRO-40)*, December 2007

## JOURNAL PAPERS

Guowei Zhang, **Daniel Sanchez**, “Leveraging Hardware Caches for Memoization,” *Computer Architecture Letters (CAL)*, 2018

Nathan Beckmann, **Daniel Sanchez**, “Cache Calculus: Modeling Caches through Differential Equations,” *Computer Architecture Letters (CAL)*, 2016

**Daniel Sanchez**, George Michelogiannakis, Christos Kozyrakis, “An Analysis of Interconnection Networks for Large Scale Chip-Multiprocessors,” *ACM Transactions on Architecture and Code Optimization (TACO)*, Volume 7, Issue 1, April 2010

## THESES

**Daniel Sanchez**, “Hardware and Software Techniques for Scalable Thousand-Core Systems,” *Ph.D. Thesis, Stanford University*, August 2012

## TECHNICAL REPORTS

Nathan Beckmann, Po-An Tsai, **Daniel Sanchez**, “Jenga: Harnessing Heterogeneous Memories through Reconfigurable Cache Hierarchies,” *MIT-CSAIL-TR-2015-035*, December 2015

Nathan Beckmann, **Daniel Sanchez**, “Bridging Theory and Practice in Cache Replacement,” *MIT-CSAIL-TR-2015-034*, December 2015

Nathan Beckmann, **Daniel Sanchez**, “A Cache Model for Modern Processors,” *MIT-CSAIL-TR-2015-011*, April 2015

Nathan Beckmann, **Daniel Sanchez**, “Jigsaw: Scalable Software-Defined Caches (Extended Version),” *MIT-CSAIL-TR-2013-017*, July 2013

**Daniel Sanchez**, “Design and Implementation of Signatures for Transactional Memory Systems,” *University of Wisconsin-Madison Technical Report CS-TR-2007-1611*, September 2007

## **SERVICE**

- Program co-chair for MICRO 2017.
- Program committee member for HotPar 2013, MICRO 2013, PACT 2014, MICRO 2014, HPCA 2015, MICRO 2015, HPCA 2016, Top Picks 2016, ISCA 2017, Top Picks 2018, ISCA 2018, Top Picks 2019, MICRO 2019, MICRO 2020, ASPLOS 2021, Top Picks 2021, MICRO 2021, ASPLOS 2022.
- Distinguished reviewer for ACM TACO 2014.