

CURRICULUM VITÆ

MARCO D. SANTAMBROGIO

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1 PERSONAL DATA

1.1 General data

Name Marco Domenico

Surname Santambrogio

Date of birth November 04, 1977

Place of birth Monza (MI) - Italy

Citizenship Italian

Marital status Married

1.2 Office address

Dipartimento di Elettronica ed Informazione (Department of Electronics and Information)

Via Ponzio 34/5, I-20133, Milano (MI), Italy

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Home page: www.dei.polimi.it/people/santambr

Research group: www.dresd.org

1.3 Academic positions and affiliations

- Academic positions

Since 07/2008 Research Assistant (research program: Metodologie di progetto di sistemi informatici hardware e software. (Design methodologies for hardware and software IT systems.)) at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).

03/2008-07/2008 Research Assistant (research program: Analisi e definizione di possibili scenari applicativi di nuovi sistemi riconfigurabili. (Analysis and definition of applicative scenarios for novel reconfigurable technologies.)) at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).

03/2005-07/2008 PhD Student in the Computer Engineering and Automation program at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milan, Italy).

11/2004-03/2005 Research Assistant (research program: Definizione di un flusso di design per sistemi riconfigurabili basati su FPGA della Xilinx. (Definition of a novel design flow for Xilinx FPGA-based reconfigurable systems.)) at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).

- Affiliations

Since 2008 Member of the IEEE Computer Society (CS)

Since 2008 Member of the IEEE Circuits and Systems Society (CAS)

Since 2005 Member of the Institute of Electrical and Electronic Engineers (IEEE)

Since 2005 Member of the Italian Association of Operations Research (AIRO)

Since 2008 Member of HipEAC, European Network of Excellence on High Performance and Embedded Architecture and Compilation

Since 2008 Member of HiPEAC Reconfigurable Computing Cluster

1.4 Education

February 2008 PhD in Information Engineering

DIPARTIMENTO DI ELETTRONICA ED INFORMAZIONE, POLITECNICO DI MILANO

PhD Thesis: *Hardware/Software codesign methodologies for dynamically reconfigurable systems*.

Advisor: Prof. D. Sciuto. Tutor: Prof. F. Ferrandi

June 2004 Master of Science in Computer Science

UNIVERSITY OF ILLINOIS AT CHICAGO, CHICAGO, ILLINOIS, USA

Master Thesis: *Dynamic Reconfigurability in Embedded System Design. A Model for the Dynamic Reconfiguration*.

Advisor: Prof. John Lillis.

April 2004 Laurea (MSc italian equivalent) in Computer Engineering

POLITECNICO DI MILANO

Thesis: *A Methodology for Dynamic Reconfigurability in Embedded System Design*.

Advisor: Prof. D. Sciuto.

July 1996 Diploma di Maturità Scientifica

High-school diploma specializing in scientific studies

LICEO SCIENTIFICO G. PEANO (Cinisello Balsamo).

1.5 Visiting periods

- MSc Student, University of Illinois at Chicago, 2002
- Visiting researcher, Heinz Nixdorf Institute, January 2006
- Invited researcher, Northwestern University, February - June 2006
- Invited researcher, Northwestern University, April - May 2007

1.6 Other information

07/2005 - 12/2006 Head of the ICT area and member of the managing board of ISF-MI Association.

July 2005 Co-founder of Engineer Without Border Milano (Ingegneria Senza Frontiere ISF-MI).

01/2001- 04/2001 Head of the IT area, for Caritas Ambrosiana and CeLIM, of two humanitarian missions in Kosovo (Jacova e Pristina)

02/2000 - 12/2000 Civil service at CeLIM NGO.

2 SCIENTIFIC ACTIVITIES

2.1 Research interests

2.1.1 Hardware/Software codesign methodologies for dynamically reconfigurable systems

In this research [E.1] I introduce a new design framework which amends this lack. Therefore aim of this research is to define a methodology and design flow, named *earendil* [B.14, B.24, B.18, B.43], for reconfigurable embedded systems which aims at defining a specification-to-bitstream and autonomous design flow based on, where possible, standard tools. The idea behind the proposed methodology [D.1, B.1, B.2, B.5] is based on the assumption that it is desirable to implement a flow that can output a set of configuration bitstreams used to configure and, if necessary, partially reconfigure a standard FPGA to realize the desired system. One of the main strengths of the proposed methodology is its low-level architectural independence. In fact it has been developed using both the Caronte [B.1, B.2, B.4, B.12] and the YaRA (Yet another Reconfigurable Architecture) architecture [F.3], but it can be easily adapted to different architectural and SoC solutions, i.e. the RAPTOR2000 system. The earendil design flow consists mainly of three phases:

- The **High Level Reconfiguration** phase, which is the first step performed in the earendil flow. Its goal is to analyze the input specification in order to find a feasible representation, produced by a first partitioning (cores/functionalities identification) phase, that can be used to perform the hardware/software codesign. In the currently implemented framework, cores are identified by extraction of isomorphic templates used to generate a set of feasible covers of the original specification. Finally, the computed cover is placed and scheduled onto the given device.
- The **Validation** phase. Aim of the *validation* phase is to drive the refinement cycle of the system design [B.11]. Using the information provided by this phase, it is possible to modify the decisions taken in the first part of the flow to improve the development process.
- The last step that has to be performed is the (Low Level Reconfiguration) phase. Goal of this step is the definition of an automatic generation of the low-level implementation of the final solution that has to be physically deployed on the target device and that realizes the original specification [B.8, B.17, B.35, B.39, B.40, B.49].

2.1.2 Placement, partitioning and scheduling of task graphs on partially dynamically reconfigurable architectures

Goal of this research is the creation of a complete theory and workflow [A.2, E.1, B.32, B.46] to help the designer in the specification and management of reconfigurable systems. The provided support is related to the definition of area constraints for tasks [B.38, F.5], reconfiguration specific constraints, like reconfiguration time [A.2, B.16, B.44], manipulation of the input specification, placement assignment [D.3, B.21, B.29, B.46] to each core defining the input specification, partitioning the input specification [B.6] and so forth. The aim is to develop an automated tool capable of helping the designer and prepare the input specification for low level design phases. Moreover, self, partial and dynamical reconfiguration, in both its mono-dimensional (1D) and bi-dimensional (2D) paradigms, gives the possibility of enhancing the flexibility of a reconfigurable system. As we have seen, it is a powerful approach but, at the same time, causes a significant increase in the complexity of system creation and management. Therefore, one of the goals of these studies is to support the designer in creating and managing a reconfigurable system, starting from the higher description of the desired system, to the identification, once the target architecture has been defined, of the online cores placement and in the core relocation support [A.1, B.19, B.35], combining the online cores placement with the runtime bitstreams relocation [A.1] to implement a complete solution that can be used in conjunction with the runtime self reconfiguration.

2.1.3 Scheduling problems with uncertainty conditions

This work starts from the classical resource constrained scheduling problem: a set of tasks has to be executed using a fixed and limited amount of resources. Each task is characterized by a duration (the time required to complete its execution). Precedence constraints ordered pairs of tasks prescribing that the latter must start only after the former has ended. Mapping constraints

define the resource on which each task must be executed. Aim of this research was to introduce two extensions of the previously described framework: *multi-mode execution* and *conditional execution*. With Multi-mode execution, a task can be performed using different alternative resources, having different performances, i.e. execution time. Some tasks must be executed by a specific resource, others can be executed using different resources. While Conditional execution means that not all the tasks must be executed. the execution of a task is subject to the occurrence of an external event, which is unpredictable at the beginning of the schedule. Different event combinations provide different subsets of tasks to be performed, that means different scheduling problems to be solved. The main objective of this research was to minimize the overall execution time [B.7], independently from the events occurred, by applying Integer Linear Programming (ILP) techniques. Different applicative fields [E.1] have been taken into account to prove both the practical relevance of the problem considered and the generality of the proposed approach.

2.1.4 An operating system support runtime management for partially dynamically reconfigurable embedded systems

The increasing amount of programmable logic provided by modern FPGAs makes it possible to execute multiple hardware applications on the same device. This approach is reinforced by dynamic reconfiguration, which allows a single part of the device to be configured with a single hardware module. In this scenario, an operating system can be developed in order to determine where a module should be configured, and to provide an interface towards the final user in order to request a hardware application in a simplified way. The proposed solution is a complete operating system to manage on-demand module configuration on an FPGA while providing a set of high-level abstractions to user applications. The development of an operating system for reconfigurable devices makes the whole system more flexible [B.3], and increases the level of abstractions for the final user [B.50]. The proposed methodology [D.1, B.50] focuses on the extension of a well-known and portable kernel such as GNU/Linux, in order to introduce a support for dynamic reconfiguration and to simplify the interface between the user application and the reconfigurable hardware [B.25]. Each software application, also named *process*, can issue one or more system calls in order to require a specific functionality, which may be available either as a software library, or as a hardware IP-Core, or both. The operating system is in charge of choosing among the software or the hardware implementation according to different criteria, such as the amount of free area on the FPGA. The reconfiguration support in the operating system has been implemented by means of two kernel modules and a reconfiguration library [B.50]. Those three elements are part of a layered structure, in which software applications communicate with the kernel by means of the functions of the reconfiguration library. Until now, the main contributions of this research can be summarized in the following two points: in an extensive and complete design flow for the self reconfiguration of SoC architectures via an extension of a standard operating system like GNU/Linux [D.1, B.25] and in the design of an Operating System solution able to support and manage the reconfiguration both in a SoC [D.1, B.3, B.55] or in Multi-FPGAs scenario [B.23, B.50].

2.1.5 Combining software Adaptive Computation and reconfigurable hardware techniques for exploring novel SoC design solutions

In existing approaches to codesign, the emphasis is placed on identifying computationally intensive tasks, also called kernels, and then maximizing performance by implementing most of these tasks on reconfigurable hardware. In this scenario, software primarily performs the control dominated tasks. The performance model of the reconfigurable hardware is mainly defined by the degree of parallelism available in a given task and the amount of reconfiguration and communication cost that will be incurred. The performance model for software execution is on the other hand static and does not become affected by external factors. The proposed methodology [B.20, B.27] aims to provide the necessary metrics [B.15] and evaluation tools to compare and choose the best implementation within a larger search space that we refer to as the gray area between hardware and software domains. We argue that with the innovations in both software optimization techniques as well as hardware technologies, the codesign task for reconfigurable SoCs will have to navigate a larger gray area than before. We propose to incorporate an effective software optimization technique, based on Adaptive Computing, and the emerging dynamic reconfiguration technology for hardware into one design framework [B.27] and explore the best of both worlds with a novel set of performance metrics and evaluation tools.

2.1.6 Computer architecture and multi-core heterogeneous systems

GPP-based reconfigurable processing elements. FPGAs can be used to create hardware/software platforms that keep their flexibility after deployment, allowing the development of complex *System-on-Chip* (SoC) and reducing the overall number of physical components, since many resources can be configured on request, replacing unused ones. In such a scenario, a larger number of complex components can be mapped at the same time into the same device [B.48]. An emerging design pattern is based on Multi Processing Element. This research focuses its attention on the definition of a Reconfigurable Processing Element based on a Harvard Architecture, called HARPE [B.42]. HARPE's architecture includes a MicroBlaze soft-processor in order to make HARPEs deployable also on devices not having processors on silicon die. In such a context, this work also introduces a novel approach for the management of processor data memory. The proposed approach allows the individual management of data and the dynamic update of the memory [B.31], thus making it possible to define Partially Dynamical Reconfigurable Multi Processing Element Systems, that consist of several master (e.g., soft-processors, hard-processors or HARPE cores) and slave components. Finally, the proposed methodology enables the possibility of creating a system in which both HARPEs and their memories (data and code) can be separately configured at run time with a partial configuration bitstream, in order to make the whole system more flexible with respect to changes occurring in the external environment. This situation will lead to the definition of an adaptable multi-processors reconfigurable architecture.

Design of dedicated CPU for regular expression matching. In many applications, string pattern matching is one of the most intensive task in terms of computation time and memory accesses. Network Intrusion Detection Systems and DNA Sequence Matching are two of those. Since software solutions are not able to satisfy the requirements in terms of performance, specialized hardware architectures are required. In [D.2, B.28] a complete framework for regular expression matching has been proposed. The proposed special-purpose processor, called ReCPU, is programmed using a regular expression programming language. The parallelism adopted in the design grants the possibility to achieve a throughput greater than one character per clock cycle requiring $O(n)$ memory space. The VHDL description of the proposed architecture is fully configurable and the design space exploration to find the optimal architecture based on area and performance cost-function has been presented in [B.45]. The reconfigurable version of ReCPU can be configured on programmable devices such as a FPGAs, with a set of ReCPUs, each one exploiting a single instance of the regular expression matching task on the given input string. These cores work in parallel on the same string analyzing different possible matching of the regular expression. Since the system is able to exploit dynamic partial reconfigurations, it can adapt at run-time the number of cores configured on the device, therefore it is possible to parallelize the regular expression matching process with a multiple cores architecture drastically reducing the time required for the completion of the task (up to one order of magnitude with respect to software solutions and up to a speedup factor of 25 with respect to hardware solutions). Finally, run-time reconfiguration capabilities allow to reduce the amount of resources required by the proposed approach.

Communication infrastructure for reconfigurable architectures. Recent advances in VLSI technology show the limits of the classical computation-centric design paradigm. The ever increasing level of integration and complexity in digital electronic systems requires a communication-centric approach for designing high performance systems, where integrable modules (IP-Cores) require high levels of communication. Classical approaches like bus or point-to-point interconnects are no longer sufficient to ensure and support communication requirements. Buses become a bottleneck with the increasing number of integrable modules, while point-to-point interconnects are only feasible for short range applications. A new relevant approach has been defined, namely Network-on-Chip [B.51], in which theory and applications of well-known data networks are borrowed in the System-on-Chip context. In this scenario, there is an emerging need of having a methodology that supports the designer in the definition of the best fitting communication infrastructure [B.40, B.49]. This scenario can be further extended to support partial dynamic reconfiguration of the Communication Infrastructure (CI), in order to cope either with the changes of the user needs or with the changing environment [B.48].

Multi-FPGAs heterogeneous architecture. In this research we consider multi-FPGAs, re-configuration and system description portability as the processes of specifying and modeling a complete system before it is partitioned and committed to a style/flow of implementation, attempting to obtain a solution which gives the optimal cost, according to a user defined quality of service value, and performance for the application. In the case of a high performance computing

cluster employing FPGAs, the reconfigurable elements need to be dynamically re-allocated and reconfigured based on the prevailing workload at a given instance. We particularly target fast configuration and task migration in high performance computing systems, such as server farms. In this research [B.36], the main emphasis is on correctness and dependability of joining technologies in the hardware and software domains, on the reconfigurable hardware characteristics, on the heterogeneous architectural description, on the satisfaction of quality of service constraints and, in general, on the exploration of the solution space, in order to evaluate the most effective solutions that are compatible. The main goal of this work is the definition of an environment able to serve several applications sharing the same heterogeneous multi-FPGAs physical architecture. In order to meet this goal several aspects need to be taken under consideration i.e. multi-FPGAs solution Vs reconfigurable one, how to characterize the underlying environment to permit the correct application mapping over it.

2.1.7 Research & Education: how to create a win-win game where research and the students experience are positively influenced one other

Research and Education have been often perceived as a dichotomy. It has often been hard to couple them in a productive and virtuous cycle. I believe that Research can obtain great benefits from Teaching and the other way around [B.47]. In particular, involving students in research activities will heavily increase the design and coding power of a research group. On the contrary, from an educative point of view, giving to the student the chance to be involved in real projects will mean giving them the chance to experience real design and development challenges and by guiding them during the design and development we can, in a maieutic way, teach them how to approach real life projects. In such a context it is necessary to provide to the students an environment where they can work and experiment a motivating experience and it is exactly at this point that the DRES project plays a key-role with its activities [see <http://www.dresd.org/DRESDevents> for more information].

2.2 Program committee, conference organization and revision activities

2.2.1 International workshop organization

- **International coordinator**

International Conference on Industrial and Information System, ICIIS 07 Date: August, 2007

Location: University of Peradeniya, Sri Lanka

Conference Chairman: Janaka Ekanayake

Workshop Chairman: Marco D. Santambrogio

Workshop Title: Reconfigurable Computing

2.2.2 Conferences and Journal organization

- **Journal Guest editor** Title: Reconfigurable computing and hardware/software codesign.

Editor: Hindawi Publishing Corporation

Guest editors: T. Plaks, M. D. Santambrogio, D. Sciuto

References: www.hindawi.com/journals/es/si/rcc.pdf

www.hindawi.com/journals/es/raa.731830.html

- **Special session organization at international conferences**

- IEEE International Symposium on Circuits and Systems, ISCAS 07

Date: May, 2007

Location: New Orleans, USA

Conference Chairman: Prof. Magdy Bayoumi, University of Louisiana at Lafayette

Session Organizer: Marco D. Santambrogio, Donatella Sciuto

Session Title: Design Methodology For Partial Dynamic Reconfiguration: A New Degree Of Freedom In The HW/SW Codesign Techniques

- 15th International Conference on Very Large Scale Integration, IFIP VLSI-SoC 2007

Date: October, 2007

Location: Atlanta, USA

Conference Chairman: Vincent John Mooney III

Session Chairman: Marco D. Santambrogio, Jurgen Becker
Session Title: Architecture Design Principles

2.2.3 Program Committee

- IEEE Reconfigurable Architectures Workshop (RAW): 2007, 2008 and 2009
- IEEE International Conference on Field Programmable Logic and Applications (FPL): 2008
- Southern Conference on Programmable Logic (SPL) Conference: 2008
- IEEE Field Programmable Technology (FPT): 2007, 2008
- International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA) Conference: 2006, 2007, 2008 and 2009
- International Conference on ReConFigurable Computing and FPGAs (ReConFig): 2006, 2008
- SPIE Conference: Microtechnologies for the New Millennium 2009
- IEEE Computer Society Annual Symposium on VLSI, 2009

2.2.4 Session chair at International Conferences

- The 2006 International Conference on Engineering of Reconfigurable Systems and Algorithms, ERSa 06
- IEEE 3rd Southern Conference on Programmable Logic, SPL 07
- 21th IEEE International Parallel and Distributed Processing Symposium (IPDPS'07) - Reconfigurable Architecture Workshop
- 21th IEEE International Parallel and Distributed Processing Symposium (IPDPS'07) - Reconfigurable Architecture Workshop
- IEEE International Symposium on Circuits and Systems, ISCAS 07
- 3rd International Conference on Information System Security, ICIS 07
- 22th IEEE International Parallel and Distributed Processing Symposium (IPDPS'07) - Reconfigurable Architecture Workshop

2.2.5 Revision activities

- IEEE Transactions on Very Large Scale Integration Systems
- ACM Transaction on Reconfigurable Technology and Systems
- ACM Transactions on Embedded Computing Systems
- Journal of Systems Architecture
- International Conferences:
 - IEEE International Conference on Field Programmable Logic and Applications (FPL);
 - IEEE Reconfigurable Architectures Workshop (RAW);
 - IEEE International Conference on Field-Programmable Technology (FPT);
 - ACM Great Lakes Symposium on VLSI (GLSVLSI);
 - International Symposium on System-on-Chip (ISSoC);
 - Engineering of Reconfigurable Systems and Algorithms(ERSA).

2.3 Invited talks

Dynamic Reconfigurability in Embedded System Design. Heinz Nixdorf Institute, Paderborn, Germany, January 26th 2006.

3 TEACHING ACTIVITY

3.1 Courses

Academic Year 2008 - 2009:

- Course: Projects of Ingegneria Informatica - prof. M. D. Santambrogio
Date: September 2008 - February 2009
University: Politecnico di Milano (Milano, Italy)

3.2 Teaching Assistantships

- University: Politecnico di Milano (Milano, Italy):
 - Course: High Performance and Processors and Systems - Graduate course (taught in English)
Teacher: prof. D. Sciuto
Academic Year: 07/08, 06/07
 - Course: Architettura dei Calcolatori (Computer Architecture) - Graduate Course
Teacher: prof. D. Sciuto
Academic Year: 07/08, 06/07
 - Course: Reti Logiche A - Undergraduate Course
Teacher: prof. C. Bolchini
Academic Year: 07/08, 06/07, 05/06, 04/05
 - Course: Informatica I - Undergraduate Course
Teacher: prof. C. Bolchini
Academic Year: 05/06
- University: Advanced Learning and Research Institute, master in Embedded Systems (Lugano, Switzerland):
 - Course: Design Technologies - Graduate course (taught in English)
Teacher: prof. G. De Micheli
Academic Year: 07/08, 06/07
 - Course: Validation and Verification - Graduate course (taught in English)
Teacher: prof. F. Somenzi
Academic Year: 06/07, 05/06, 04/05
- University: Università degli Studi di Milano (Crema, Italy)
 - Course: Sistemi Operativi (Operating System) - Undergraduate Course
Teacher: prof. V. Piuri
Academic Year: 07/08, 06/07, 05/06

3.3 Theses Supervision

Advisor of the following Master Theses:

- *Design Methodologies for Dynamic Reconfigurable Multi-FPGA Systems* - Student: A. Panella. University of Illinois at Chicago, May 2008;
- *Operating System Support for Core Management in a Dynamic Reconfigurable Environment* - Student: I. Beretta. University of Illinois at Chicago, May 2008;
- *Management and Analysis of Bitstreams Generators for Xilinx FPGAs* - Student: D. Candiloro. University of Illinois at Chicago, May 2008;
- *Time-driven reconfiguration-aware floorplacer* - Student: A. Montone. University of Illinois at Chicago, May 2008;
- *1D and 2D Bitstream Relocation for Partially Dynamically Reconfigurable Architecture* - Student: M. Novati. University of Illinois at Chicago, May 2008;

Co-Advisor of the following Master Theses:

From the academic year 2004 - 2005 until today, Marco D. Santambrogio has been the co-advisor of 12 students for their M.Sc. thesis works at Politecnico di Milano

Co-Advisor of the following Bachelor Theses:

From the academic year 2004 - 2005 until today, Marco D. Santambrogio has been the co-advisor of 87 students for their bachelor thesis works at Politecnico di Milano

4 AWARDS AND RESEARCH GRANTS

- **Awards:**

- **Best paper award:** 15th International Conference on Very Large Scale Integration, IFIP VLSI-SoC 2007 (*ReCPU: a Parallel and Pipelined Architecture for Regular Expression Matching* [B.28]) in
- **Dimitri N. Chorafas PhD Thesis Award** from the Chorafas Foundation (Berne, Switzerland) for the best PhD Theses in "Systems Engineering and Information Technology", May 2008. Thesis title: *Hardware/Software codesign methodologies for dynamically reconfigurable systems* ([E.1])
- December, 2008. He has been awarded a **Progetto Rocca Post-doc Fellowship Fellowship at MIT**.

5 PUBLICATIONS

5.1 International Journals

- A.1** S. Corbetta, M. Morandi, M. Novati, M. D. SANTAMBROGIO, D.Sciuto, P. Spoletini.
Internal and External Bitstream Relocation for Partial Dynamic Reconfiguration.
IEEE Transaction on Very Large Scale Integration (VLSI) Systems, *accepted - to appear*
- A.2** R. Cordone, F. Redaelli, M.A. Redaelli, M. D. SANTAMBROGIO, D.Sciuto.
Partitioning and Scheduling of Task Graphs on Partially Dynamically Reconfigurable FPGAs.
IEEE Transactions on Computer-Aided Design (TCAD) of Integrated Circuits and Systems, *accepted - to appear*

5.2 International Conferences

- B.1** F. Ferrandi, M. D. SANTAMBROGIO, D. Sciuto.
A Design Methodology for Dynamic Reconfiguration: The Caronte Architecture.
19th IEEE International Parallel and Distributed Processing Symposium (IPDPS'05) - Reconfigurable Architecture Workshop - RAW, IPDPS, vol. 04, no. 4, proc. p. 163b, April 2005
- B.2** A. Donato, F. Ferrandi, M. Redaelli, M. D. SANTAMBROGIO, D. Sciuto.
Caronte: a complete methodology to implement partially dynamically self-reconfiguring embedded systems on modern FPGA.
IEEE Symposium on Field-Programmable Custom Computing Machines - FCCM05, proc. p. 321 - 322, FCCM, April 2005
- B.3** A. Donato, F. Ferrandi, M. D. SANTAMBROGIO, D. Sciuto.
Operating system support for dynamically reconfigurable SoC architectures.
IEEE International SOC Conference - IEEE-SOCC 2005, proc. p. 235 - 238, September 2005
- B.4** G. Agosta, F. Bruschi, M. D. SANTAMBROGIO, D. Sciuto.
A Data Oriented Approach to the Design of Reconfigurable Stream Decoders.
IEEE 2005 3rd Workshop on Embedded Systems for Real-Time Multimedia - ESTIMedia 2005, proc. p. 107 - 112, September 2005
- B.5** A. Donato, F. Ferrandi, M. Redaelli, M. D. SANTAMBROGIO, D. Sciuto.
Exploiting partial dynamic reconfiguration for SoC design of complex application on FPGA platforms.
13th IFIP International Conference on Very Large Scale Integration - IFIP VLSI-SOC 2005, proc. p. 179 - 184, October 2005
Selected among the conference best papers and invited for a publication in the book: VLSI-SoC: From Systems To Silicon, Springer ([D.1])
- B.6** F. Ferrandi, M. Redaelli, M. D. SANTAMBROGIO, D. Sciuto.
Solving the Coloring Problem to Schedule on Partially Dynamically Reconfigurable Hardware.
13th IFIP International Conference on Very Large Scale Integration - IFIP VLSI-SOC 2005, proc. p. 97 - 102, October 2005
- B.7** R. Cordone, F. Ferrandi, G. Palermo, M. D. SANTAMBROGIO, D. Sciuto.
Using Speculative Computation and Parallelizing Techniques to Improve Scheduling of Control based Designs.
11th Asia and South Pacific Design Automation Conference, ASP-DAC 2006, proc. p. 898 - 904, January 2006
- B.8** F. Ferrandi, G. Ferrara, R. Palazzo, V. Rana, M. D. SANTAMBROGIO.
VHDL to FPGA automatic IPCore generation: A case study on Xilinx design flow.
20th IEEE International Parallel and Distributed Processing Symposium (IPDPS'06) - Reconfigurable Architecture Workshop - RAW, proc. p. 219, April 2006

- B.9** M. D. SANTAMBROGIO, C. Tziviskou, G. Le Moli.
MorfWeb: A New Way of Living the Web Access.
 Int'l Conference on Information and Communication Technologies and Development - ICTD 2006, May 2006
- B.10** S. Borgio, D. Bosisio, M. Monchiero, A. Tumeo, F. Ferrandi, M. D. SANTAMBROGIO, D. Sciuto.
Hardware DWT accelerator for MultiProcessor System On-Chip on FPGA.
 In Proceedings of IEEE IC-SAMOS'06 - Embedded Computer Systems: Architectures, Modeling, and Simulation, Samos, Greece, proc. p. 107 - 114, July 2006
- B.11** C. Amicucci, F. Ferrandi, M. D. SANTAMBROGIO, D. Sciuto.
SyCERS: a SystemC design exploration framework for SoC reconfigurable architecture.
 The 2006 International Conference on Engineering of Reconfigurable Systems and Algorithm, ERSA 06, proc. p. , 63 - 69, June 2006
- B.12** G. Agosta, F. Bruschi, M. D. SANTAMBROGIO, D. Sciuto.
Synthesis of Object Oriented Models on Reconfigurable Hardware.
 The 2006 International Conference on Engineering of Reconfigurable Systems and Algorithm, ERSA 06, proc. p. , 249 - 250, June 2006
- B.13** F. Ferrandi, A. Mele, V. Rana, M. D. SANTAMBROGIO, D. Sciuto.
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