Appears in the Proceedings of the 26th international conference on Parallel Architectures and Compilation Techniques (PACT), 2017

SAM: Optimizing Multithreaded Cores for Speculative Parallelism

Maleen Abeydeera* Suvinay Subramanian* Mark C. Jeffrey* Joel Emer*† Daniel Sanchez*
*Massachusetts Institute of Technology †NVIDIA
{maleen, suvinay, mcj, emer, sanchez}@csail.mit.edu

***Abstract*—This work studies the interplay between multithreaded cores and speculative parallelism (e.g., transactional memory or thread-level speculation). These techniques are often used together, yet they have been developed independently. This disconnect causes major performance pathologies: increasing the number of threads per core adds conflicts and wasted work, and puts pressure on speculative execution resources. These pathologies often squander the benefits of multithreading.**

We present speculation-aware multithreading (SAM), a simple policy that addresses these pathologies. By coordinating instruction dispatch and conflict resolution priorities, SAM focuses execution resources on work that is more likely to commit, avoiding aborts and using speculation resources more efficiently. We design SAM variants for in-order and out-of-order cores. SAM is cheap to implement and makes multithreaded cores much more beneficial on speculative parallel programs.

We evaluate SAM on systems with up to 64 SMT cores. With SAM, 8-threaded cores outperform single-threaded cores by 2.33× on average, while a speculation-oblivious policy yields a 1.85× speedup. SAM also reduces wasted work by 52%.

***Keywords*-speculative parallelism, multithreading, multicore**

I. Introduction

Hardware support for speculative parallelism is now pervasive. Several new processors already implement hardware transactional memory (HTM) [16, 35, 36, 88, 91], and many other research proposals, such as thread-level speculation (TLS) [76, 77] and deterministic multithreading [22], rely on hardware support for speculative execution of atomic regions. Likewise, commercial processors often use multithreaded cores to improve performance [73, 82]. Although speculative parallelism and multithreading are often used together—for example, three of the four commercial HTMs (Intel TSX, IBM POWER8, and BlueGene/Q) use multithreaded cores [52]—little work has explored the interplay between these techniques [27, 59]. In this paper, we show that this sacrifices significant performance, as *multithreading policies have a large effect on the performance of speculative parallelism*.

We first analyze the effect of conventional multithreading on speculative parallelism (Sec. II). Two key problems arise as the number of threads per core increases: the amount of conflicts and aborted work grows, and the time spent holding speculation resources increases, causing more stalls. Both problems have the same root cause: since the multithreading policy is oblivious to speculation, *unlikely-to-commit tasks consume scarce resources and hurt the throughput of likely-to-commit ones*. On many applications, these effects squander the benefits of multithreading, motivating the need for speculation-aware multithreading policies.

Most prior work does not consider the effect of multithreading policies on speculative parallelism. While prior work has proposed TLS and HTM systems for simultaneous multithreading (SMT) cores [3, 59] and GPUs [26, 27], they focus on the versioning and conflict detection mechanisms, not the multithreading policy. Meanwhile, prior multithreading policies for SMT cores [74, 82] and GPUs [43, 48, 68] seek to maximize pipeline and memory efficiency in non-speculative systems. But maximizing instructions per cycle is not the key concern in speculative systems—these systems should maximize the execution rate of instructions *that ultimately commit*.

Our key insight is that *tasks should be prioritized according to how speculative they are*. For TLS and other schemes that support ordered parallelism [31, 40, 76, 78, 93], where the program dictates the execution order of speculative tasks, this order directly determines how speculative each task is. For HTM and other schemes that support unordered parallelism [18, 32, 35, 51, 62], where any execution order is valid, it is less clear how speculative each task is. However, we observe that HTM conflict resolution policies often enforce an order among transactions on the fly. We can leverage this order to prioritize tasks.

We present *speculation-aware multithreading* (SAM), a simple policy that exploits this insight. SAM modifies a multithreaded processor pipeline to prioritize instructions from less-speculative tasks (Sec. III). SAM avoids pipeline interference from more- to less-speculative tasks, reducing wasted work. And since less-speculative tasks commit earlier, SAM also makes more effective use of speculation resources.

We design SAM variants for in-order and out-of-order cores. We find that SAM is much more effective than prior SMT policies that aim to maximize pipeline efficiency, like ICount [82]. We also present a simple adaptive policy that achieves SAM's low aborts when contention is high, and ICount's high pipeline efficiency when contention is low.

In summary, this paper makes the following contributions:

- An analysis that shows why conventional multithreading causes performance pathologies on speculative workloads.
- A basic SAM policy that addresses the pathologies of speculation-oblivious multithreading by always prioritizing instructions from likely-to-commit tasks at the issue stage.
- An adaptive SAM policy that further improves performance by balancing speculation efficiency and pipeline efficiency.

SAM improves the performance benefit of multithreaded cores on speculative parallel programs. We demonstrate

SAM on an architecture that supports ordered and unordered speculative parallelism (Sec. IV). On a 64-core system with 2-wide issue in-order SMT cores, with SAM, 8-threaded cores outperform single-threaded cores by 2.33× on average, while speculation-oblivious round-robin achieves a 1.85× speedup. SAM also reduces wasted work by 52%, making speculative execution more efficient. With out-of-order execution, 8-threaded cores improve performance over single-threaded cores by 1.52× with SAM vs only 1.11× with ICount, and SAM reduces wasted work by 2× (Sec. VI).

II. Background and Motivation

A. Speculative Parallelism

Prior work has investigated two main types of architectural support to exploit speculative parallelism. First, thread-level speculation (TLS) schemes seek to parallelize sequential programs [24, 28, 31, 66, 67, 76, 78, 93]. TLS schemes ship tasks from function calls or loop iterations to different cores, run them speculatively, and commit them in program order. Second, hardware transactional memory (HTM) schemes support optimistic synchronization in explicitly-parallel programs [19, 32, 35, 51, 62]. HTM guarantees that certain tasks, called transactions, execute atomically and in isolation. Unlike TLS's ordered tasks, HTM transactions are unordered.

We demonstrate the benefits of speculation-aware multithreading on Swarm [40, 41], a recent architecture for speculative parallelization. We choose Swarm as a baseline for two key reasons. First, Swarm's task-based execution model is general: it supports ordered and unordered parallelism, subsuming TLS and HTM, and allows more ordered programs to be expressed than TLS. This lets us test SAM with a broader range of speculative programs than alternative baselines. Second, Swarm's microarchitecture enables scalable speculative execution of fine-grain tasks. This lets us test SAM on large-scale systems with hundreds of threads.

Finally, prior work has also proposed software-only techniques to exploit speculative parallelism [10, 58, 65, 72, 85]. These techniques do not need hardware changes, but are limited by the overheads of version management, conflict detection, and scheduling of speculative tasks. While our evaluation focuses on hardware-accelerated techniques, SAM should be equally applicable to software-only techniques.

B. Multithreaded Cores

Multithreaded cores improve pipeline utilization by executing multiple threads concurrently. Fine-grain multithreading cores [73] can issue instructions from a single thread on each cycle, while simultaneous multithreading (SMT) cores [83] can issue instructions from multiple threads on each cycle.

Multithreading is crucial to achieve high performance with simple in-order cores, where threads suffer frequent stalls due to long-latency operations (e.g., cache misses). Simple and highly-threaded cores are the building block of throughput-optimized systems like HEP [73], Niagara [45], and GPUs [25].

Multithreading is also beneficial with out-of-order (OoO) cores, although to a smaller degree than with in-order cores, because OoO cores feature many complex techniques to tolerate long-latency operations. Unlike in-order cores, OoO cores are sensitive to the particular interleaving of instructions, and require specialized issue policies like ICount [82] to achieve high pipeline efficiency. As we will see, SAM can be combined with these policies to achieve both high speculation efficiency and high pipeline efficiency.

C. Pitfalls of Speculation-Oblivious Multithreading

We now explore the interplay between multithreaded cores and speculative tasks by analyzing the behavior of a few representative applications as the number of threads per core increases. This analysis identifies the pitfalls of speculation-oblivious multithreading and motivates the need for a speculation-aware multithreading policy.

For these experiments, we use a baseline system that extends Swarm with a state-of-the-art conflict resolution policy, Wait-n-GoTM [37]. Upon a conflict, Wait-n-GoTM adaptively decides whether to forward speculative data or to stall the requester, and orders tasks lazily. This policy reduces aborts under contention, especially for unordered benchmarks. Sec. IV describes this system in detail, but in-depth knowledge is not required to understand the following analysis.

The baseline uses 2-wide issue, in-order cores similar to those of Cavium ThunderX [30]. Cores use SMT: at each cycle, the core can issue up to two micro-ops from one or two threads. When multiple threads have issuable micro-ops, a speculation-oblivious *round-robin* policy selects among them.

Fig. 1 shows how the number of threads per core affects performance on a 64-core system (Sec. V details our methodology). Each 8-bar group reports results for a single application, using from 1 to 8 threads per core. We consider an unordered application, `vacation`, and two ordered applications, `des` and `astar`. The height of each bar is execution time relative to that of single-threaded cores (lower bars are better). Moreover, each bar shows the breakdown of how cores spend cycles:

- Cycles where micro-ops are issued by tasks that:
  - perform useful work that will be *committed*, or
  - are performing work that will later be *aborted*.
- Cycles where no micro-op is issued, because:
  - data or structural dependences among a thread's instructions result in all micro-ops being *not ready*,
  - an inter-task data-dependence *conflict* has stalled a thread's task,
  - a thread is stalled because a speculation resource is full, such as the task or commit *queue*, or
  - a thread has no instructions because it has *no task* to run.

Among these categories, multithreading is aimed at reducing *not ready* in order to increase the number of cycles where micro-ops are issued. This is beneficial when the effect is an increased rate of *committed* micro-ops. However, we will show

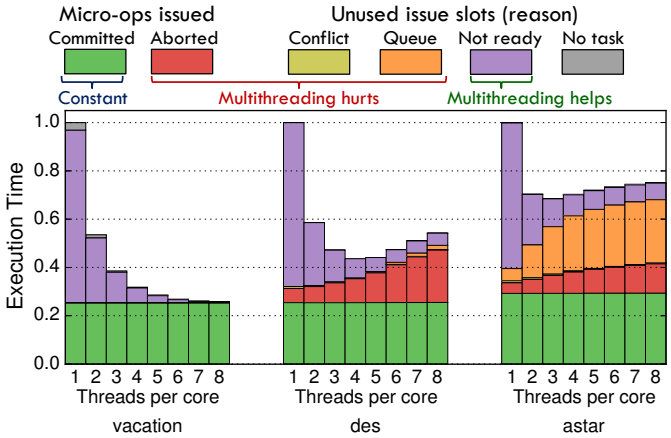


Figure 1. Execution time and cycle breakdown of three representative apps running on 64-core systems with 1 to 8 threads per core (lower is better).

that multithreading can also have the undesirable consequence of increasing cycles spent in *aborted*, *conflict*, and *queue*.

Multithreading can be highly beneficial: `vacation` in Fig. 1 shows that multithreading can dramatically increase performance. `vacation` has plentiful parallelism, but accesses main memory frequently. As a result, its time is spent either issuing instructions from tasks that later *commit*, or waiting (*not ready*) on data dependences caused by long-latency loads. With a single thread per core, not-ready stalls waste 75% of issue slots. These stalls greatly decrease with multithreading. They are still significant with four threads per core, but become negligible at eight threads per core. With eight threads per core, `vacation` is 3.9× faster than on a single thread.

This result shows that multithreading can improve performance on speculative programs: these programs often have much more parallelism than the system has cores, and multithreading is a cheap way to put that parallelism to good use. Supporting eight threads increases core area by about 30% [20] but nearly quadruples performance in `vacation`. Though more threads yield diminishing returns, we find that the most resource-efficient configuration is often highly threaded.

However, speculation introduces two deleterious pathologies that can limit the benefits of multithreading:

Pathology 1—Increased aborts: `des` in Fig. 1 shows that multithreading can increase wasted work to the point of hurting performance. Like `vacation`, `des` with a single thread per core loses many issue slots to dependences among instructions. Unlike `vacation`, `des` has limited parallelism: with a single thread per core, 7% of issue slots are wasted on tasks that are later aborted. Aborts grow with the number of threads per core: with eight threads per core, 40% of issue slots are lost to aborted work. As a result, multithreading *hurts performance* beyond four threads per core.

It is well known that, when speculative applications have limited parallelism, increasing concurrency adds aborts and may hurt performance. However, prior work has shown this effect when increasing the number of cores [92], not the number of threads per core. This implies two critical differences. First, with multithreading, wasted work hurts performance much more quickly than when increasing the number of cores, because *tasks that will abort take execution resources away from tasks that will commit, slowing them down*. Second, with multithreading, there is a simple way to affect how instructions from different tasks share core resources: the issue policy. A speculation-aware issue policy can prioritize instructions from likely-to-commit tasks, improving their performance.

Pathology 2—Inefficient use of speculation resources: `astar` in Fig. 1 shows that multithreading can degrade performance by overloading speculation resources. Like the two previous applications, single-threaded `astar` loses over half of issue slots to instruction dependences, which multithreading could address. However, `astar` is an ordered application that stresses our baseline's commit queues. Commit queues hold the speculative state of tasks that finish execution but cannot yet commit, so that the core can run another task. When these commit queues fill up, however, cores cannot run more tasks, and stall. Fig. 1 shows that these queue stalls increase with the number of threads per core, and make multithreading degrade performance beyond three threads.

In general, adding threads increases pressure on speculation resources due to two compounding effects. First, more tasks are active, demanding more speculation resources. Second, multithreading increases the latency of individual tasks, so tasks hold speculation resources for longer. This is not limited to commit queues, e.g., BlueGene/Q runs out of transaction IDs more frequently with multiple threads per core [88].

In summary, wasted work and inefficient use of speculation resources have a substantial impact on the performance of multithreading. These observations lead to speculation-aware multithreading (SAM). SAM prioritizes the execution of tasks with a higher conflict resolution priority. SAM reduces wasted work because it focuses execution resources on tasks that are more likely to commit. And SAM also reduces the time speculation resources are held, because tasks with a higher conflict resolution priority commit earlier. Though simple, SAM is highly effective at addressing these pathologies.

III. Speculation-Aware Multithreading

The speculation-aware multithreading (SAM) policy prioritizes each thread according to the conflict resolution priority of the speculative task that the thread is currently running.

We describe SAM's mechanisms for a generic conflict resolution policy (we discuss our baseline's policy in Sec. IV). A conflict resolution policy establishes an implicit or explicit priority order among speculative tasks, and resolves conflicts among tasks following this priority. For example, under most policies, lower-priority tasks cannot abort higher-priority tasks.

There is a wide variety of conflict resolution policies [11, 37, 51, 70], both in terms of the information used to prioritize tasks (age, work done so far, etc.) and the corrective actions taken upon a conflict (stalling or aborting a task, or forwarding

data). In general, two characteristics are relevant for SAM. First, a task's conflict resolution priority can change while the task runs (e.g., upon a conflict with another task). Therefore, SAM interfaces with the conflict resolution policy to receive these frequent priority updates and immediately adjust thread priorities. Second, two tasks may have the same priority (e.g., if they are unordered and have not encountered any conflicts). Therefore, SAM breaks ties among same-priority threads using a secondary policy, such as round-robin or ICount.

In the remainder of this section, we first describe SAM's implementation for in-order and out-of-order cores, then analyze why SAM effectively reduces multithreading pathologies by comparing it with several other policies.

A. SAM on In-Order Cores

Fig. 2 shows the in-order core we use and the changes needed to support SAM. Our implementation performs issue-stage prioritization. Each cycle, the issue stage selects among ready micro-ops from all threads. Priorities are absolute: ready micro-ops from a higher-priority thread are always selected over those of lower-priority threads. Ready micro-ops from same-priority threads share slots using a round-robin policy.

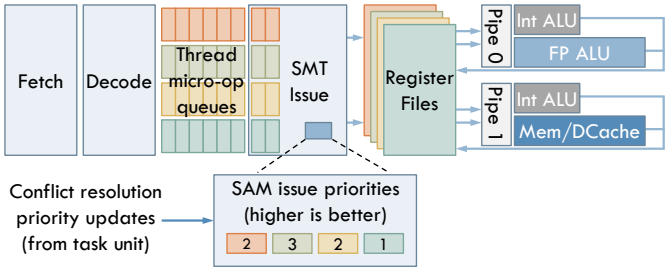


Figure 2. In-order core with SAM modifications.

This prioritized issue scheme is simple and available in commercial systems [12, 29]. The key problem that SAM addresses is how to set thread priorities to maximize the benefits of multithreaded cores on speculative systems. SAM recomputes thread priorities when a thread starts executing a new task and when the conflict resolution priority of a running task is updated.

Fairness and forward progress: SAM is unfair by design—it prioritizes one or a few threads rather than sharing resources equitably among threads. While priorities may cause long-term unfairness and even prevent forward progress in non-speculative systems [14], SAM does not suffer from these problems because conflict resolution policies always guarantee that every task can eventually become the system's highest-priority task [5, 11, 51].

B. SAM on Out-of-Order Cores

SAM's prioritized execution introduces more nuanced tradeoffs on out-of-order (OoO) cores. On in-order cores, priorities have little effect on pipeline efficiency. But priorities can affect the throughput of OoO cores, for two reasons:

- *Increased stalls:* Threads in an OoO core share limited issue buffer and reorder buffer (ROB) entries, as well as physical (renamed) registers. These resources are acquired by micro-ops before they are ready to issue. Therefore, prioritizing one thread may clog these resources with dependent micro-ops that will take a long time to become ready, causing stalls. Prior OoO SMT issue policies like ICount [82] address this pathology by prioritizing threads according to how well they use these resources. This is not a problem on in-order cores because prioritization is only done among *ready* micro-ops.
- *Increased wrong-path execution:* OoO cores can execute micro-ops far past a mispredicted branch. These wrong-path micro-ops waste execution resources. In SMT cores, if resources are shared fairly among threads, wrong-path execution becomes less frequent, because each thread has fewer micro-ops in flight (and thus does not execute as far past unresolved branches). But this reduction does not materialize if we prioritize a particular thread rather than sharing resources fairly. This is not a problem on in-order cores because a non-issuable branch prevents subsequent instructions from being issued (e.g., our in-order core resolves branches at issue, so it avoids wrong-path issues, though it does perform wrong-path fetches and decodes).

Despite these handicaps, we find that *prioritizing instructions from likely-to-commit tasks is the first-order constraint for OoO cores*. Therefore, our SAM implementation performs aggressive prioritization. In fact, SAM is more effective when backend structures (issue buffer, ROB, physical registers, and load-store queues) are dynamically shared among threads rather than statically partitioned. The reason is that shared structures let SAM prioritize threads more aggressively. Sec. VI presents experimental results to justify this selection.

SAM's desire for prioritization makes our core deviate from typical designs, which seek some amount of fairness among threads. For example, dynamically shared ROBs are relatively rare (e.g., the EV8 used a shared ROB [23], but modern Intel cores use partitioned ROBs). And our results contradict prior work by Raasch and Reinhardt [61], who find that partitioned vs shared ROBs make little difference, because they implicitly focused on fair policies.

Basic SAM policy: Fig. 3 shows our OoO core SAM implementation. Each cycle, if there are free issue buffer, ROB,

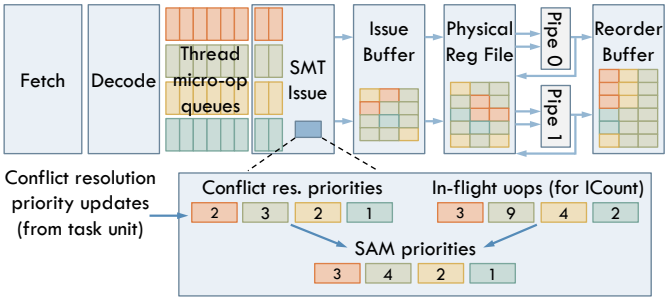


Figure 3. Out-of-order core with SAM modifications.

and renamed register entries, the issue stage injects up to two decoded micro-ops into the unified issue buffer. SAM performs prioritization at this point, always selecting micro-ops from higher-priority threads. SAM breaks ties among same-priority threads using ICount (i.e., it selects micro-ops from the thread with the fewest micro-ops in flight). This way, SAM retains ICount's pipeline efficiency when tasks are undifferentiated.

Adaptive SAM policy: Although we find that prioritizing aggressively is better *on average*, applications with rare aborts and little contention can still benefit from ICount's higher pipeline efficiency. To this end, we implement a simple policy that combines the benefits of SAM and ICount. This policy keeps running counts of cycles lost to task-level speculation (*aborted* + *conflict* + *queue*) and pipeline inefficiencies (*not ready* + *wrong path*). If cycles lost to task-level speculation dominate, the core uses SAM; if cycles lost to pipeline inefficiencies dominate, the core uses ICount. Sec. VI-C shows that this adaptive policy slightly improves on the basic SAM policy at low thread counts.

C. SAM Analysis

We now analyze why SAM effectively reduces multithreading pathologies. Fig. 4 compares SAM with several other multithreading policies. Each bar shows the breakdown of issue slots, following the same nomenclature as Sec. II-C.

These experiments use a system with 64 in-order cores with 8 threads per core (results do not qualitatively change with OoO cores). We use five representative applications that cover the full range of sensitivity to aborts, queue stalls, and conflict stalls: `vacation-high`, `des`, and `astar` from Sec. II, as well as `kmeans-high` and `intruder`.

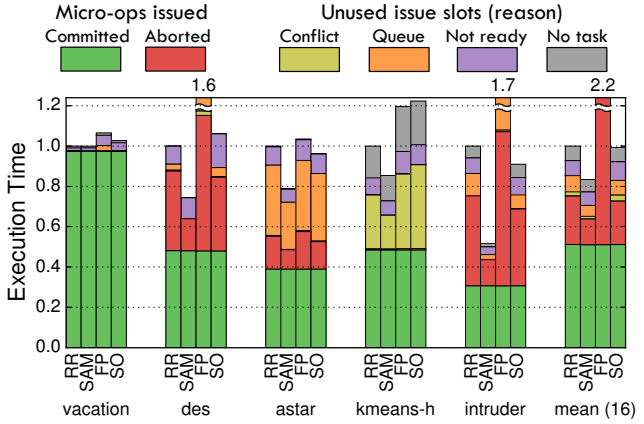


Figure 4. Execution time and cycle breakdown of different issue policies across representative applications, on a system with 64 in-order cores and 8 threads per core (lower is better).

Fig. 4 shows that SAM significantly outperforms the baseline *round-robin* policy (RR).[1] SAM reduces aborts, queue stalls, and conflicts. As we will see in Sec. VI, these benefits are consistent across all applications.

[1]We have evaluated speculation-oblivious policies beyond RR, like ICount, but they make nearly no difference on an in-order core (Sec. VI).

Two effects could explain SAM's improvement over RR. First, SAM prioritizes tasks that are more likely to commit. Second, SAM, and in fact any prioritization policy, introduces unfairness: most resources are devoted to the highest-priority task, reducing the overlap among tasks in the same core.

Distinguishing these two effects is important: any priority scheme causes unfairness, so simpler policies could perform as well as SAM. To this end, Fig. 4 also includes two simple prioritization policies: fixed-priority (FP), where each thread in the core uses a fixed priority that is preserved across tasks; and start-order (SO), which gives higher priority to older tasks.

FP performs worst, showing that prioritizing differently than the conflict resolution priority is a poor strategy: FP often gives resources to tasks that are likely to abort, wasting much more work than any other policy. At 8 threads per core, FP is 2.2× slower than RR. SO performs as well as RR on average, but shows variance across applications. We observe that SO performs better on the applications where start order is close to conflict resolution order. These experiments show that prioritizing likely-to-commit work is the dominant effect.

In summary, simpler prioritization policies perform worse than directly enforcing conflict resolution priorities. One may wonder whether a more sophisticated policy would perform better, e.g., using prediction to better estimate how likely to commit a task is. However, *if such a predictor exists, we argue that it should be used to alter the conflict resolution priority directly*.

IV. Baseline Speculative Architecture

We implement SAM on a baseline speculative architecture that builds on Swarm [40, 41], a recent architecture that performs well on both ordered and unordered programs. This lets us evaluate SAM with a broader range of programs than if we used a TLS or HTM baseline. To reduce aborts under contention and make the system more efficient on unordered benchmarks, we adopt the conflict resolution techniques from Wait-n-GoTM [37]. Although we evaluate SAM within this baseline, SAM solves a general problem and should benefit any other HTM and TLS schemes that use multithreaded cores. Further, SAM is not tied to a conflict resolution policy. We use Wait-n-GoTM because it is a state-of-the-art policy.

Sec. IV-A and Sec. IV-B present Swarm's main features (see prior work [40, 41] for details). Sec. IV-C describes the Swarm + Wait-n-GoTM conflict resolution policy. Sec. IV-D extends Swarm's conflict detection mechanisms to cheaply support multithreaded cores, in a way similar to BulkSMT [59].

A. Swarm Execution Model

Swarm programs consist of timestamped tasks. Each task may access arbitrary data, and can create child tasks with any timestamp greater than or equal to its own. Swarm guarantees that tasks appear to run in timestamp order. If multiple tasks have equal timestamp, Swarm chooses an order among them.

Swarm exposes its execution model through a simple API. Listing 1 illustrates this API by showing the Swarm implementation of `des`, a discrete event simulator for digital circuits adapted from Galois [34, 58].

```
void desTask(Timestamp ts, GateInput* input) {
  Gate* g = input->gate();
  bool toggledOutput = g.simulateToggle(input);
  if (toggledOutput)
    // Toggle all inputs connected to this gate
    for (GateInput* i : g->connectedInputs())
      swarm::enqueue(desTask, ts+delay(g,i), i);
}

void main() {
  [...]  // Set up gates and initial values
  // Enqueue events for input waveforms
  for (GateInput* i : externalInputs)
    swarm::enqueue(inputWaveformTask, 0, i);
  swarm::run();  // Start simulation
}
```

Listing 1. Swarm implementation of discrete event simulation for digital circuits.

Each task runs a function that takes a timestamp and an arbitrary number of additional arguments. Listing 1 defines one task function, `desTask`, which simulates a signal toggling at a gate input. Tasks can create child tasks by calling `swarm::enqueue` with the appropriate task function, timestamp, and arguments. In our example, if an input toggle causes the gate output to toggle, `desTask` enqueues child tasks for all the gates connected to this output. Finally, a program invokes Swarm by enqueuing some initial tasks with `swarm::enqueue` and calling `swarm::run`, which returns control when all tasks finish. For example, Listing 1 enqueues a task for each input waveform, then starts the simulation.

Swarm's execution model supports both TLS-style ordered speculation by choosing timestamps that reflect the serial order as in prior work [67], and TM-style unordered speculation by using an equal timestamp for all tasks. Moreover, Swarm's execution model generalizes TLS by *decoupling task creation and execution orders*: whereas in TLS schemes a task can only spawn speculative tasks that are immediate successors [31, 32, 67, 76, 77], a Swarm task can create child tasks with any timestamp equal or higher than its own. This allows programs to convey new work to hardware as soon as it is discovered instead of in the order it needs to run, exposing a large amount of parallelism for ordered irregular applications [40].

B. Swarm Microarchitecture

Swarm uncovers parallelism by executing tasks speculatively and out of order. To uncover enough parallelism, Swarm can speculate thousands of tasks ahead of the earliest active (unfinished) task. Swarm introduces modest changes to a tiled, cache-coherent multicore, shown in Fig. 5. Each tile has a group of multithreaded cores, each with its own private L1 cache. All cores in a tile share an L2 cache, and each tile has a slice of a fully-shared L3 cache. Every tile is augmented with a *task unit* that queues, dispatches, and commits tasks.

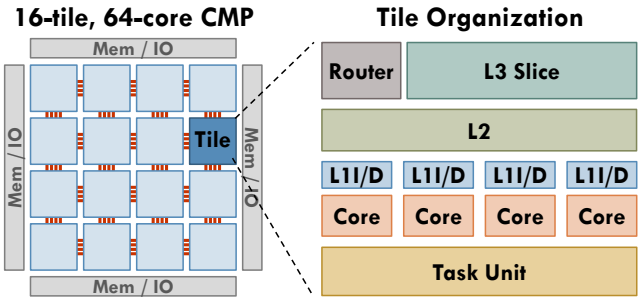


Figure 5. Swarm CMP and tile configuration.

Swarm hardware efficiently supports fine-grain tasks and a large speculation window through four main mechanisms: low-overhead hardware task management, large task queues, scalable data-dependence speculation mechanisms, and high-throughput ordered commits.

Hardware task management: Each tile's task unit queues runnable tasks and maintains the speculative state of finished tasks that cannot yet commit. Swarm executes every task speculatively, except the earliest active task. To uncover enough parallelism, task units can dispatch any available task to cores, no matter how distant in timestamp order. A task can run even if its parent is still speculative.

Each task is represented by a task descriptor that contains its function pointer, timestamp, and arguments. Threads dequeue tasks for execution in timestamp order from the local task unit. Successful dequeues initiate speculative execution at the task's function pointer and make the task's timestamp and arguments available in registers. A thread stalls if there is no task to dequeue. Tasks create child tasks and enqueue them to a tile for execution.

Large task queues: The task unit has two main structures: *(i)* a *task queue* that holds task descriptors for every task in the tile, and *(ii)* a *commit queue* that holds the speculative state of tasks that have finished execution but cannot yet commit. Together, these queues implement a task-level reorder buffer.

Task and commit queues support tens of speculative tasks per core (e.g., 128 task queue entries and 32 commit queue entries per core) to implement a large window of speculation (e.g., 8192 tasks in the 64-core CMP in Fig. 5). Nevertheless, because programs can enqueue tasks with arbitrary timestamps, task and commit queues can fill up. This requires some simple actions to ensure correct behavior. Tasks that have not been dequeued and whose parent has committed are *spilled* to memory to free task queue entries. For all other tasks, queue resource exhaustion is handled by either stalling the enqueuer or aborting higher-timestamp tasks to free space [40].

Scalable data-dependence speculation: Swarm performs eager (undo log-based) version management and eager conflict detection using Bloom filters, similar to LogTM-SE [90]. Swarm always forwards still-speculative data accessed by a later task; on a conflict, Swarm aborts only descendants and data-dependent tasks.

High-throughput ordered commits: Finally, Swarm adapts the virtual time algorithm [38] to achieve high-throughput ordered commits. Tiles periodically communicate with an arbiter (e.g., every 200 cycles) to discover the earliest unfinished task in the system. All tasks that precede this earliest unfinished task can safely commit. This scheme achieves high commit rates, up to multiple tasks per cycle on average. This allows fine-grain ordered tasks, as short as a few tens of cycles.

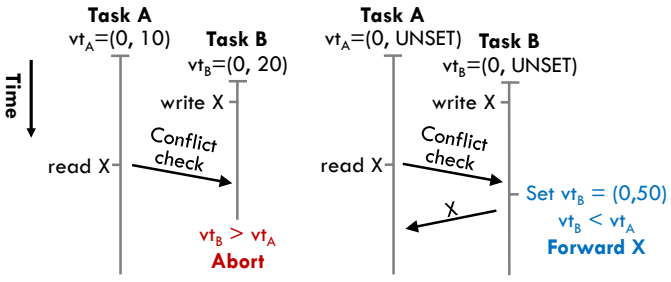
C. Conflict Resolution Policy

Our key hypothesis is that thread issue priority and conflict resolution ordering should be coordinated. Therefore, it is important that we use a conflict resolution policy that does not overly restrict task ordering. Unfortunately, Swarm as proposed in prior work overly restricts conflict resolution order among unordered tasks. Furthermore, since multithreading often increases wasted work (Sec. II), we should use a policy that minimizes aborts. Swarm also violates this principle and causes more aborts than needed by always forwarding speculative data. We solve both these problems by adapting the key techniques from Wait-n-GoTM [37].

Lazy virtual time tiebreakers: Swarm's conflict resolution policy encodes task order using *virtual time*: the concatenation of a task's programmer-assigned timestamp and a *tiebreaker*. Tiebreakers are unique and monotonically increasing, which guarantees forward progress and preserves parent-before-child order. A task's virtual time determines both its commit order and its conflict resolution order: on an access, the task aborts all conflicting higher-virtual time tasks; conversely, the task can be aborted by any lower-virtual time tasks.

The original Swarm protocol greedily assigns each task a unique tiebreaker when the task begins execution. When tasks have equal programmer-assigned timestamp, greedy tiebreaking restricts order and causes needless aborts. Fig. 6(a) shows such a needless abort: tasks A and B both have timestamp 0, and are assigned tiebreakers 10 and 20 when they start execution. Task B writes to address X first, then task A issues a read request to X. Because B is ordered after A, B must abort.

Drawing from Wait-n-GoTM [37], we instead assign tiebreakers lazily. Tasks start running without a tiebreaker, and are assigned one when they acquire a dependence with an equal-timestamp task. Fig. 6(b) shows how this works in our example: tasks A and B have no tiebreaker until task A requests X. At that point, task B, which already wrote X, acquires a tiebreaker and forwards X's data to A. Among tasks with the same timestamp, tasks without a tiebreaker are always ordered after tasks with a tiebreaker (our implementation accomplishes this by using the largest possible tiebreaker to represent UNSET). To preserve parent-before-child order, a parent acquires a tiebreaker when it creates its first equal-timestamp child. To preserve commit order, if a task finishes execution without a tiebreaker, it is assigned one. To guarantee forward progress, a task retains its tiebreaker until it commits.



(a) Needless abort caused by eager virtual time tiebreakers

(b) Lazy tiebreakers order on first conflict, avoiding abort

Figure 6. Eager virtual time tiebreakers (used in original Swarm) vs lazy tiebreakers (used here).

Wait-n-GoTM employs a more sophisticated scheme, TimeTraveler [86], which uses lower and upper bounds that are progressively restricted upon conflicts. One can construct situations where TimeTraveler would avoid aborts that a single tiebreaker cannot. However, these situations are rare (e.g., they involve three or more tasks conflicting on different addresses), and we observe the benefit would be marginal: across all applications, 81% of accesses come from tasks without tiebreakers. Therefore, we opt for this simpler scheme.

Adaptively stalling vs forwarding: Suppose an access from task A conflicts with task B (e.g., A issues a read to a line that B previously wrote). If B has higher virtual time than A, B must be aborted. However, if B has a lower virtual time than A, there are two options: the system could forward B's speculatively-written data to A, or it could stall A until B finishes executing or commits. Forwarding can improve performance, but makes A dependent on B, causing it to abort on a *cyclic* dependence, i.e., if B writes the line again.

Most systems adopt a fixed policy: LogTM [51, 90] and most early HTMs [19, 32, 63] always stall, while Swarm, DATM [64], and most other conflict-serializable HTMs [5, 59, 60] always forward. Wait-n-GoTM improves on these designs by detecting what conflicts are likely to cause cyclic dependences and stalling only on those. We adopt Wait-n-GoTM's line-based predictor and training scheme, including one predictor per tile. This predictor is checked before the tile responds to a conflicting request. If the line is predicted to cause a cyclic dependence, the tile NACKs the request, stalling requester task A, and records the dependence in staller task B's log. When B finishes, the tile ACKs task A, which resumes execution when all stalls have been cleared (multiple tasks may stall a given request). This implements the Wait-n-GoTM-*wait* variant [37].

SAM prioritization: In this system, the task's virtual time is its conflict resolution priority. Therefore, SAM prioritizes each thread using its task's virtual time. Tasks with a lower virtual time are given higher priority, and tasks with equal virtual time are given equal priority. The core recomputes thread priorities when a thread dequeues a new task and when a task's virtual time is assigned a tiebreaker.

D. Multithreaded Cores

Finally, we modify the Swarm L1 caches to support multiple threads. We strive for simplicity, since L1 accesses must be fast. Each line has a single *safe bit* per thread context. Safe bits let multiple threads share the L1 without violating conflict check rules. An L1 hit can only be served from the L1 if the thread's safe bit is set. If unset, the core issues an L2 access, which causes a conflict check. When the request finishes, the safe bit is set. If the request is a write, the line's safe bits of all other threads are cleared. When a thread dequeues a new task, if its virtual time precedes the previous task's, the thread's safe bits for all L1 lines are flash-cleared (safe bits are kept otherwise, because conflict checks performed for a given virtual time are also valid for higher ones [40]).

Safe bits are similar to BulkSMT-ORDER's access bits [59]. Unlike BulkSMT, which can detect conflicts and order tasks within the core, we defer all conflict detection to the tile for simplicity. Because tiles are small, tile-level checks are fast.

V. Experimental Methodology

Modeled systems: We use a cycle-accurate, event-driven simulator based on Pin [49, 56]. We use detailed core, cache, network, and main memory models, and simulate all speculative execution overheads (e.g., running mispeculating tasks until they abort, simulating conflict check and rollback delays and traffic, etc.). We model systems of up to 64 cores and 8 threads per core, with parameters given in Table I.

We use 2-wide issue in-order and out-of-order cores, shown in Figs. 2 and 3. Cores run the x86-64 ISA. We use the instruction decoder and functional-unit latencies of zsim's core model, which have been validated against Nehalem [69]. Our in-order core is similar to Cavium ThunderX [30], while out-of-order cores are similar to Knights Landing [75]. Cores use SMT with up to 8 threads. Threads share the front-end and execution units, but have separate micro-op queues before the issue stage. The backend has two restricted execution ports: both ports can execute integer micro-ops, but floating-point micro-ops can run in port 0 only, and memory-access micro-ops can run in port 1 only. In-order cores are scoreboarded and stall-on-use, so even a single thread can have multiple memory requests in flight. Out-of-order cores feature a 36-entry issue buffer and a 72-entry ROB, both dynamically shared.

Benchmarks: We use a diverse set of ordered and unordered benchmarks. Table II details their provenance, input sets, and 1-core run-times on an in-order core. Most benchmarks have 1-core run-times of over one billion cycles.

We use eight ordered benchmarks. Six are the graph analytics (`bfs`, `sssp`, `astar`, `msf`), simulation (`des`), and database (`silo`) applications from the original Swarm paper [40], and use the same inputs. The other two, `color` and `nocsim`, are from [39] and use the same inputs. `color` performs graph coloring using the largest-degree-first heuristic [89]. `nocsim` is a detailed NoC simulator derived from GARNET [2].

TABLE I. Configuration of the 64-core CMP.

Cores	64 cores, 16 tiles, 2 GHz, x86-64 ISA, SMT with 1–8 threads
Frontend	8B-wide ifetch; 2-level bpred with 512×10-bit BHSRs + 1024×2-bit PHT; 16-entry per-thread micro-op queues
In-order backend	2-way issue, scoreboarded, stall-on-use, functional units as in Fig. 2, 16-entry load/store buffers
OoO backend	2-way issue/rename/dispatch/commit, 36-entry issue buffer, 72-entry ROB, 16-entry load/store buffers
L1 caches	16 KB, per-core, split D/I, 8-way, 2-cycle latency
L2 caches	256 KB, per-tile, 4 banks (64 KB/bank), 8-way, hashed, inclusive, 7-cycle latency
L3 cache	16 MB, shared, static NUCA [44] (1 MB slice/tile), 4 banks/tile, 16-way, hashed, inclusive, 9-cycle bank latency
Coherence	MESI, 64 B lines, in-cache directories
NoC	4 4×4 meshes; 192-bit links, X-Y routing, 1-cycle routers, 1-cycle links
Main mem	8 controllers at chip edges, 120-cycle latency, 25.6 GB/s per controller
Queues	128 task queue entries/core (8192 total), 32 commit queue entries/core (2048 total)
Instructions	5 cycles per `enqueue/dequeue/finish_task` instruction
Conflicts	2 Kbit 8-way Bloom filters, H_3 hash functions [17] Tile checks take 5 cycles (Bloom filters) + 1 cycle per timestamp compared in the commit queue
Commits	Tiles send updates to GVT arbiter every 200 cycles
Spills	Coalescers fire when a task queue is 87% full Coalescers spill up to 15 tasks each

TABLE II. Benchmark information: source implementations, inputs, and execution time on a single in-order core, single-thread baseline system.

	Source	Input	1-core cycles
bfs	PBFS [46]	hugetric-00020 [6, 21]	2.78 Bcycles
sssp	Galois [58]	East USA roads [1]	1.95 Bcycles
astar	[40]	Germany roads [54]	1.17 Bcycles
color	[33]	com-youtube [47]	0.78 Bcycles
msf	PBBS [9]	kron_g500-logn16 [6, 21]	0.61 Bcycles
des	Galois [58]	csaArray32	1.30 Bcycles
nocsim	GARNET [2]	16x16 mesh, tornado traffic	16.32 Bcycles
silo	[81]	TPC-C, 4 whs, 32 Ktxns	2.08 Bcycles
ssca2	STAMP [50]	-s15 -i1.0 -u1.0 -l6 -p6	9.93 Bcycles
vacation-l		-n2 -q90 -u98 -r1048576 -t262144	2.56 Bcycles
vacation-h		-n4 -q60 -u90 -r1048576 -t262144	3.48 Bcycles
kmeans-l		-m40 -n40 -i rand-n16384-d24-c16	7.80 Bcycles
kmeans-h		-m15 -n15 -i rand-n16384-d24-c16	3.08 Bcycles
genome		-g4096 -s48 -n1048576	1.89 Bcycles
intruder		-a10 -l64 -s32768	1.77 Bcycles
yada		-a15 -i ttimeu100000.2	1.39 Bcycles

We use eight unordered, transactional memory benchmarks from STAMP [50]. We implement transactions with tasks of equal timestamp, so that they can commit in any order. As in prior work in transaction scheduling [4, 92], we break the original threaded code into tasks that can be scheduled asynchronously and generate children tasks as they find more work to do. The default "+" and "++" configurations are either too short in our largest system (512 threads), or too long to be simulated in reasonable time, respectively, so we use custom configurations that interpolate between the default ones.

We use all STAMP applications except `bayes` and `labyrinth`, which consist of few very long transactions that conflict frequently and all but serialize execution, making

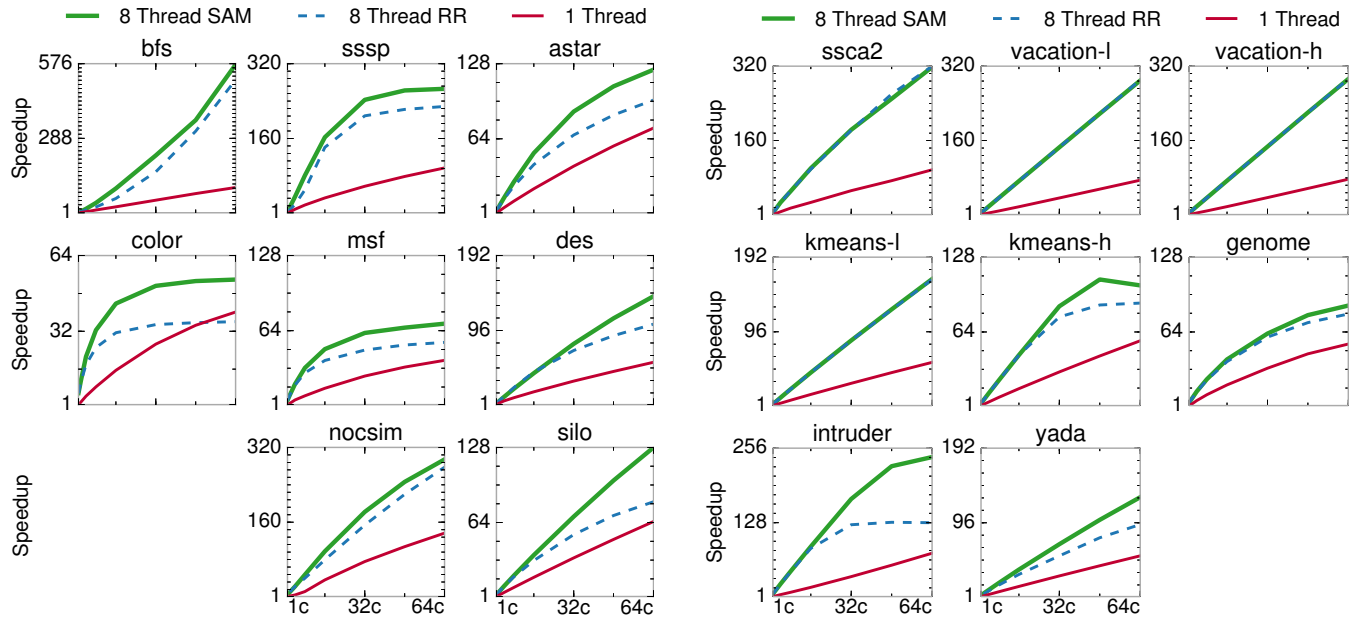


Figure 7. Performance of single-threaded cores and 8-threaded SMT cores with Round-Robin and SAM on (a) ordered and (b) unordered (STAMP) benchmarks, as the system scales from 1 to 64 cores. Speedups are relative to the 1-core single-thread system.

them unsuitable for a 512-thread system. (Extending Swarm to exploit nested speculative parallelism allows `bayes` and `labyrinth` to scale [79], but they stop being unordered applications.) We observe that `intruder` and `yada` use software task scheduling data structures that limit their scalability. We refactor both applications to use Swarm's hardware task scheduling instead, which makes them scale. We also modify `kmeans` to avoid false sharing.

Metrics: We report average performance changes using *harmonic-mean* speedups.

On issue slot breakdowns (e.g., Figs. 1 and 4), we account for each stall reason in proportion to the number of threads it prevents from issuing. For example, if an issue slot cannot be used because 3 threads have *no ready* micro-ops and the remaining 5 have *no task*, *not ready* is charged for $3/8$ of the slot, and *no task* for $5/8$. If a thread uses the slot, stalled threads are not charged.

For each benchmark, we fast-forward to the start of the parallel region (skipping initialization), and report results for the full parallel region. We perform enough runs to achieve 95% confidence intervals $\leq 1\%$.

VI. Evaluation

A. Multithreaded Scalability

Fig. 7 compares the performance and scalability of systems with 1 to 64 in-order cores, using three configurations: single-threaded cores, and 8-threaded SMT cores with the Round-Robin (RR) and SAM policies. As we scale the number of cores, we keep *per-core* L2/L3 sizes and queue capacities constant. This captures performance per unit area. Note that this causes some super-linear speedups because the larger shared L3 and hardware queues reduce memory pressure and task spills, respectively. Each line shows the speedup of a single configuration over the 1-core single-threaded system.

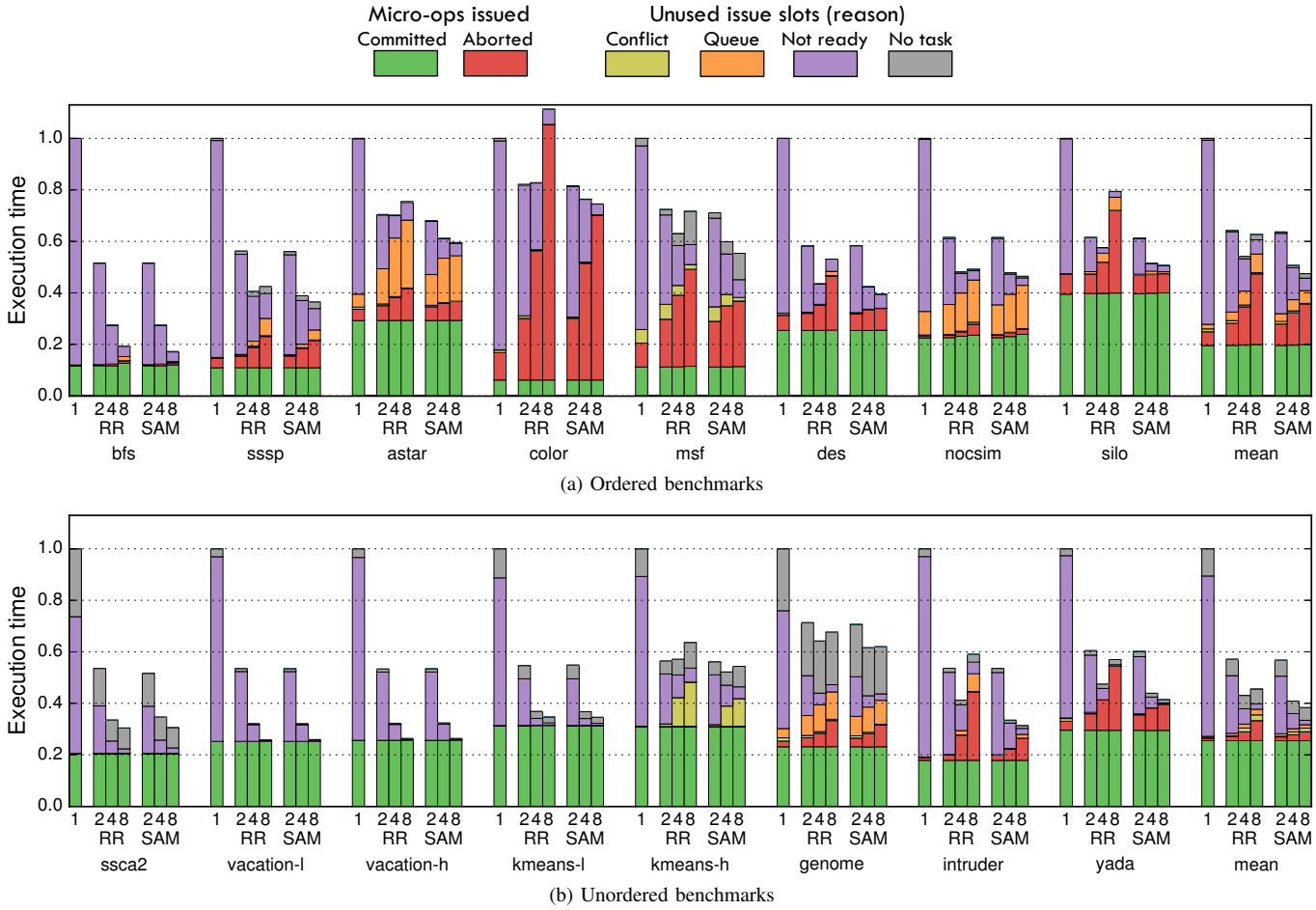
Overall, multithreading improves performance over the single-threaded configuration, by 2.33× with SAM and by 1.85× with RR on average. Over all benchmarks, SAM outperforms RR by 20% in harmonic speedup.

Four applications (`ssca2`, `vacation-l`, `vacation-h`, and `kmeans-l`) do not suffer from any multithreading pathology: they have negligible aborts and conflicts, and do not overload commit queues. Thus, they are insensitive to the issue policy—RR and SAM perform identically.

For all other applications, SAM consistently outperforms RR. SAM's benefits usually increase with the number of cores, as application parallelism becomes more scarce, and pathologies more frequent. SAM eliminates or ameliorates these pathologies. On these applications, SAM outperforms RR by 28% on average, and by up to 88% (`intruder`).

B. Analysis of SAM on In-Order Cores

To gain more insights into the differences between SAM and RR, Fig. 8 reports the execution time and issue slot breakdown at 64 cores. Similar to Fig. 1, it shows how increasing the number of threads per core affects execution time. Each seven-bar group reports results for one application, using single-threaded cores as well as 2-, 4-, and 8-threaded cores with both RR and SAM. Results are normalized to those of single-threaded cores (lower bars are better).



(a) Ordered benchmarks

(b) Unordered benchmarks

Figure 8. Execution times and breakdown of issue slots at 64 cores (in-order) for (a) ordered and (b) unordered (STAMP) benchmarks, under a single-threaded configuration, and 2-, 4-, and 8-threaded configurations with Round-Robin and SAM (lower is better).

Overall, increasing the number of threads per core has three dominant effects: *(i)* not-ready stalls decrease, *(ii)* conflict stalls and issue slots lost to aborted tasks increase, and *(iii)* queue stalls increase. By prioritizing the execution of tasks that are more likely to commit, SAM mitigates the latter two factors and improves on RR. We analyze how these factors affect applications with different contention characteristics and speculation requirements.

SAM has little effect when the pipeline is lightly loaded: Fig. 8 shows that SAM's benefits over RR increase with larger thread counts: SAM's overall benefit is negligible at 2 threads/core, 6% at 4 threads/core, and 20% at 8 threads/core. This happens because SAM, and in fact any issue prioritization policy, has little effect when the number of threads is insufficient to cover stalls (e.g., due to cache misses). In this situation, not-ready stalls are common, and threads rarely compete for issue slots in the same cycle. Fig. 8 shows that this is common with few threads per core, where not-ready stalls are significant.

Nonetheless, multithreaded systems generally include enough threads to hide stalls and saturate the pipeline in most applications, and SAM is highly effective in this regime. Note that the number of threads needed to saturate the pipeline is implementation-dependent. Systems with simple in-order cores need a large number of threads to cover stalls. For example, Niagara [45] uses 8 threads/core. However, systems with more complex cores that use aggressive (and expensive) intra-thread stall-hiding mechanisms, such as out-of-order execution, need fewer threads. Indeed, on out-of-order cores SAM delivers significant gains with fewer threads per core (Sec. VI-C).

RR and SAM perform equally well on applications without pathologies: Ordered `bfs` and unordered `ssca2`, `vacation-l`, `vacation-h`, and `kmeans-l` have plentiful parallelism but are memory-bound. With little contention, most time is spent issuing instructions from tasks that commit, or stalled on long-latency loads. RR and SAM perform equally well by reducing not-ready stalls. However, even eight threads per core cannot hide all memory latency in `bfs` and `ssca2`, and some stalls remain. At eight threads per core, these applications complete 2.9× (`kmeans-l`) to 5.2× (`bfs`) faster than with single-threaded cores.

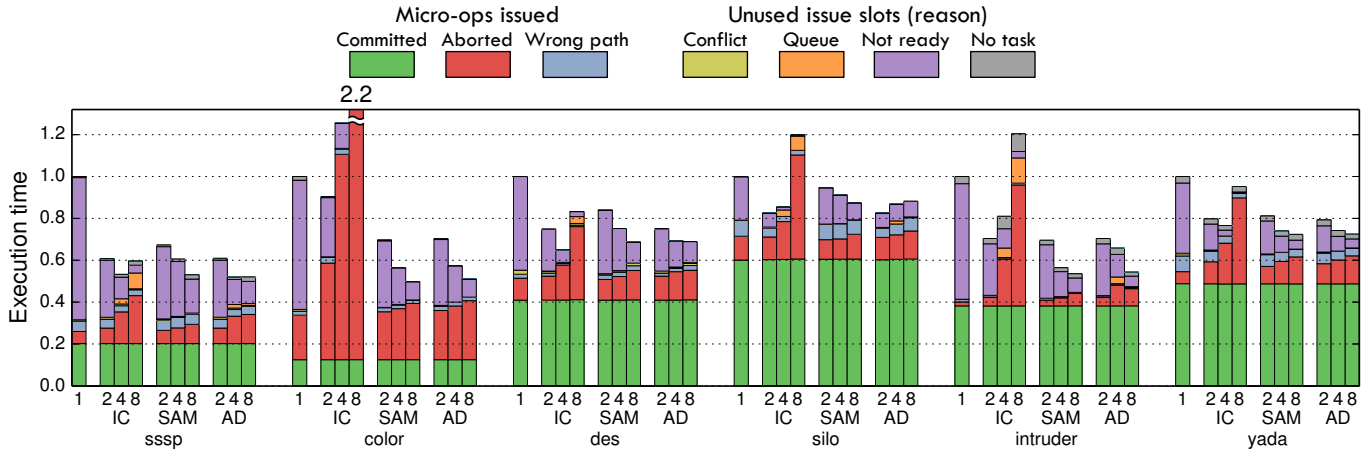


Figure 9. Execution times and breakdown of issue slots with 64 *out-of-order* cores for selected benchmarks, under a single-threaded configuration, and 2-, 4-, and 8-threaded configurations with ICount, SAM, and ADaptive policies.

SAM reduces wasted work and conflicts under contention: `color` has occasional data dependences among tasks, so adding threads increases aborts. With RR, aborts grow to the point of overwhelming the benefit of reduced stalls. However, since SAM prioritizes issues from tasks that are more likely to commit, it tempers the performance loss caused by aborted work. At eight threads per core, SAM is 49% faster than RR on `color`, and 34% faster than with single-threaded cores. `msf`, `des`, and `silo` exhibit similar behavior.

The STAMP benchmarks `genome`, `intruder`, and `yada` also benefit from SAM. Though these applications are unordered, transactions inherit an order from the dynamic manifestation of dependences. Prioritization based on this order reduces wasted work by as much as 3.1× (`intruder`).

On `kmeans-high`, conflict stalls, caused when the Wait-n-GoTM protocol detects a likely cyclic dependence, negate the reduction in not-ready stalls. SAM reduces the chance of such dependences by reducing the overlap of transactions.

SAM reduces queue stalls on applications that need a large speculation window: To find independent work, ordered applications may speculate so far ahead that they fill their commit and task queues, causing queue stalls. Queue stalls are significant in many ordered benchmarks and `astar` exemplifies this phenomenon. As we saw in Sec. II, in `astar`, increasing threads per core with RR causes queue stalls to grow to the point of negating the benefits of reduced not-ready stalls. SAM reduces queue stalls by focusing execution resources on tasks with a lower virtual time, which must commit earlier. At eight threads per core, SAM is 27% faster than RR on `astar`, and 68% faster than the single-threaded configuration. `sssp` and `silo` exhibit similar effects; SAM improves their performance by reducing both queue stalls and aborted issue slots. `nocsim`'s queue stalls are significant, but do not grow beyond two threads per core; SAM helps `nocsim` by reducing aborted work, not queue stalls.

C. Analysis of SAM on Out-of-Order Cores

Compared to in-order cores, out-of-order cores are able to cover more stalls, so the performance benefits of multithreading are lower. However, a comparatively larger fraction of issue slots are wasted to aborts, hence the need for SAM is higher. On average, 8-threaded cores outperform single-threaded cores by 1.52× with SAM vs only 1.11× with ICount (IC). Moreover, at 8 threads, SAM reduces wasted work by 2× over IC. [2]

To understand these differences, Fig. 9 reports the execution time and issue slot breakdown for six representative applications. `color`, `silo`, and `intruder` show that *aborts and conflict/queue stalls are the first-order concern in OoO cores*. With IC, cycles lost to these pathologies make these applications *slower* on 8-threaded cores than on single-threaded cores. By contrast, SAM keeps cycles lost to aborts and conflict/queue stalls nearly flat, outperforming IC by up to 4.4× (`color`). This happens even though IC reduces not-ready stalls and wrong-path execution more than SAM.

`sssp` shows how the adaptive policy can be beneficial. With 2 and 4 threads per core, IC's better pipeline utilization makes IC outperform SAM. With SAM, a single thread grabs most ROB entries, starving lower-priority threads. The adaptive policy detects this situation (*aborts* < *wrong path* + *not ready stalls*) and opts for the higher pipeline efficiency of IC. `des` and `silo` show similar behavior.

Finally, `intruder` shows a case where the adaptive policy is suboptimal. With 4 threads per core, SAM has more not-ready stalls than IC but it more than makes up for it by reducing aborts. Therefore, the basic SAM policy is 43% faster than IC. However, the adaptive SAM policy, which by design tries to equalize aborts and stalls, attains a middle ground, where it is only 23% better than IC. Though they occur, these anomalies are very rare, and adaptive SAM nearly always matches the best of SAM and IC.

[2]We have also evaluated using RR instead of IC in OoO cores, but, like prior work, we find that IC is consistently better.

Sensitivity to resource sharing policies: As discussed in Sec. III, we dynamically share backend OoO structures among threads. Fig. 10 shows why this is a good idea by comparing the performance of statically-partitioned and dynamically-shared ROBs under IC and SAM. With more threads, IC suffers more aborts and queue and conflict stalls. These hurt performance with more threads, despite IC's higher pipeline utilization (fewer cycles lost to wrong-path or not-ready micro-ops). Partitioned and shared ROBs show the same trend.

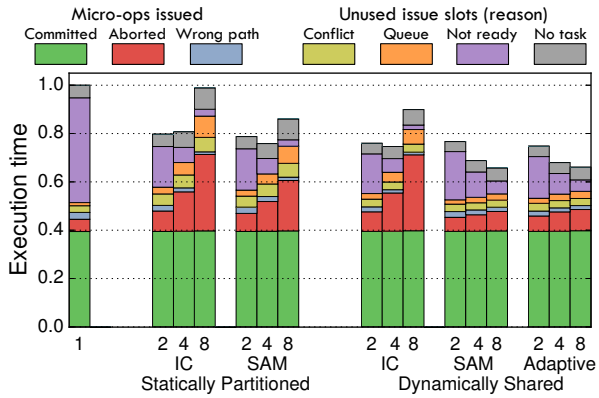


Figure 10. Performance of ICount, basic SAM, and adaptive SAM with statically-partitioned vs dynamically-shared ROBs.

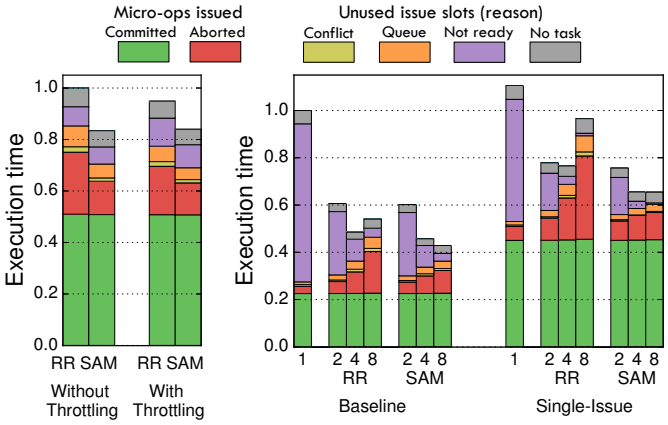
SAM ameliorates these pathologies, but the type of ROB impacts its effectiveness. With partitioned ROBs, as threads grow SAM still suffers from increased aborts and queue/conflict stalls, although at a lower rate than ICount. This happens because the highest-priority thread fills its ROB partition and lets micro-ops from other, more speculative threads be issued.

With a shared ROB, however, SAM can fill the issue buffer with micro-ops from a single thread. As a result, SAM keeps cycles lost to aborts and queue/conflict stalls nearly flat. This comes at the price of higher wrong-path micro-ops and not-ready stalls. But these inefficiencies are secondary, and SAM is thus most effective when it can prioritize most aggressively.

D. Case Study: Throttling

Throttling, i.e., limiting the number of tasks executed in parallel, is a general strategy to reduce aborts in speculative systems. Prior work has designed transactional memory schedulers that limit the number of concurrent transactions [4, 7, 8, 92], reacting to contention to reduce aborts. Throttling can improve performance when tasks that ultimately abort slow down committed tasks, as is the case with multithreaded cores. However, we show that SAM is significantly more effective than throttling: adaptively limiting the number of active threads provides no benefit over SAM, and while throttling slightly improves RR, a large gap remains between RR and SAM.

We implement a simple throttler that builds on two insights. First, in all our applications, we observe there is a single thread count that performs best, and there are no other local maxima. Therefore, we use simple hill climbing to find the best number



(a) Effect of throttling (b) Effect of issue width

Figure 11. Average execution time and issue slot breakdown for in-order 64-core (a) 8-threaded systems with RR and SAM, with and without throttling; and (b) systems with dual-issue (baseline) and single-issue cores.

of threads per core. Second, many applications are either stable or change slowly over time. Therefore, we perform hill climbing as the application runs, incurring minimal cost.

Our throttler operates by periodically exploring nearby thread counts, and settles on the count that performs best. Since our applications are speculative, we use committed instructions per cycle as the performance metric (i.e., we do not consider executed instructions from tasks that later abort).

First, the throttler randomly chooses to either increase or decrease the number of active threads on every core in the system. If performance improves at the new thread count, the throttler continues changing the number of threads per core in the same direction, until it either reaches the minimum/maximum number of threads or performance degrades. If performance degrades, the throttler goes back to the previous thread count. This way, the throttler settles on the best-performing thread count among the explored ones. Each measurement interval is M cycles long, and the throttler stays at the new thread count for S cycles. We tune M (50K−500K cycles) and S (250K−2.5M cycles) on a per-application basis to provide maximum benefit for each application.

RR with throttling yields marginal improvements, and a large gap with SAM remains: As shown in Fig. 11(a), throttling improves RR marginally, by 5.4% on average at 8 threads per core. However, this is not sufficient to close the gap with SAM. Moreover, throttling does not improve SAM's performance. Throttling with RR only helps reduce aborts incurred at higher thread counts. In contrast, SAM reduces aborted instructions and queue stalls by prioritizing instructions from tasks that are likely to commit. Further, performance with throttling is sensitive to the throttler's interval lengths—no single length performs best across all applications. Such careful parameter tuning makes throttling harder to apply than SAM.

In summary, throttling is inferior to SAM, as applying it to RR fails to capture most of SAM's improvements.

E. Sensitivity to Issue Width

Finally, Fig. 11(b) compares the behavior of a single-issue in-order core to the baseline 2-wide issue core. With one thread per core, the single-issue core performs 11% worse than the baseline. RR's performance degrades more rapidly beyond four threads, and 8-threaded RR cores are worse than 2-threaded cores. This happens because fewer threads are needed to avoid most stalls in the narrower pipeline. By contrast, SAM's performance does not degrade with thread count, although its benefits with increasing thread counts are reduced. Overall, this result shows that SAM avoids pathologies even when execution resources are more heavily contended.

VII. Additional Related Work

A. Multithreading in Speculative Parallelism

IMT [57] is perhaps the closest proposal to SAM. For a multithreaded single-core TLS system, IMT prioritizes the sole non-speculative thread when inter-thread dependences are frequent. In contrast, SAM derives core-local priorities for all cores and threads in the system. While IMT is sensible in a 1-core system, on the 512-thread system we evaluate, IMT would have negligible impact by prioritizing the one thread (system-wide) that runs the single non-speculative task.

Other work has supported speculative parallelization on SMT cores, first in the context of TLS [3, 55, 87], and more recently on HTM [59]. These proposals focus on tailoring the versioning and conflict detection mechanisms to SMT cores. However, these systems use conventional multithreading policies, such as round-robin or ICount [82]. By contrast, SAM shows that coordinating issue and conflict resolution priorities makes speculation much more efficient.

Recent work has implemented HTM for GPUs [26, 27], which have heavily multithreaded cores. Like the above designs, this work focuses on tailoring speculative mechanisms to the characteristics of GPUs, to cope with their large numbers of threads and exploit their data-parallel nature. These techniques also use conventional multithreading policies.

B. Prioritization in Non-Speculative Systems

Prior work has proposed SMT prioritization policies for parallel programs. Tullsen et al. [84] propose fine-grain synchronization techniques to accelerate lock-based programs. Cai et al. [15] and Boneti et al. [12, 13] use SMT priorities to address work imbalance in barrier-based programs. Beyond SMT, ACS [80] and BIS [42] accelerate critical sections and other bottlenecks in multithreaded programs by scheduling them in fast cores on a heterogeneous system. These prioritization techniques are useful to accelerate non-speculative synchronization constructs, but not speculative parallelism, where all synchronization among tasks is implicit.

Prior work has also proposed many GPU thread (i.e., warp) prioritization schemes [43, 48, 53, 68, 71]. These schemes mainly seek to improve locality by limiting the number of threads that are interleaved at fine granularity. Locality is the overriding concern in GPUs because they are heavily threaded and have very little on-chip storage per thread. However, issue policies have a minor effect on locality for the number of threads per core we consider.

Finally, some SMT systems expose issue priorities to software [12, 29]. While our SAM implementation controls priorities in hardware, software TM or TLS systems could use this support to implement SAM.

VIII. Conclusion

We have shown that conventional multithreading policies cause significant pathologies on speculative parallel programs: increased aborts and added pressure on speculation resources. We have presented speculation-aware multithreading (SAM), a simple policy that addresses these pathologies. SAM prioritizes threads by their conflict resolution priority. By focusing execution resources on likely-to-commit tasks, SAM reduces aborts and conflicts; and since these tasks commit earlier, SAM also makes more effective use of speculation resources. As a result, SAM improves the performance benefit of multithreaded cores on speculative programs. On a 64-core system with 2-wide issue in-order SMT cores, 8-threaded cores outperform single-threaded ones by 2.33× on average with SAM, vs. by 1.85× with round-robin. SAM also reduces wasted work by 52%. With out-of-order execution, 8-threaded cores outperform single-threaded cores by 1.52× with SAM vs only 1.11× with ICount, and SAM reduces wasted work by 2×.

Acknowledgments

We sincerely thank Nathan Beckmann, Victor A. Ying, Hyun Ryong Lee, Nosayba El-Sayed, Harshad Kasture, Po-An Tsai, Guowei Zhang, Anurag Mukkara, Yee Ling Gan, our shepherd Lawrence Rauchwerger, and the anonymous reviewers for their helpful feedback.

This work was supported in part by C-FAR, one of six SRC STARnet centers by MARCO and DARPA, and by NSF grants CAREER-1452994 and CCF-1318384. Mark C. Jeffrey was partially supported by an NSERC postgraduate scholarship.

REFERENCES

[1] "9th DIMACS Implementation Challenge: Shortest Paths," 2006.

[2] N. Agarwal, T. Krishna, L.-S. Peh, and N. K. Jha, "GARNET: A detailed on-chip network model inside a full-system simulator," in *ISPASS*, 2009.

[3] H. Akkary and M. A. Driscoll, "A dynamic multithreading processor," in *MICRO-31*, 1998.

[4] M. Ansari, M. Luján, C. Kotselidis, K. Jarvis, C. Kirkham, and I. Watson, "Steal-on-abort: Improving transactional memory performance through dynamic transaction reordering," in *HiPEAC*, 2009.

[5] U. Aydonat and T. S. Abdelrahman, "Hardware support for relaxed concurrency control in transactional memory," in *MICRO-43*, 2010.

[6] D. Bader, H. Meyerhenke, P. Sanders, and D. Wagner, Eds., *10th DIMACS Implementation Challenge Workshop*, 2012.

[7] G. Blake, R. G. Dreslinski, and T. Mudge, "Proactive transaction scheduling for contention management," in *MICRO-42*, 2009.

[8] G. Blake, R. G. Dreslinski, and T. Mudge, "Bloom filter guided transaction scheduling," in *MICRO-44*, 2011.

[9] G. Blelloch, J. Fineman, P. Gibbons, and J. Shun, "Internally deterministic parallel algorithms can be fast," in *PPoPP*, 2012.

[10] W. Blume, R. Doallo, R. Eigenmann, J. Grout, J. Hoeflinger, and T. Lawrence, "Parallel programming with Polaris," *Computer*, vol. 29, no. 12, 1996.

[11] J. Bobba, K. E. Moore, H. Volos, L. Yen, M. D. Hill, M. M. Swift, and D. A. Wood, "Performance pathologies in hardware transactional memory," in *ISCA-34*, 2007.

[12] C. Boneti, F. J. Cazorla, R. Gioiosa, A. Buyuktosunoglu, C.-Y. Cher, and M. Valero, "Software-controlled priority characterization of POWER5 processor," in *ISCA-35*, 2008.

[13] C. Boneti, R. Gioiosa, F. J. Cazorla, and M. Valero, "A dynamic scheduler for balancing HPC applications," in *SC08*, 2008.

[14] S. Boyd-Wickizer, M. F. Kaashoek, R. Morris, and N. Zeldovich, "Non-scalable locks are dangerous," in *Linux Symposium*, 2012.

[15] Q. Cai, J. González, R. Rakvic, G. Magklis, P. Chaparro, and A. González, "Meeting points: using thread criticality to adapt multicore hardware to parallel regions," in *PACT-17*, 2008.

[16] H. W. Cain, M. M. Michael, B. Frey, C. May, D. Williams, and H. Le, "Robust architectural support for transactional memory in the Power architecture," in *ISCA-40*, 2013.

[17] J. Carter and M. Wegman, "Universal classes of hash functions (extended abstract)," in *STOC-9*, 1977.

[18] L. Ceze, J. Tuck, P. Montesinos, and J. Torrellas, "BulkSC: bulk enforcement of sequential consistency," in *ISCA-34*, 2007.

[19] L. Ceze, J. Tuck, J. Torrellas, and C. Cascaval, "Bulk disambiguation of speculative threads in multiprocessors," in *ISCA-33*, 2006.

[20] J. D. Davis, J. Laudon, and K. Olukotun, "Maximizing CMP throughput with mediocre cores," in *PACT-14*, 2005.

[21] T. Davis and Y. Hu, "The University of Florida sparse matrix collection," *ACM TOMS*, vol. 38, no. 1, 2011.

[22] J. Devietti, B. Lucia, L. Ceze, and M. Oskin, "DMP: deterministic shared memory multiprocessing," in *ASPLOS-XIV*, 2009.

[23] J. Emer, "EV8: the post-ultimate alpha," *Keynote at PACT*, 2001.

[24] A. Estebanez, D. R. Llanos, and A. Gonzalez-Escribano, "A survey on thread-level speculation techniques," *ACM CSUR*, vol. 49, no. 2, 2016.

[25] K. Fatahalian and M. Houston, "GPUs a closer look," in *ACM SIGGRAPH 2008 classes*, 2008.

[26] W. W. Fung and T. M. Aamodt, "Energy efficient GPU transactional memory via space-time optimizations," in *MICRO-46*, 2013.

[27] W. W. Fung, I. Singh, A. Brownsword, and T. M. Aamodt, "Hardware transactional memory for GPU architectures," in *MICRO-44*, 2011.

[28] M. J. Garzarán, M. Prvulovic, J. M. Llabería, V. Viñals, L. Rauchwerger, and J. Torrellas, "Tradeoffs in buffering speculative memory state for thread-level speculation in multiprocessors," in *HPCA-9*, 2003.

[29] R. Golla and P. Jordan, "T4: A highly threaded server-on-a-chip with native support for heterogeneous computing," in *HotChips-23*, 2011.

[30] L. Gwennap, "ThunderX rattles server market," *Microprocessor Report*, vol. 29, no. 6, 2014.

[31] L. Hammond, M. Willey, and K. Olukotun, "Data speculation support for a chip multiprocessor," in *ASPLOS-VIII*, 1998.

[32] L. Hammond, V. Wong, M. Chen, B. D. Carlstrom, J. D. Davis, B. Hertzberg, M. K. Prabhu, H. Wijaya, C. Kozyrakis, and K. Olukotun, "Transactional memory coherence and consistency," in *ISCA-31*, 2004.

[33] W. Hasenplaugh, T. Kaler, T. B. Schardl, and C. E. Leiserson, "Ordering heuristics for parallel graph coloring," in *SPAA*, 2014.

[34] M. A. Hassaan, M. Burtscher, and K. Pingali, "Ordered vs. unordered: a comparison of parallelism and work-efficiency in irregular algorithms," in *PPoPP*, 2011.

[35] M. Herlihy and J. E. B. Moss, "Transactional memory: Architectural support for lock-free data structures," in *ISCA-20*, 1993.

[36] C. Jacobi, T. Slegel, and D. Greiner, "Transactional memory architecture and implementation for IBM System Z," in *MICRO-45*, 2012.

[37] S. A. R. Jafri, G. Voskuilen, and T. Vijaykumar, "Wait-n-GoTM: improving HTM performance by serializing cyclic dependencies," in *ASPLOS-XVIII*, 2013.

[38] D. Jefferson, "Virtual time," *ACM TOPLAS*, vol. 7, no. 3, 1985.

[39] M. C. Jeffrey, S. Subramanian, M. Abeydeera, J. Emer, and D. Sanchez, "Data-centric execution of speculative parallel programs," in *MICRO-49*, 2016.

[40] M. C. Jeffrey, S. Subramanian, C. Yan, J. Emer, and D. Sanchez, "A scalable architecture for ordered parallelism," in *MICRO-48*, 2015.

[41] M. C. Jeffrey, S. Subramanian, C. Yan, J. Emer, and D. Sanchez, "Unlocking ordered parallelism with the Swarm architecture," *IEEE Micro*, vol. 36, no. 3, May 2016.

[42] J. A. Joao, M. A. Suleman, O. Mutlu, and Y. N. Patt, "Bottleneck identification and scheduling in multithreaded applications," in *ASPLOS-XVII*, 2012.

[43] A. Jog, O. Kayiran, N. Chidambaram Nachiappan, A. K. Mishra, M. T. Kandemir, O. Mutlu, R. Iyer, and C. R. Das, "OWL: Cooperative thread array aware scheduling techniques for improving GPGPU performance," in *ASPLOS-XVIII*, 2013.

[44] C. Kim, D. Burger, and S. Keckler, "An adaptive, non-uniform cache structure for wire-delay dominated on-chip caches," in *ASPLOS-X*, 2002.

[45] P. Kongetira, K. Aingaran, and K. Olukotun, "Niagara: A 32-way multithreaded SPARC processor," *IEEE Micro*, vol. 25, no. 2, 2005.

[46] C. Leiserson and T. Schardl, "A work-efficient parallel breadth-first search algorithm," in *SPAA*, 2010.

[47] J. Leskovec and A. Krevl, "SNAP Datasets: Stanford large network dataset collection," http://snap.stanford.edu/data, 2014.

[48] D. Li, M. Rhu, D. R. Johnson, M. O'Connor, M. Erez, D. Burger, D. S. Fussell, and S. W. Redder, "Priority-based cache allocation in throughput processors," in *HPCA-21*, 2015.

[49] C. Luk, R. Cohn, R. Muth, H. Patil, A. Klauser, G. Lowney, S. Wallace, V. J. Reddi, and K. Hazelwood, "Pin: Building customized program analysis tools with dynamic instrumentation," in *PLDI*, 2005.

[50] C. C. Minh, J. Chung, C. Kozyrakis, and K. Olukotun, "STAMP: Stanford Transactional Applications for Multi-Processing," in *IISWC*, 2008.

[51] K. Moore, J. Bobba, M. Moravan, M. Hill, and D. Wood, "LogTM: Log-based transactional memory," in *HPCA-12*, 2006.

[52] T. Nakaike, R. Odaira, M. Gaudet, M. M. Michael, and H. Tomari, "Quantitative comparison of hardware transactional memory for Blue Gene/Q, zEnterprise EC12, Intel Core, and POWER8," in *ISCA-42*, 2015.

[53] V. Narasiman, M. Shebanow, C. J. Lee, R. Miftakhutdinov, O. Mutlu, and Y. N. Patt, "Improving GPU performance via large warps and two-level warp scheduling," in *MICRO-44*, 2011.

[54] OpenStreetMap, "http://www.openstreetmap.org."

[55] V. Packirisamy, Y. Luo, W.-L. Hung, A. Zhai, P.-C. Yew, and T.-F. Ngai, "Efficiency of thread-level speculation in SMT and CMP architectures-performance, power and thermal perspective," in *ICCD*, 2008.

[56] H. Pan, K. Asanović, R. Cohn, and C.-K. Luk, "Controlling program execution through binary instrumentation," *SIGARCH Comput. Archit. News*, vol. 33, no. 5, Dec 2005.

[57] I. Park, B. Falsafi, and T. N. Vijaykumar, "Implicitly-multithreaded processors," in *ISCA-30*, 2003.

[58] K. Pingali, D. Nguyen, M. Kulkarni, M. Burtscher, M. A. Hassaan, R. Kaleem, T.-H. Lee, A. Lenharth, R. Manevich, M. Méndez-Lojo, D. Prountzos, and X. Sui, "The tao of parallelism in algorithms," in *PLDI*, 2011.

[59] X. Qian, B. Sahelices, and J. Torrellas, "BulkSMT: Designing SMT processors for atomic-block execution," in *HPCA-18*, 2012.

[60] X. Qian, B. Sahelices, and J. Torrellas, "OmniOrder: Directory-based conflict serialization of transactions," in *ISCA-41*, 2014.

[61] S. E. Raasch and S. K. Reinhardt, "The impact of resource partitioning on SMT processors," in *PACT-12*, 2003.

[62] R. Rajwar and J. R. Goodman, "Transactional lock-free execution of lock-based programs," in *ASPLOS-X*, 2002.

[63] R. Rajwar, M. Herlihy, and K. Lai, "Virtualizing transactional memory," in *ISCA-32*, 2005.

[64] H. E. Ramadan, C. J. Rossbach, and E. Witchel, "Dependence-aware transactional memory for increased concurrency," in *MICRO-41*, 2008.

[65] L. Rauchwerger and D. A. Padua, "The LRPD test: Speculative run-time parallelization of loops with privatization and reduction parallelization," *IEEE Trans. Parallel Distrib. Syst.*, vol. 10, no. 2, 1999.

[66] J. Renau, K. Strauss, L. Ceze, W. Liu, S. Sarangi, J. Tuck, and J. Torrellas, "Thread-level speculation on a CMP can be energy efficient," in *ICS'05*, 2005.

[67] J. Renau, J. Tuck, W. Liu, L. Ceze, K. Strauss, and J. Torrellas, "Tasking with out-of-order spawn in TLS chip multiprocessors: microarchitecture and compilation," in *ICS'05*, 2005.

[68] T. G. Rogers, M. O'Connor, and T. M. Aamodt, "Cache-conscious wavefront scheduling," in *MICRO-45*, 2012.

[69] D. Sanchez and C. Kozyrakis, "ZSim: Fast and accurate microarchitectural simulation of thousand-core systems," in *ISCA-40*, 2013.

[70] W. N. Scherer III and M. L. Scott, "Advanced contention management for dynamic software transactional memory," in *PODC*, 2005.

[71] A. Sethia, D. A. Jamshidi, and S. Mahlke, "Mascar: Speeding up GPU warps by reducing memory pitstops," in *HPCA-21*, 2015.

[72] N. Shavit and D. Touitou, "Software transactional memory," in *PODC*, 1995.

[73] B. Smith, "The architecture of HEP," in *On Parallel MIMD computation: HEP supercomputer and its applications*, 1985.

[74] A. Snavely and D. M. Tullsen, "Symbiotic jobscheduling for a simultaneous multithreading processor," in *ASPLOS-IX*, 2000.

[75] A. Sodani, R. Gramunt, J. Corbal, H.-S. Kim, K. Vinod, S. Chinthamani, S. Hutsell, R. Agarwal, and Y.-C. Liu, "Knights Landing: Second-generation Intel Xeon Phi product," *IEEE Micro*, vol. 36, no. 2, 2016.

[76] G. Sohi, S. Breach, and T. Vijaykumar, "Multiscalar processors," in *ISCA-22*, 1995.

[77] J. G. Steffan, C. Colohan, A. Zhai, and T. Mowry, "A scalable approach to thread-level speculation," in *ISCA-27*, 2000.

[78] J. G. Steffan and T. Mowry, "The potential for using thread-level data speculation to facilitate automatic parallelization," in *HPCA-4*, 1998.

[79] S. Subramanian, M. C. Jeffrey, M. Abeydeera, H. R. Lee, V. A. Ying, J. Emer, and D. Sanchez, "Fractal: An execution model for fine-grain nested speculative parallelism," in *ISCA-44*, 2017.

[80] M. A. Suleman, O. Mutlu, M. K. Qureshi, and Y. N. Patt, "Accelerating critical section execution with asymmetric multi-core architectures," in *ASPLOS-XIV*, 2009.

[81] S. Tu, W. Zheng, E. Kohler, B. Liskov, and S. Madden, "Speedy transactions in multicore in-memory databases," in *SOSP-24*, 2013.

[82] D. M. Tullsen, S. J. Eggers, J. S. Emer, H. M. Levy, J. L. Lo, and R. L. Stamm, "Exploiting choice: Instruction fetch and issue on an implementable simultaneous multithreading processor," in *ISCA-23*, 1996.

[83] D. M. Tullsen, S. J. Eggers, and H. M. Levy, "Simultaneous multithreading: Maximizing on-chip parallelism," in *ISCA-22*, 1995.

[84] D. M. Tullsen, J. L. Lo, S. J. Eggers, and H. M. Levy, "Supporting fine-grained synchronization on a simultaneous multithreading processor," in *HPCA-5*, 1999.

[85] N. Vachharajani, R. Rangan, E. Raman, M. J. Bridges, G. Ottoni, and D. I. August, "Speculative decoupled software pipelining," in *PACT-16*, 2007.

[86] G. Voskuilen, F. Ahmad, and T. Vijaykumar, "TimeTraveler: Exploiting acyclic races for optimizing memory race recording," in *ISCA-37*, 2010.

[87] S. Wallace, B. Calder, and D. M. Tullsen, "Threaded multiple path execution," in *ISCA-25*, 1998.

[88] A. Wang, M. Gaudet, P. Wu, J. N. Amaral, M. Ohmacht, C. Barton, R. Silvera, and M. Michael, "Evaluation of Blue Gene/Q hardware support for transactional memories," in *PACT-21*, 2012.

[89] D. J. Welsh and M. B. Powell, "An upper bound for the chromatic number of a graph and its application to timetabling problems," *The Computer Journal*, vol. 10, no. 1, 1967.

[90] L. Yen, J. Bobba, M. Marty, K. Moore, H. Volos, M. Hill, M. Swift, and D. Wood, "LogTM-SE: Decoupling hardware transactional memory from caches," in *HPCA-13*, 2007.

[91] R. M. Yoo, C. J. Hughes, K. Lai, and R. Rajwar, "Performance evaluation of Intel transactional synchronization extensions for high-performance computing," in *SC13*, 2013.

[92] R. M. Yoo and H.-H. S. Lee, "Adaptive transaction scheduling for transactional memory systems," in *SPAA*, 2008.

[93] Y. Zhang, L. Rauchwerger, and J. Torrellas, "Hardware for speculative run-time parallelization in distributed shared-memory multiprocessors," in *HPCA-4*, 1998.