The Design of a Low Power Carbon Nanotube Chemical Sensor System

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ABSTRACT

This paper presents a hybrid CNT/CMOS chemical sensor system that comprises of a carbon nanotube sensor array and a CMOS interface chip. The full system, including the sensor, consumes $32\mu W$ at $1.83kS/s$ readout rate, accomplished through an extensive use of CAD tools and a model-based architecture optimization. A redundant use of CNT sensors in the frontend increases the reliability of the system.

Categories and Subject Descriptors

B.7.0 Hardware [**Integrated Circuits**]: General

General Terms

Design

Keywords

Sensor System, Carbon Nanotube, Low Power

1. INTRODUCTION

Autonomous microsensor systems receive much attention from both industry and government for the potential in detecting the hazardous environment. The emergence of nanotechnology has also accelerated such research efforts by proposing new reliable sensing materials [1].

To reflect this trend, a number of sensor-integrated CMOS platforms have been introduced, and demonstrated a stable and accurate operation [2, 3]. The power consumption of these systems exceeds several milliwatts, primarily due to the use of a micro-hotplate which heats up the sensors to achieve high sensitivity, and also due to the use of OPAMPs to accommodate a large dynamic range.

This paper extends upon the state-of-the-art by presenting an ultra-low power chemical sensor system consuming 32 μW using carbon nanotubes (CNTs) as the chemical sensing medium [4]. The prototype system comprises of two chips, a CMOS interface chip and a CNT sensor chip, integrated on a printed circuit board.

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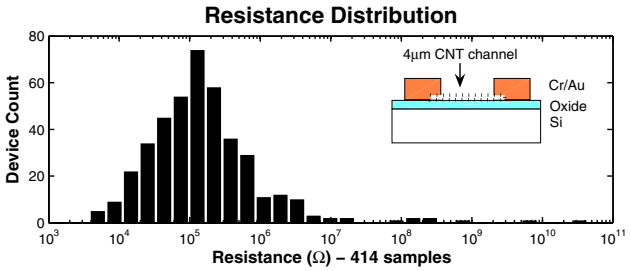


Figure 1: Measured data on the distribution of CNT resistance from 414 devices. inset: CNT-FET sensor diagram.

This paper begins with a description of the CNT sensor characteristics and testing procedures. Next, the interface architecture and design optimization are explained. Then, the design methodology and performance of the CMOS chip are discussed. Finally, the complete system results and test setup are presented.

2. CNT SENSOR CHARACTERIZATION

2.1 Device Fabrication

In this study, the resistance change of CNT FETs is monitored as the sensors are exposed to NO_2, a toxic gas released in industrial processes and automotive emissions. An array of CNT sensors is used to sense the chemical to increase the stability of the system in the presence of CNT sensor process variation.

CNTs can be highly sensitive even at room temperature unlike other sensing technologies. This feature renders a micro-hotplate unnecessary, making CNTs particularly attractive for low-power applications. Additionally, CNTs have nanometer range diameters which facilitate miniaturization. Since all atoms in a CNT are exposed on its surface, high selectivity to specific chemical agents can be achieved through coating. However, current fabrication methods generally yield CNTs with large resistance variations. Furthermore, CNT sensors exhibit fast response but slow recovery time to gases. While active heat or UV treatment can accelerate the long recovery time, such schemes are not amenable to low power operation and thus hasn't been implemented in this work.

In this work, an array of 24 single-walled CNT FETs is fabricated on a p-type silicon wafer with a thin layer of thermal oxide on top. The layout for a 4-inch Cr mask was designed in *CleWin*. This mask defines alignment marks and large metal pads used for probing devices. After photo-lithographically patterning the wafers, a layer of Ti/Pt was deposited. *DesignCad LT* was used to create all patterns for subsequent electron-beam lithography steps. After

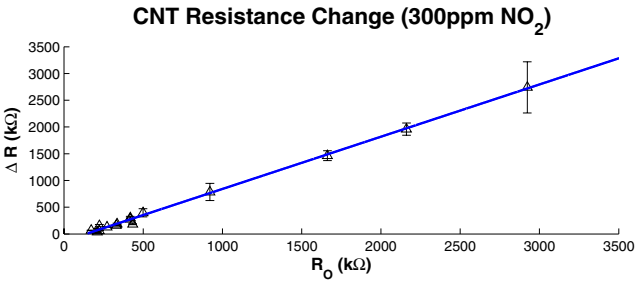


Figure 2: Experimental data on the linear dependence on ΔR-R_0. Multiple sensing measurements were taken from a single die using the setup in Section 2.2.

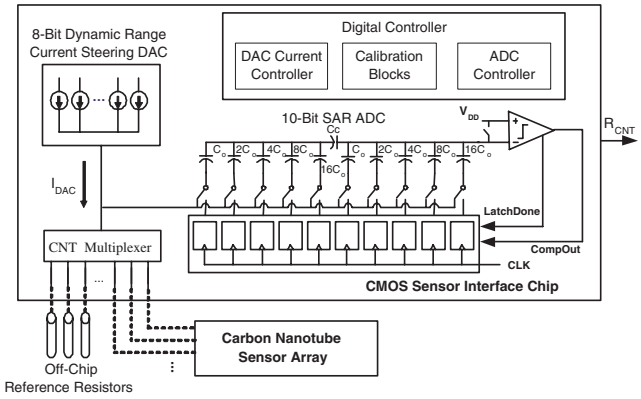


Figure 3: Proposed interface architecture.

patterning and depositing islands of Fe/Mo-based catalyst, CNTs are grown via chemical vapor deposition (CVD), using a CH_4 gas source at 900^{o}C [5]. Finally, a second metal layer (Cr/Au) is deposited to achieve good electrical contact to the nanotubes.

2.2 Sensor Characteristics and Test Procedures

All DC measurements were obtained using a semiconductor parameter analyzer (*HP 4156A*). Figure 1 shows the CNT FET structure (4 μm channel, Cr/Au contacts) and the distribution of resistance, exhibiting a spread across 6 orders of magnitude. This distribution results from one of the most critical and challenging aspects of CNT fabrication: the number of CNTs between the electrodes of each device can vary and can be either metallic or semiconducting, where semi-conducting CNT FETs have a diameter-dependent band gap. To interface to the CNT sensor array, the front-end circuit accomodate a wide resistance range, effectively defined as 10 $k\Omega$ - 9 $M\Omega$. In addition, the CNT resistance should be measured with a precision near 2% to detect NO_2 in the sub-ppm range, which results in a 16-bit dynamic range (R_{LSB}=182 Ω).

A gas-flow control system was constructed to serve as a test vehicle for characterizing the CNT sensors before integrating with the CMOS chip. This setup allowed independent sensor studies to be conducted, and most of the gas control setup was re-used during system testing presented in this section. Each mass flow controller (MFC) has an independent control knob, and a total of three MFCs were used: two for the carrier gas (Ar) and one for the sensing gas (NO_2). The concentration of NO_2 is modulated by adjusting the flow rates of each gas. The maximum flow rate for the two MFCs for Ar differ by an order of magnitude to produce a broader range of gas concentrations. In addition, a pre-diluted mix of 1000 ppm NO_2 in Ar was used to achieve ppm-range concentrations. Due to practical limits of maximum flow rate and MFC control resolution, the effective concentration range was 600 ppb - 1000 ppm. A varying mixture of NO_2 and Ar eventually flows into the sealed gas chamber, out through an outlet, and is dispersed in the chemical fume hood. The T-shaped gas chamber was made out of PVC due to its chemical resiliency.

After measuring the DC properties of each CNT device, selected dies were packaged and wire-bonded on a 68-pin chip carrier. The packaged chip is inserted through one end of the gas chamber, and the chamber is sealed during experiments. The chip is electrically connected to a custom-made variable-gain transimpedance amplifier, which can measure up to 8 devices simultaneously. All signals are set and acquired by a data acquisition unit from National Instruments (USB-6008), which is then recorded on a computer via *LabView*. To measure resistances over a wide range, the gain of the transimpedance amplifier was designed to be manually adjustable. The *LabView* interface also provides features to re-calibrate the transimpedance amplifiers and record the gain settings.

The CMOS interface, presented in subsequent sections, essentially automates the above control circuitry and procedures in a single chip. While the large dynamic range of CNT resistance poses circuit challenges, using an array of sensors as opposed to single devices can effectively increase the reliability of gas detection and identification. Figure 2 shows the linear relation between the resistance change and the initial baseline resistance of several measured devices. Multiple sensing measurements were taken from a single die. The initial baseline conductance was measured in the presence of Ar before introducing NO_2. The final conductance value was taken as the saturated value after introducing NO_2. As-grown array allows systematic studies of the resistive properties of CNT FETs over a wide range, and highlights the need for variation-tolerant circuit interfaces.

3. CARBON NANOTUBE SENSOR INTERFACE CHIP

The CMOS interface design is constrained primarily by two competing interests: low power consumption and a large dynamic range. In order to reduce power, an OPAMP-less interface architecture is exploited in this work. The architecture should also be amenable to power-scaling as the resistance readout rate is reduced. To meet these goals, the proposed work allocates the dynamic range requirement into two analog blocks of lower dynamic range. To interface the array of sensors, the interface chip should have at least 24 sensor channels.

3.1 Proposed Architecture

The basic idea of the proposed architecture is to source predetermined current to the CNT sensors, and read the voltage developed across the sensors. This architecture is attractive because the interface can change the resistance measurement resolution by changing the input current ($R_{resolution} = \frac{V_{LSB}}{I_{INPUT}}$), and can easily be time-multiplexed to access multiple sensor channels. Note from the equation the inherent trade-off between the power consumption (i.e. input current) and the resolution.

Figure 3 shows the architecture proposed in this work, comprised of an ADC, a variable current source and a digital controller. Note that if the dynamic range of the ADC is N bits, and if the dynamic range of the current source is M bits, the dynamic range of the proposed architecture is N+M bits. For this chip, two extra bits are

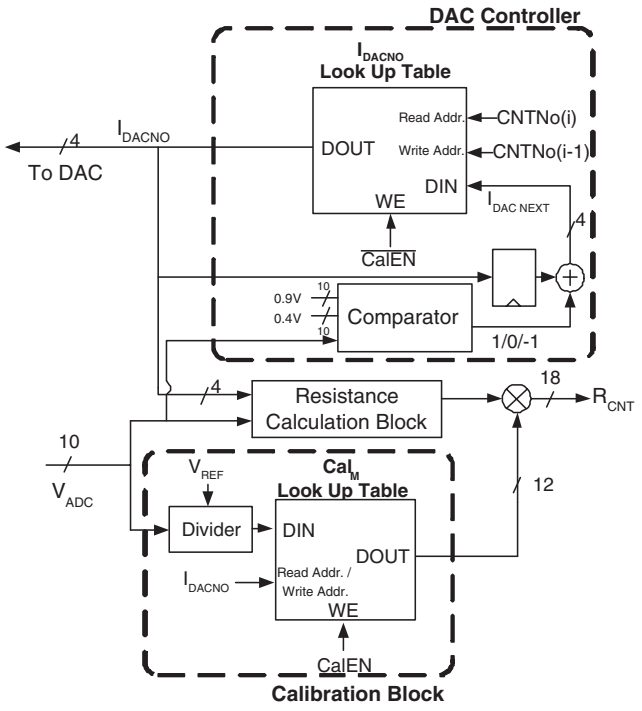


Figure 4: The critical dataflow in the digital controller.

added to the required 16-bit dynamic range to enable a digital DAC calibration, as explained in Section 3.3.

A successive approximation register (SAR) ADC is chosen for this work because the only components that draw static current are the preamplifiers in the comparator. The preamplifiers are gated when the ADC is turned off to further save power. Also, a sub-DAC configuration is used for the capacitor DAC in order to save die area [6].

The variable current source (to vary the I_{INPUT}) is implemented using a current steering DAC. The current source can thus be controlled with digital words rather than an analog voltage. A thermometer - code configuration of a current steering DAC is used to better match the DAC cells in the presence of process variations.

The digital controller block serves three purposes: calibrating the non-linearity of the DAC, adaptively controlling the DAC current as the resistance changes, and controlling the ADC operation. The designed chip interfaces 24 CNT sensors, which are sequentially time-multiplexed through a 32:1 CNT multiplexer. Extra ports are used for off-chip reference resistors used during the DAC calibration (Section 3.3.)

3.2 DAC Control Schemes

The DAC control for the proposed architecture is an underconstrained problem in that several combinations of current and voltage can result in the same resistance value. Observing that the proposed architecture can increase the measurement resolution by increasing the input current, the digital controller (Figure 4) drives the DAC current to be the maximum while keeping enough headroom for the DAC current sources. The control scheme is further simplified by allowing only binary-weighted current from the DAC. In other words, the DAC output current can be one of nine levels (100 nA, 200 nA, ... , 25.6 μA). The input current is denoted with 4-bit I_{DACNO}, which takes on the values 0 - 8 as current increases. Constraining the current levels to only binary multiples of minimum current allows the chip to compute the resistance with a simple register shift operations.

The resistance of each CNT sensor will change as chemical is introduced; the current controller automatically adjusts the DAC output current for the next measurement based on the present resistance measurement (Figure 4.) If the voltage from the i^{th} sensor is greater than 0.9V or less than 0.4V, the comparator outputs -1 and 1, respectively. The output of the comparator is added to the I_{DACNO} to update the look-up table for that particular (i^{th}) CNT's next measurement.

3.3 DAC Current Calibration

In order to measure the exact resistance, the proposed architecture relies heavily on the ideal characteristics of the DAC and ADC. However, process variations can deteriorate the linearity of the current-steering DAC. This can result in a nonlinear resistance conversion characteristic. The DAC linearity problem is exacerbated since the DAC cells will be biased in the subthreshold regime. To reduce the linearity error, the proposed design measures the current with known off-chip reference resistors, and stores the ratio of the desired current to the measured current in a look-up table. This ratio is then multiplied by the resistance computed through shift register operations to obtain the calibrated resistance. The overhead (in terms of power, die area, and calibration time) of measuring the current is not significant since there are only nine current levels.

4. DESIGN METHODOLOGIES

4.1 Energy Optimization with MATLAB

Energy optimization is performed on the proposed architecture. As a first optimization step, the supply voltages in both analog and digital domains are scaled to 1.2V and 0.5V, respectively. The second optimization step studies different ways of allocating 18-bit dynamic range requirement to two analog blocks to minimize the energy consumption. Energy per resistance conversion can be represented as

$$E_{OP} = P_{ADC} \times T_{ADC} + P_{DAC} \times T_{DAC} + E_{DIGITAL} \quad (1)$$

where E_{OP} is the energy consumed per resistance read-out operation, P_{ADC} and P_{DAC} are the power consumed by ADC and DAC respectively, and T_{ADC} and T_{DAC} are the on-period of ADC and DAC, respectively. The objective of the proposed optimization is to minimize E_{OP} as N varies, where N is the number of bits allocated to the ADC. This optimization was carried out in *MATLAB* by modeling each terms in Equation 1.

In the case of the SAR ADC, T_{ADC} can simply be modeled as $N \times T_{CLK}$, the amount of time needed for one voltage conversion operation. Modeling T_{DAC} is not as straightforward because it is in general a function of N and parasitic capacitances at the ADC input node. When the ADC is N bit, the signal present at the ADC input node should also have at least N-bit precision. Thus,

$$T_{DAC} \geq R_{INPUT} \times C_{INPUT} \times \ln(2^N) \quad (2)$$

where R_{INPUT} and C_{INPUT} are the effective resistance and capacitance looking into the ADC input node from the current steering DAC. R_{INPUT} is roughly the CNT resistance, while C_{INPUT} can be approximated by the sum of capacitances from the capacitor DAC in the ADC and the parasitic capacitance at the input signal node. The parasitic capacitance (C_{par}) at the input signal node is swept between $1 - 5pF$ based on a simple model of the testing setup. P_{ADC} is extrapolated from the Figure-of-Merit (FOM) of typical low speed ADCs. Assuming 20kS/s operation with an FOM of 250fJ/conversion step, $P_{ADC} = 5 \times 10^{-9} \times 2^{N+1}$.

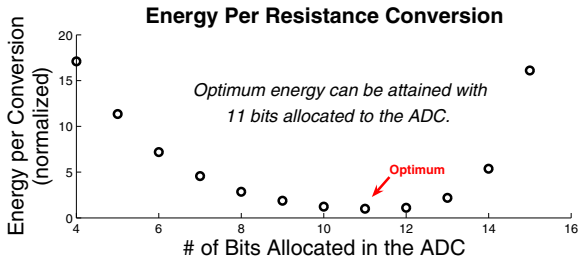


Figure 5: Energy consumed per resistance conversion as the ADC resolution changes.

To model the DAC power, I_{LSB} should be determined. The I_{LSB} is determined by the largest resistance to measure and the required voltage headroom for the DAC (in this implementation, 0.3V headroom is guaranteed.) To measure 9MΩ with 0.9V voltage swing available at the ADC input node, 100nA is chosen as the minimum current. Consequently, $P_{DAC} = 100nA \times 2^{(18-N)} \times 1.2V$.

The energy consumption of the system is plotted as a function of N in Figure 5; the energy per conversion achieves a narrow optimum around N = 11. However, designing a single-ended 11-bit ADC is not a trivial task, and the penalty paid by using a 10-bit ADC instead is only 17%. Thus, a 10-bit ADC is used in this work.

4.2 Circuit Simulation and Implementation

The design flow of the chip is shown in Figure 6. The chip can be divided up into the analog and the digital parts. The analog component design, including the ADC and the DAC, was carried out primarily in the *Cadence* environment. *Cadence Spectre* simulation tool was used for the functionality verification, and *Cadence Virtuoso* was used for layout. Analog signal interconnects are carefully laid out as to minimize the coupling with the digital circuit.

The digital component design exploited CAD tools extensively. The digital blocks, including the ADC controller, were designed using *Verilog*, and the functionality of the design was verified with *Synopsys VCS Verilog Simulator*. Once the functionality of the digital blocks have been verified, *Synopsys Design Compiler* was used to synthesize the circuit using $0.18\mu m$ standard cell library.

As mentioned in Section 4.1, the digital blocks operate at 0.5V. Therefore, *Cadence SignalStorm* was used to re-characterize the standard cells at 0.5V prior to synthesizing the chip. During synthesis with *Synopsys Design Compiler*, extensive clock-gating was implemented to reduce the power consumption. Once the transistor-level description of the chip was generated, *Nanosim* was used to verify the functionality of the digital components. After functional verification, *Synopsys Astro* was used for place-and-route. *Synopsys Primetime* was then used to verify timing in the post-layout netlist, accounting for process variations.

Finally, the digital components and the analog blocks were connected in *Synopsys Astro*. First, the analog blocks laid-out in *Cadence Virtuoso* were imported *Synopsys Astro*, and was placed. Then guard-rings were placed around sensitive analog blocks to decouple between the analog and digital components. The analog and digital components were routed through the place-and-route function in *Synopsys Astro* using Scheme scripts. The operation of the system is verified with *Synopsys Nanosim* at a lower accuracy setting, with extracted capitances from the layout.

4.3 Chip Testing Strategy and Setup

A register scan-chain is used to read the resistor values from the chip and to read / modify important control registers. For example,

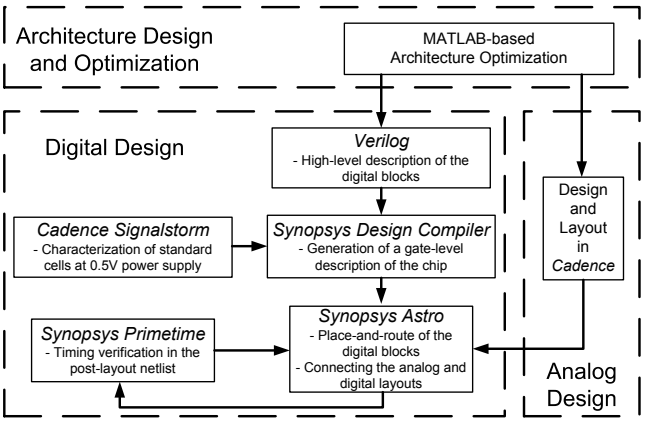


Figure 6: The design flow of the chip.

the scan-chain can be used to read / modify calibration words computed during the DAC calibration phase, and it can also be used to read / modify the I_{DACNO} look up table (LUT.) The ability to control these registers is useful in debugging.

The chip has an on-chip configuration register that can specify the testing mode of the system. The chip has three testing modes: the DAC testing mode, the ADC testing mode and the system testing mode. During the DAC testing mode, the I_{DACNO} look-up table can be controlled with an external signal. Since the chip will not operate the DAC at a high frequency, it's not necessary to modify the entries in the LUT at a high frequency. During the ADC testing mode, a sinusoid of 14-bit signal resolution is applied to the chip - digitized with the ADC. The digital blocks, excluding the ADC control, can be turned on/off so that the performance of the ADC can be characterized in the presence/absence of the digital circuit noise. During the system testing mode, the system operates in a normal fashion, but the registers on chip can be freely controlled with external signals. The system testing mode facilitates the full characterization of the chip.

An arbitrary waveform generator, a *Keithley* sourcemeter, a *Tektronix* 500MHz real-time scope, a *Tektronix* logic analyzer and pattern generator were used in chip testing. The test vectors were generated from the verilog simulation scripts, and were post-processed with *Perl* to meet the format of the pattern generator.

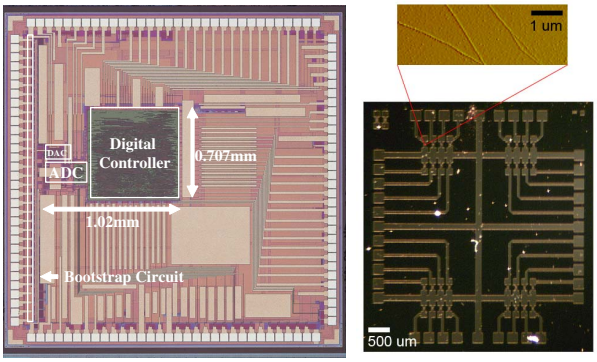
5. PERFORMANCE RESULTS

5.1 Chip Testing Result

The CMOS interface chip was fabricated in a 0.18 μm CMOS process (Figure 7(a)) to verify the concepts introduced in this paper. T_{DAC} of 512 μs was sufficient to provide 10-bit signal resolution at the input of ADC, and was kept at 512 μs throughout the chip testing. The performance, as well as the statistics of this chip, is summarized in Table 1.

Chip Specifications	
Process Technology	180 nm
Active Area	$\sim$ 1.02 mm $\times$ 0.707 mm
Number of Pins	128 Pins
Supply Voltage	0.5 V (Digital) 1.2V (Analog)

Table 1: Statistics of the chip



(a) (b)

Figure 7: The die photo of (a) the CMOS interface circuit. (b) the CNT chemical sensor chip.

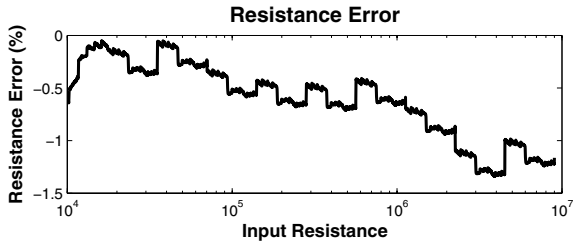


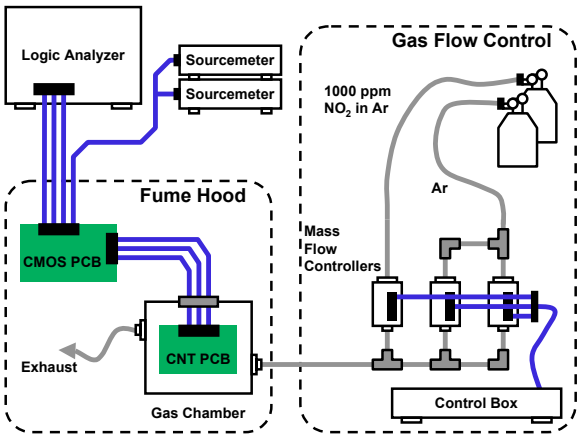
Figure 8: Measurement error across the entire dynamic range is less than 1.34%.

Using the DAC calibration scheme, the DAC current error up to 8% is calibrated down to less than 1.2% for every DAC word. The residual current error is suspected to be due to the mismatch among the reference resistors. The resistance measurement error is less than 1.34% across the whole dynamic range (Figure 8.) Primary sources of error are the residual DAC nonlinearity and the ADC nonlinearity. The INL and DNL of the designed ADC is +1.34LSB/-1.2LSB and +0.46LSB/-0.22LSB, respectively. The power dissipation of the designed interface scales linearly as the sampling rate reduces. The worst case power consumption occurs when resistors all lie close to $10K\Omega$ (i.e. the DAC is fully on for all CNT's), in which case 32 μW is consumed at 1.83 kS/s sampling rate.

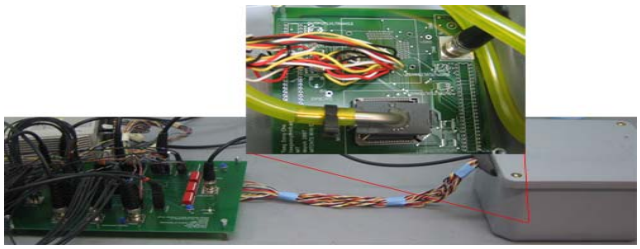
The performance of published chemical sensor interfaces is compared in Table 2. The μ-hotplate power is excluded, if applicable. Notice that the specification of the published interfaces varies greatly, thus a fair comparison of these interfaces remains as a difficult task. Nevertheless, Table 2 shows that the power consumption of the proposed work compares favorably with the state-of-the-art sensor interfaces.

5.2 System Demonstration

CNT chemical sensors (Figure 7(b)) and the interface chip is integrated on a printed circuit board, and the functionality of the full system is tested by exposing the CNT sensors to 50 ppm, 150 ppm and 300 ppm of NO_2 in Ar. The gas was introduced to the CNT sensors that sit in a gas chamber, and the measurement taken by the fabricated chip is acquired by a logic analyzer. Figure 9(a) shows a diagram of the equipment setup. Section 2.2 describes details of the sensing experiments, and the identical MFCs and gas flow controller is used here for system testing. The sensing circuitry



(a)



(b)

Figure 9: (a)This is a block diagram showing the entire equipment setup for the system demonstration. Details of the gas flow control setup is described in Section 2.2. The two test chips are both placed in the chemical fume hood, and the signals are acquired by the logic analyzer. (b) A photo of the testing setup.

and *LabView* interface is replaced by the CMOS interface chip and logic analyzer. To accommodate the printed circuit board, a larger square-shaped gas chamber replaces the T-shaped chamber in Section 2.2. The chamber is also sealed and additional tubing is employed inside to ensure fast and reliable delivery of the gas analytes to the CNT sensor chip (Figure 9(b).)

The real-time sensing operation of the CNT sensors as well as the proper functionality of the CMOS interface can be seen from Figure 10. Notice that the resistance change in sensors due to the change in chemical concentration is reflected in the low frequency change in resistance. The high frequency component of the transient response is due to the intrinsic noise in CNT devices [10].

Since the CNT sensors do not consume any active power, the total power consumption of the designed chemical sensor system is at maximum $32\mu W$, enabling deployment of the developed system in a sensor network environment. It is important to note that the characteristic of CNT sensors varies significantly from tube to tube. From Figure 2, the ΔR-R_0 curve is linear but does not pass through the origin due to a non-zero minimum value of the baseline resistance R_0. Hence, the magnitude of $\frac{\Delta R}{R_0}$ tends to be larger for larger values of R_0, which is reflected in Figure 10. However larger deviations seem to exist from this trend for smaller values of R_0 because such devices are likely composed of multiple CNTs. Since the NO_2 - CNT binding energy is known to vary depending on the type of CNT [11], devices with multiple CNTs tend to exhibit larger variations from the general trend. This justifies the use of multiple

	Meas. Error	Resistance Range	Readout Rate	Power Consumption
Malfatti *et al.*[2]	$< 0.5\%$	$500K\Omega \sim 1G\Omega$	Not Available	$3.1mW$
Grassi *et al.*[7]	$< 0.14\%$	$100\Omega \sim 20M\Omega$	$100Hz$	$6mW$
Flammini *et al.*[8]	$< 0.5\%$	$10K\Omega \sim 10G\Omega$	Depends on Res.	$600mW$
Frey *et al.*[9]	$< 0.2\%$	$3K\Omega \sim 12M\Omega$	$3kHz$	$\sim 130mW$
This work	$\mathbf{< 1.32\%}$	**10KΩ ∼ 9MΩ**	**1.83kHz**	**32μW**

Table 2: Comparison of published sensor interface circuits

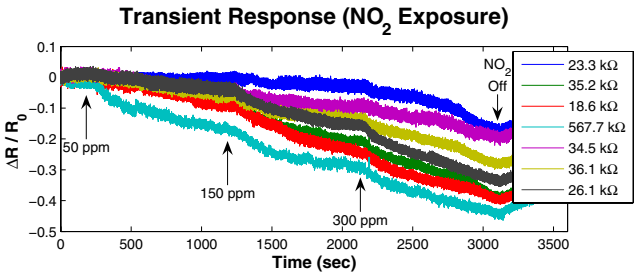


Figure 10: The CNT resistance change detected with the interface circuitry. Experimental conditions (gas exposure time, chamber size, and device geometry) differ from that in Fig. 2.

CNT sensor devices, which span across a wide dynamic range, to sense the chemicals in the frontend. Standard pattern recognition and machine learning techniques can be used to infer the chemical concentration from the resistance measurement data [12].

6. CONCLUSION

A low power chemical sensor system using carbon nanotubes as the sensing medium is presented. Extending the dynamic range using an automatic gain control, along with on-chip digital calibration of analog components, can be achieved with low energy overhead as presented. To overcome the variability of the CNT sensors, multiple sensors are deployed to sense the chemical, and standard pattern recognition techniques can be used to infer the chemical concentration in the presence of sensor noise.

This work can be extended to develop a single-chip solution of chemical sensor system by bringing reference resistors on-chip and packaging carbon nanotubes on-die. Packaging carbon nanotubes on-die can be done by transferring grown carbon nanotubes to pads that are otherwise wire-bonded. The single chip solution will decrease the cost of the developed system, which will increase the possibility of mass deployment.

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