Design and Characterization of CNT-CMOS Hybrid Systems

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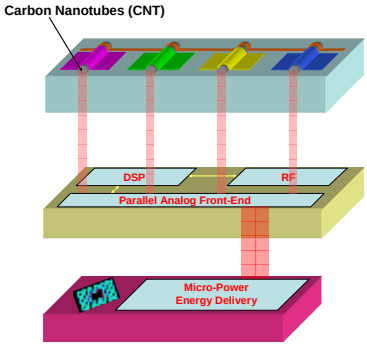
Motivation

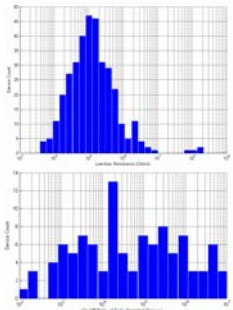


Motivation

- Hybrid CNT-CMOS systems can be used for a wide range of applications (e.g., sensors, RF circuits, power electronics, etc)
- Focus of this study is to develop circuit models, enhanced fabrication methods, and integrated systems

Design Challenges

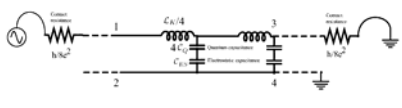
- Interfacing CNT with CMOS
- System-level CNT interconnect characterization and optimization
- Selectivity of metallic vs. semiconducting CNTs
- Enhanced fabrication methods to reduce performance variability



Logarithmic variation of (a) Low-bias resistance (b) Current On-Off ratio of fully depleted devices (Single-walled Nanotube devices with Au contacts / in collaboration with Daniel Nezich)

Verification of the CNT Interconnect Model

CNT Transmission Line Model

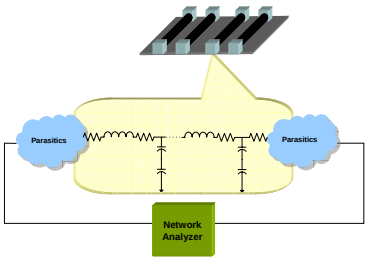


L_K ~16nH/μm, C_Q ~100aF/μm, C_{ES} ~50aF/μm

P. Burke, IEEE Trans. Nanotechnology 2002

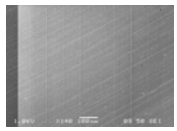
- The existence of kinetic inductance and quantum capacitance is predicted
- Measurement of L_K and C_Q, and $R_{scatter}$ is required to use the model in circuit design / simulation

Measurement Setup

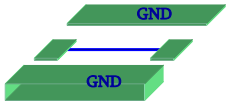


Challenges

- Large parasitics overwhelm the capacitance of interest => Highly accurate deembedding technique should be developed. Previous work on deembedding can be reference in Tiemeijer et al, IEEE MTT 2005
- Long CNT (in the order of centimeter) is preferable to increase the accuracy of the measurement => Fabrication technique to grow long tubes will be developed



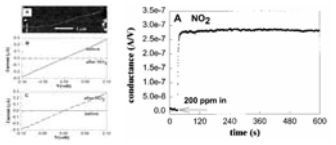
Courtesy of A.Cecco, J. Kong



Test Structure for Deembedding

CNT-CMOS Chemical Sensor System Design

CNT Chemical Sensor Characteristics



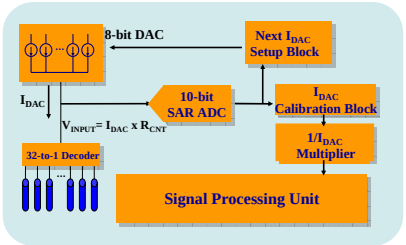
J. Kong et al, Science 2000

- CNT is a potentiometric chemical sensor
- CNT does not have to be heated to function as a sensor
- Coating will enable selectivity to the chemicals of interest.

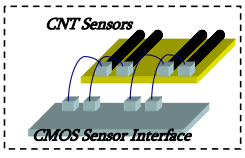
Interface Specification

Resolution	1% change from the base resistance
Dynamic Range	10kOhm ~ 10MOhm (17-bits)
Maximum Current	~ 30uA/cell

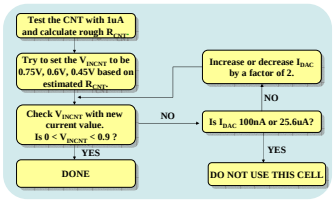
CMOS Interface Architecture



System Concept



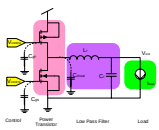
Resistance Level Calibration



- Division of large dynamic range requirement into sub-blocks of smaller dynamic range.
- All Digital DAC Calibration using reference resistors
- Real-time update of I_{DAC} for individual CNTs

CNT in DC-DC Converter

DC-DC Converter Circuit



- Main Power Losses

$$P_{conduction} = I^2 R_{on\text{-}p} \tau_p / T + I^2 R_{on\text{-}n} \tau_n / T$$

$$P_{switching} = \frac{1}{2}(C_{gp} + C_{gn} + C_{diode}) V^2_{battery}$$

$$P_{leak} = I_{leak} V_{battery}$$

$$\eta = \frac{I_{load} V_{out}}{P_{conduction} + P_{switching} + P_{leak}}$$

Power Transistor Fabrication Using CNT

- Device Schematic
- AFM image of CNT film
- Device Array Mask

Advantages of CNT Circuit

- Transistors made of bundles of nanotubes and that work in ballistic transport region can have smaller R_{on} and C_g which corresponds to lower loss of the converter

Sponsorship: DARPA / MARCO Interconnect Focus Center