Low Noise Amplifier – 6.776 Lab 1

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Introduction

Low-noise amplifier plays a critical role in the design of Radio Frequency (RF) system because the channel capacity depends on the signal to noise ratio of the information being received. In this lab, we have designed a low-noise amplifier that operates at 5V supply with power budget of 5mW. In the course of implementation, however, a number of issues arose due to relatively low output resistance of JFET's and finite input resistance of passive probes.

Section 1: Basic Architecture

We have chosen common-gate configuration (Fig. 1) to implement our LNA due to several reasons. First of all, because the input impedance is quite high and does not vary too much from transistor to transistor (Zin ~ 1/gm), we can reliably match the input resistance quite easily. Secondly, the frequency response of the common-gate configuration is much better than that of common source because the common-gate configuration does not suffer from the miller effect of Cgd. Thus, even without cascode transistor, we can implement high-frequency amplifier with sufficient gain.

In our preliminary circuit (Fig. 1), we used a single transistor to obtain enough gain to meet the specification. As you can see in Fig.1, the DC voltage at source is not exactly at ground so that in order to use the common gate configuration, we need to provide a DC decoupling cap between the input voltage source and the source of the JFET. This decoupling capacitor can actually be amortized into the input impedance transformer, and in order to do so, we have adopted the tapped - capacitor matching network for our amplifier. In the tapped - capacitor configuration, one capacitor blocks the DC signal while it also acts as a voltage multiplier, which is exactly what we want.

Assuming that the input impedance transformer is lossless, the power gain from the input of the matching network to the input of the amplifier is 1. This actually signifies that, because the input impedance of the amplifier is not 50 Ohm, but rather bigger (from the simulation) than 50 Ohm, we can anticipate to attain some voltage gain from the input impedance matching network as well.

Section 2: Simulation Results

Here is a summary of the simulation results.

Criterion	Specification	Simul. Result
Supply Voltage	5V	5V
Load	10pF/1M	10pF/1M
Power Diss.	<5mW	4.2mW
Gain	>25	59.1
3dB BW	>200kHz	228kHz
Center Freq.	50MHz +- 10%	53.83MHz
Input Impedance	50 +- 10	47.94 + j1.52
NF	<6dB	2.296dB
Output Swing	>100mV	> 100mV

As you can see from above, we can easily meet the specification with a single transistor. This actually improves the noise figure drastically that we can achieve about 2dB of Noise Figure. Furthermore, the input impedance matching network actually does give us some gain, and in our case it was around a factor of 3. The plots are attached at the end of the report (Figure 2, 3, 4, 5, 6)

Section 3: Measurement Result

We have implemented our circuit on the vector board to verify the functionality with J310 JFET's as our transistors. However, we only attained a gain of 6. Part of it was due to finite Q in inductors and capacitors that we ignored in the preliminary simulation, and furthermore, the output resistance of the JFET was very small. When we measured the output resistance of the discrete J310, the value was 2.6 kOhm. By taking these effects into account in the simulation, we only attained the gain of 12, which includes the voltage gain at the input impedance transformer. Gain from the active stage itself was about 6, which is in accord with numerical analysis. If we do the small signal analysis for common-gate configuration, the gain is given by

$$G = \frac{V_{out}}{V_{in}} = \frac{\frac{R_L}{r_0} + R_L g_m}{\frac{R_L}{r_0} - 1} = \begin{cases} \approx 1 + g_m r_0 & R_L \text{ is large} \\ \approx -R_L g_m & r_0 \text{ is large} \end{cases}$$

Thus, the gain of the active stage becomes 1+2m*2.6k≈6.2. In order to overcome such problem with low output resistance of JFET's, we decided to add another transistor in a cascode configuration so that we can minimize the effect of small output resistance in JFET's. Small signal analysis of cascoded amplifier (Fir. 5) gives the gain of

$$G = \frac{V_{out}}{V_{in}} = \frac{(1+g_m r_0)^2}{\frac{r_0}{R_L}(2+g_m r_0)+1} = \begin{cases} \approx g_m R_L & r_0 \text{ is large} \\ \approx 1+g_m r & R_L \text{ and } r_0 \text{ are comparable} \end{cases}$$

Therefore, by introducing a cascoded transistor, we can recover the gain that is not influenced by gds factor as long as R_L is high. Unfortunately, the load resistance in these circuits can be quite low. For example, if we consider the finite Q in inductors, the effective resistance looking into the LC tank can be quite small. If Q of the inductor is 28 (worst case according to the datasheet), the effective resistance looking into the LC tank (assuming ideal C) is w_o * L * Q, where w_o is the center frequency, L is the inductance value, and Q is the Quality factor of the LC tank. If we plug in approximated numbers (L = 815nH) to see the order of magnitude, the effective resistance can only be 7.17kOhm.

Taking all these effects into account in doing the simulation on cadence, we attained the following values.
The plots are added at the end of the report (Fig. 7, 8, 9, 10, 11).

Criterion	Specification	Simul. Result
Supply Voltage	5V	5V
Load	10pF/1M	10pF/1M
Power Diss.	<5mW	4.9mW
Gain	>25	36
3dB BW	>200kHz	800kHz
Center Freq.	50MHz +- 10%	51.5MHz
Input Impedance	50 +- 10	50 – j2
NF	<6dB	4.2dB
Output Swing	>100mV	> 100mV

The simulation result shows that we can still meet the specification with low output resistance by using cascode configuration. You can see that the band-width increased because the effective load-resistance actually decreased. Based on these results, we have implemented our circuit on the vector board. However, we still could not reach the gain of 25. Some issues have been raised regarding the finite input resistance of passive probes. Because the input resistance of the passive probes was much lower than the specified value (1Mega Ohms), the gain was degraded by more than a factor of 5. This was verified by using an active probe to measure the signals at different points in circuit.

Furthermore, because we didn't have inductors and capacitors of values we want, we had to connect inductors and caps in series and parallel. However, by connecting the discrete inductors in series, we can degrade the Q factor by

more than a factor of 2. This actually results in even lower gain in our amplifier.

As of March 23, 2006, we are still working on possible ways to increase the load impedance of the amplifier to increase the gain. Apart from the gain, we have met all the specifications, and they are summarized as below.

Criterion	Specification	Meas. Result
Supply Voltage	5V	5V
Load	10pF/1M	10pF/1M
Power Diss.	<5mW	4.8mW
Gain	>25	7
3dB BW	>200kHz	>1MHz
Center Freq.	50MHz +- 10%	50MHz
Input Impedance	50 +- 10	53 + j3
NF	<6dB	N/A
Output Swing	>100mV	> 100mV

Figures

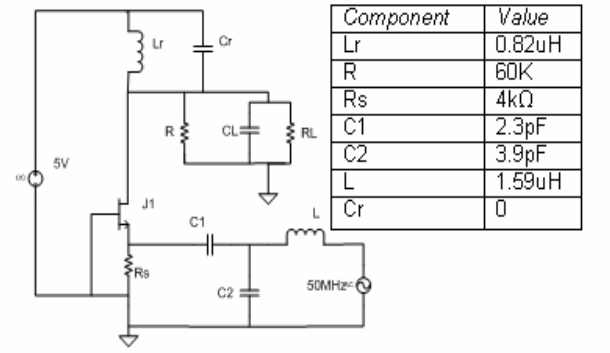

Figure 1. Schematic of Our Original Design

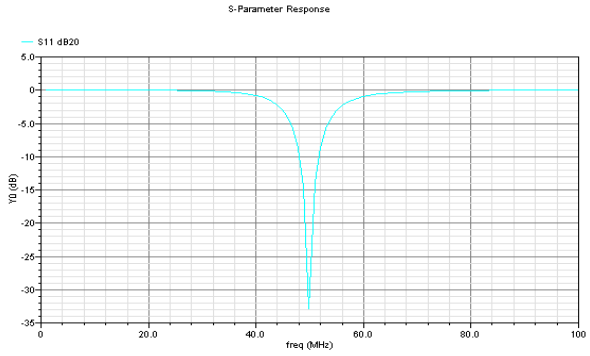

Figure 2. S11 of the Amplifier

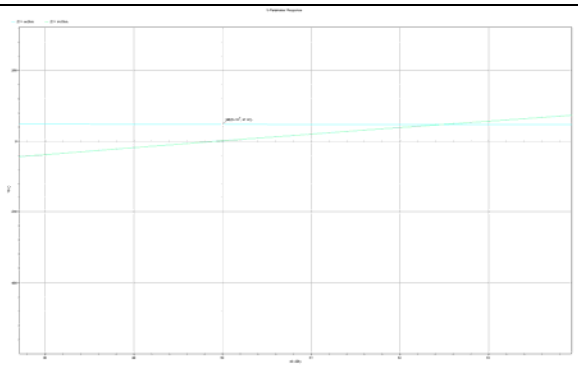

Figure 3. Input Impedance of the Amplifier

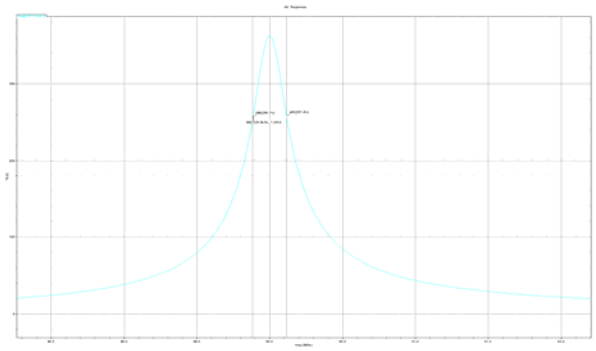

Figure 4. Bandwidth

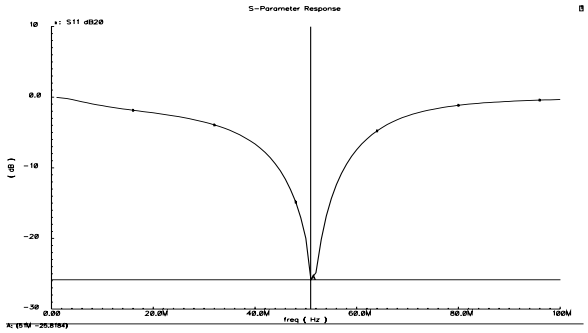

Figure 8. S11 of the Amplifier

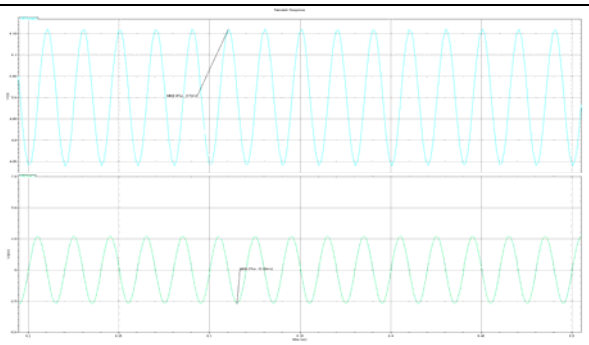

Figure 5. Gain

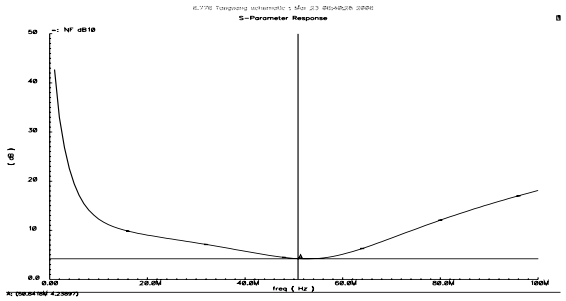

Figure 9. Noise Figure

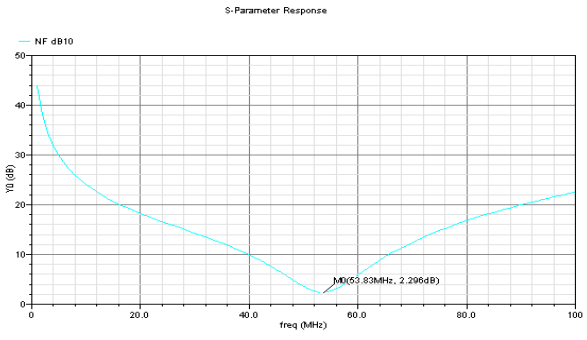

Figure 6. Noise Figure

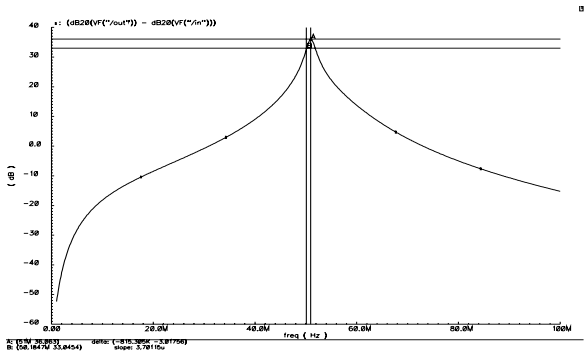

Figure 10. Bandwidth

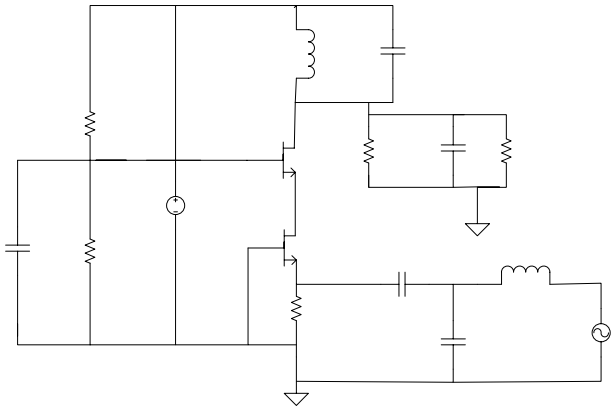

Figure 7. Modified Circuit – Cascode version

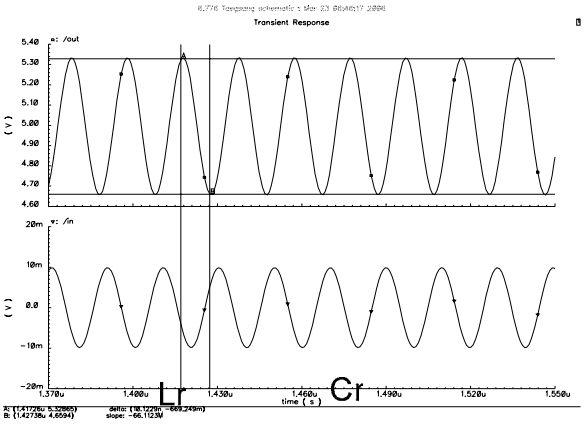

Figure11. Gain

R1

R

CL

RL

5V

DC

J1

R2

L

C1

C

Rs

50MHz

AC

C2