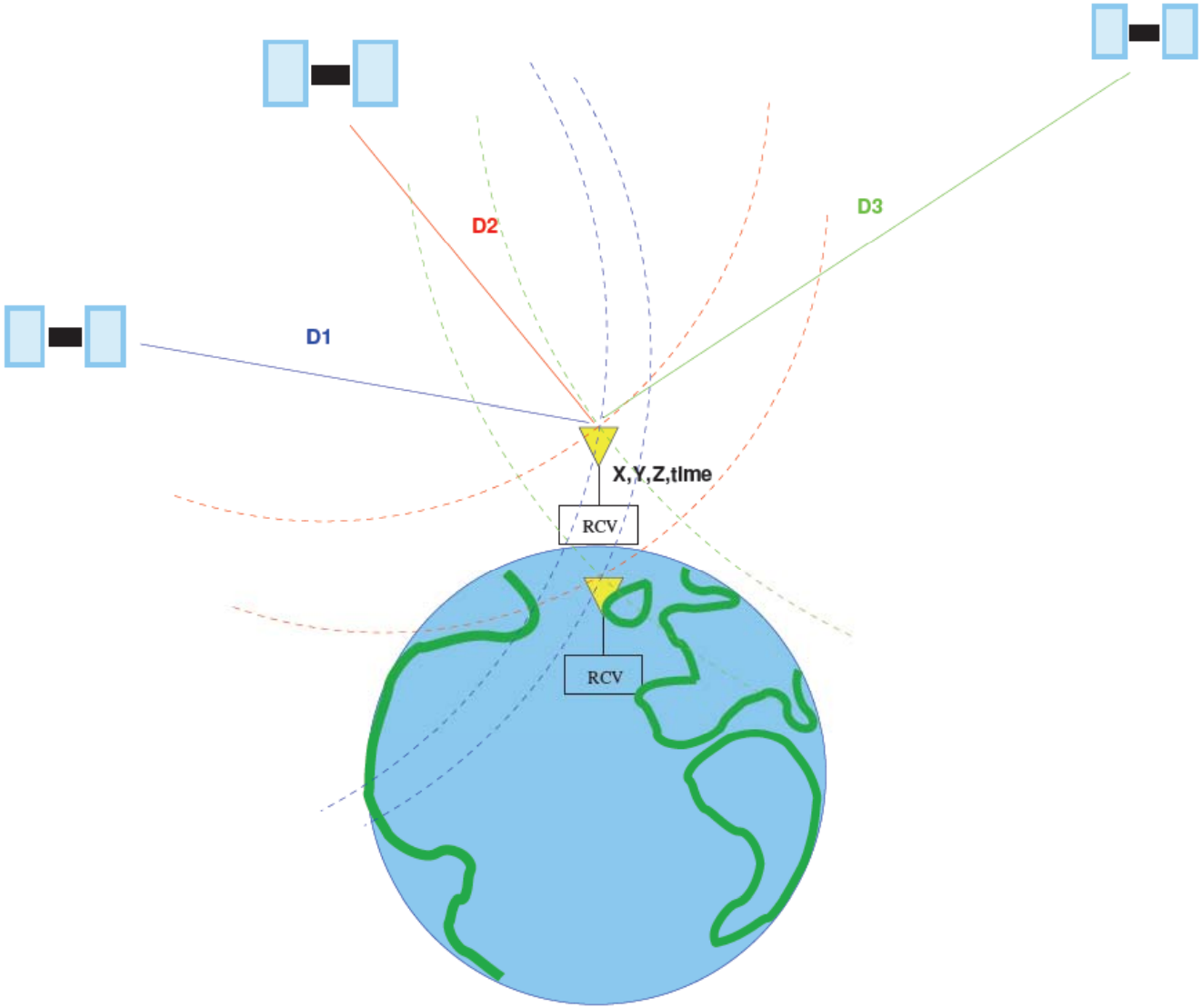
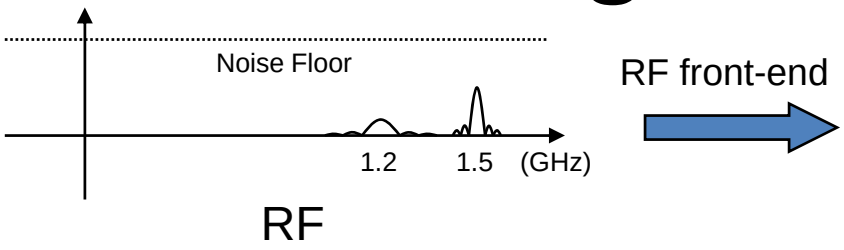

Down-conversion and Correlation Engines for GPS Receivers
- A Low Power Solution

# GPS System

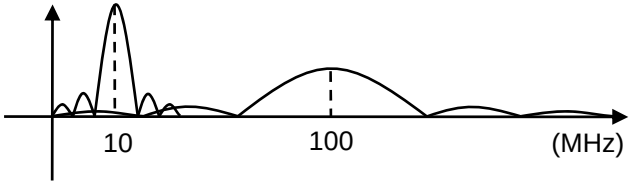


# GPS Signal Processing



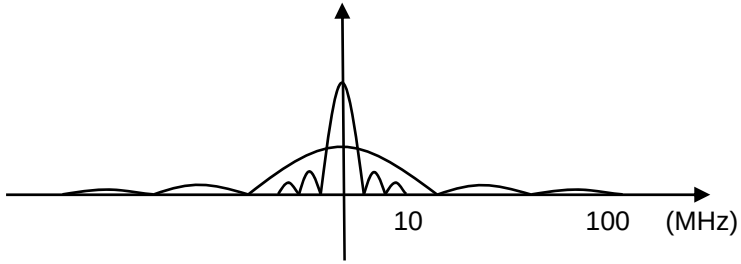

RF

RF front-end



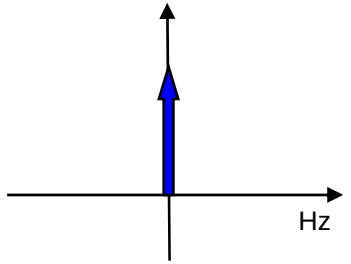

IF

Down conversion



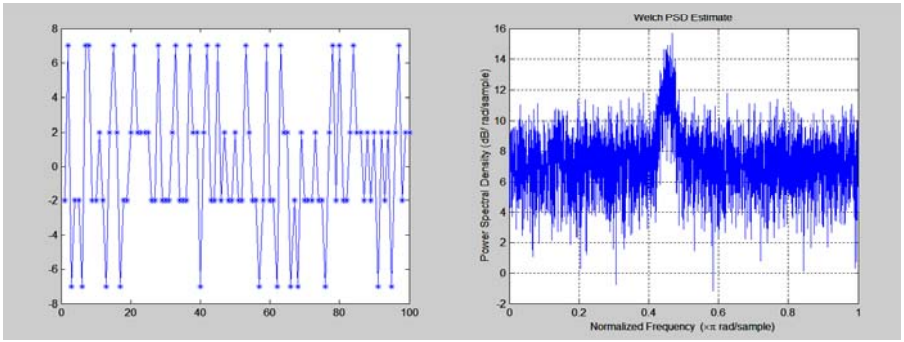

Baseband

Code remove & Despreading

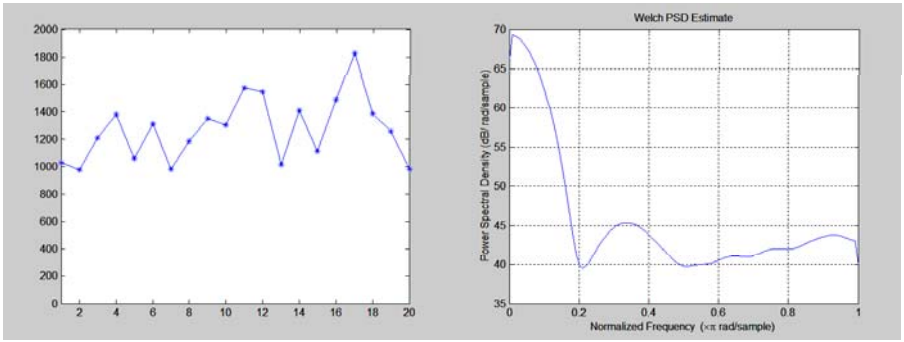



Narrow Band

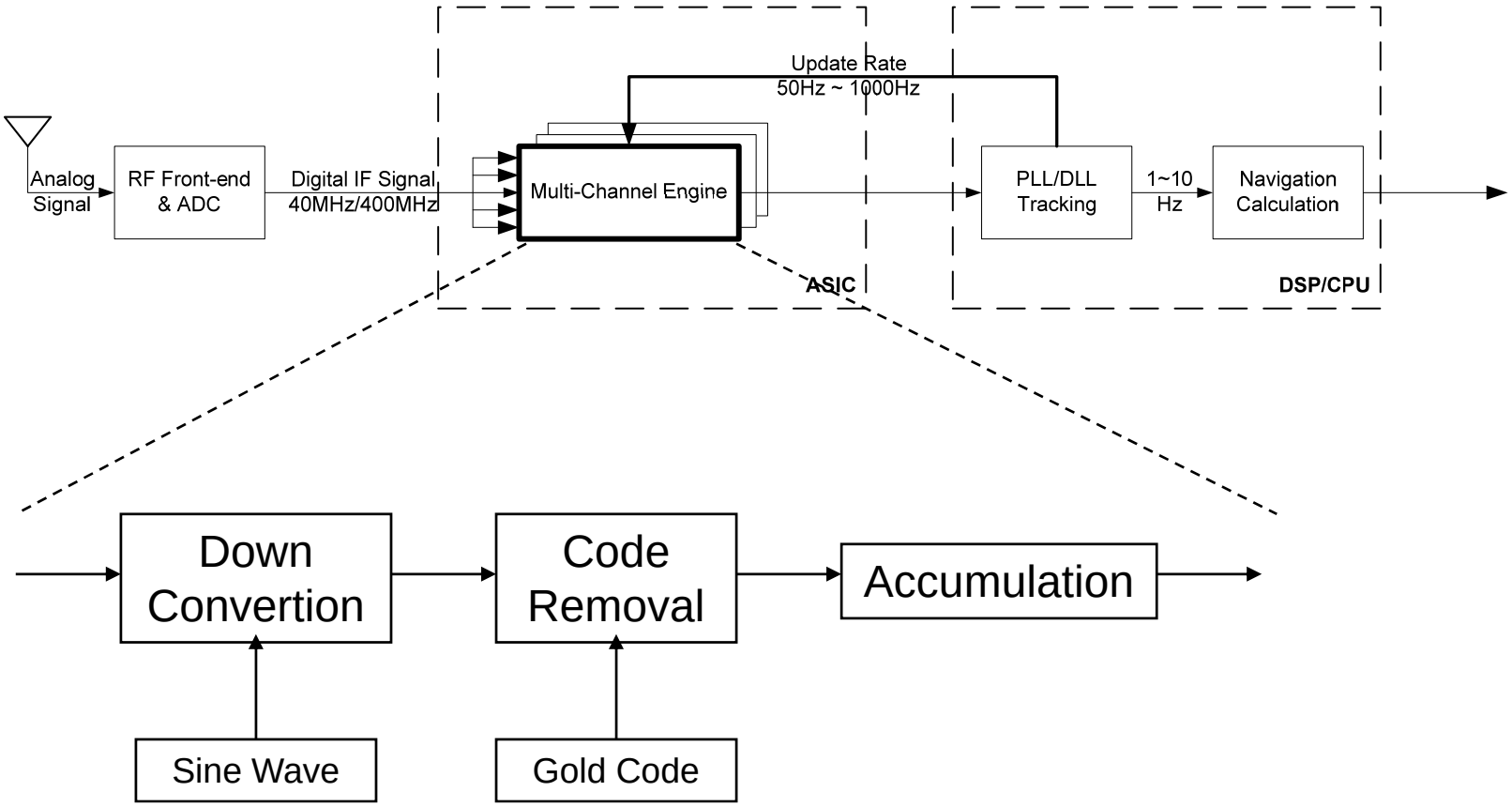
GPS Engine




Processing



# GPS Receiver

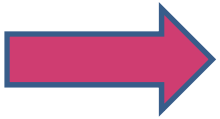


# Design Process

| Software Tools | Matlab | Verilog | RC Compiler | Cadence | NanoSim |
|---|---|---|---|---|---|
| Purpose | Algorithm Simulation | Circuit Design | Circuit Synthesis | Verification & Measurement | |
| | | | | | |
| Files Generated | Testing Vectors | Hardware Description | Synthesized Circuit | HSpice Netlist | Waveforms |

# A Low Power Design

$P=CV_{DD}^2 f$

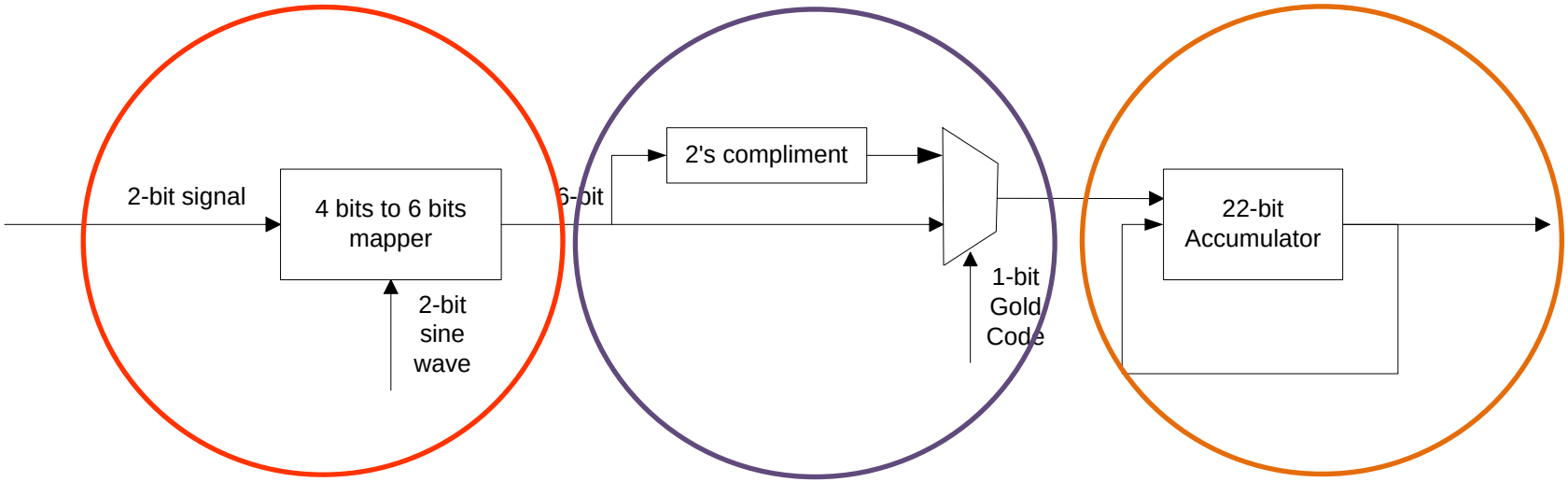


Voltage Scaling

Pipelining?

Parallelism?

# Sequential Implementation

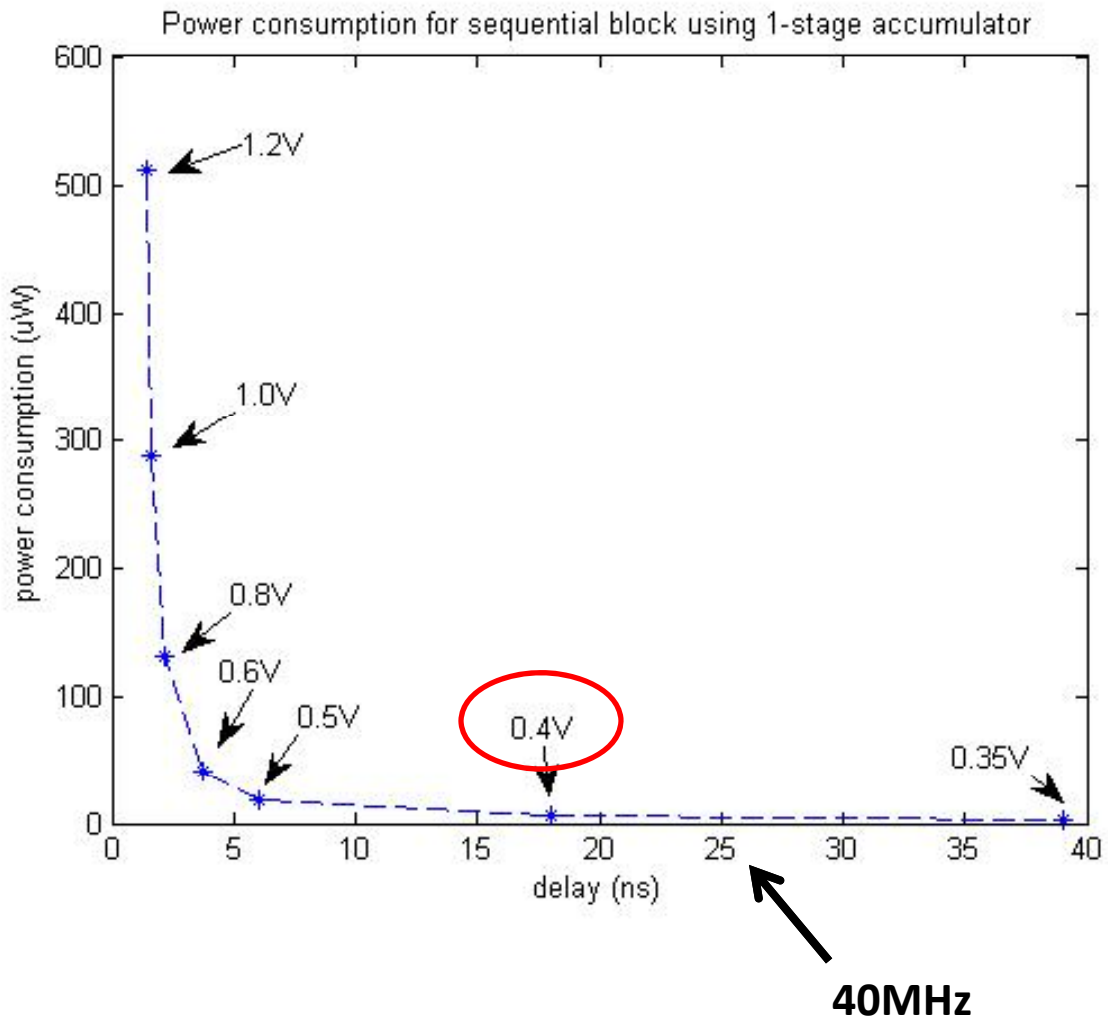



Down Conversion

Code removal

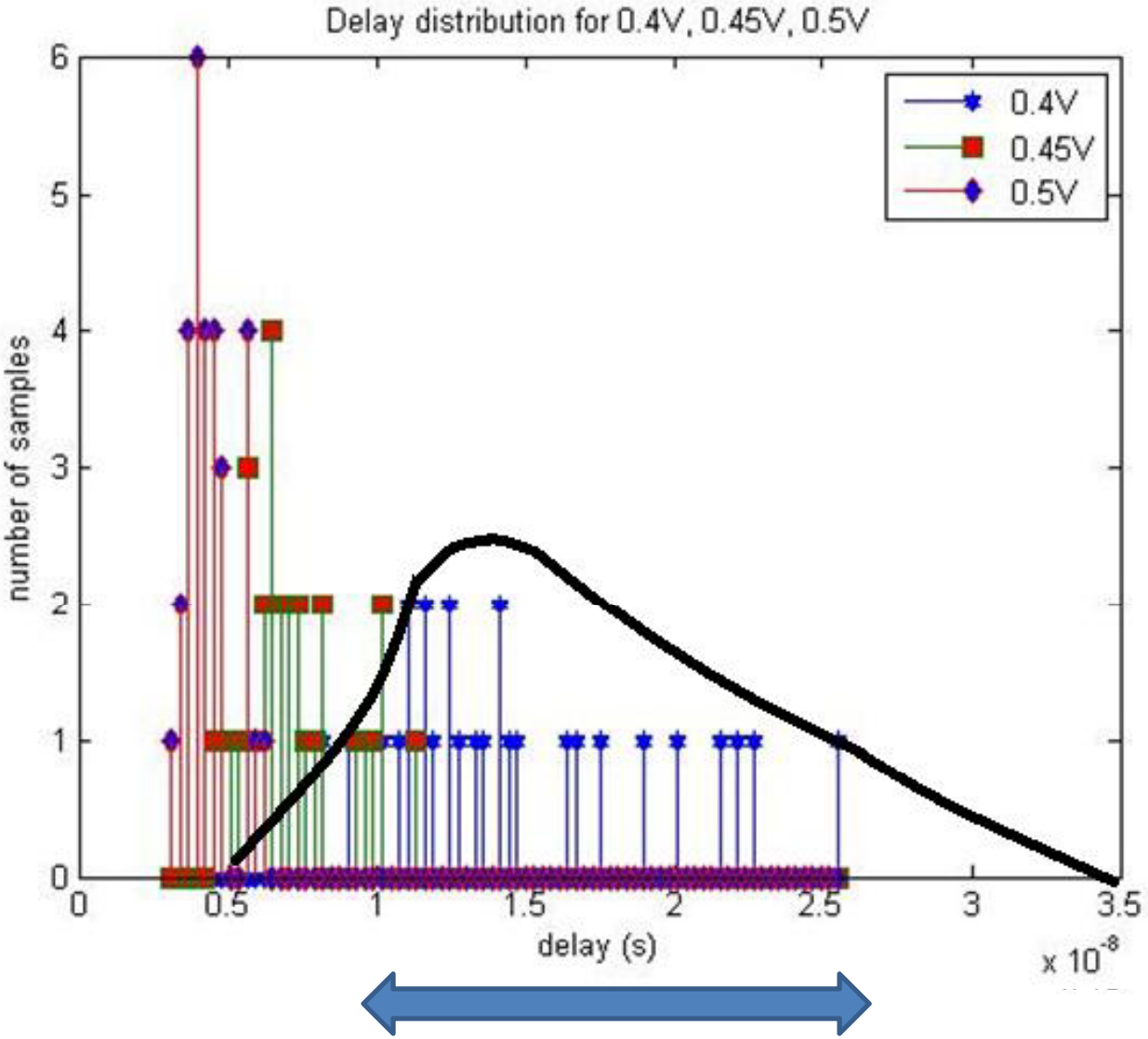
Accumulation

# Dealing with 40MHz




No parallel paths needed

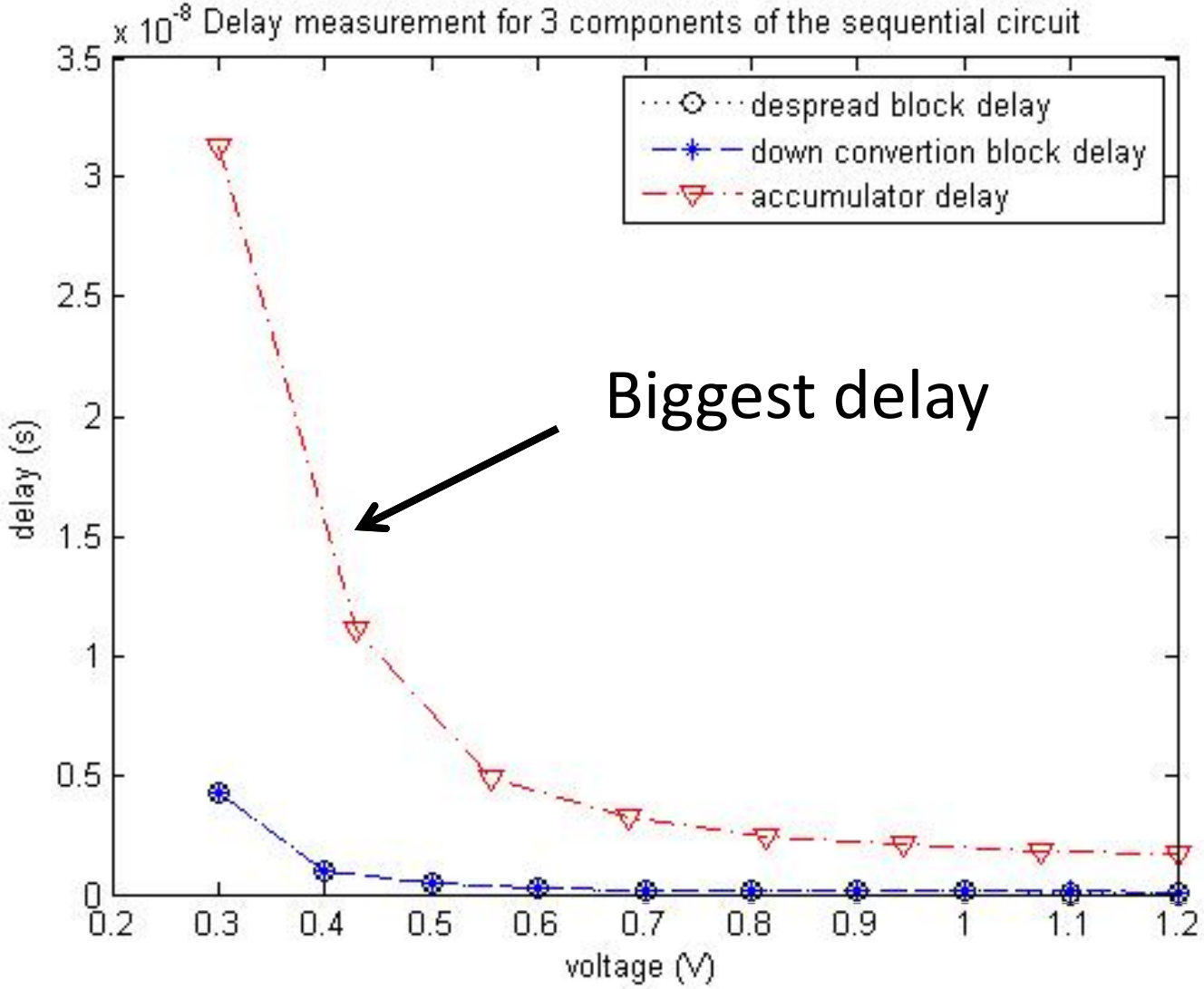
# Reliability Problem



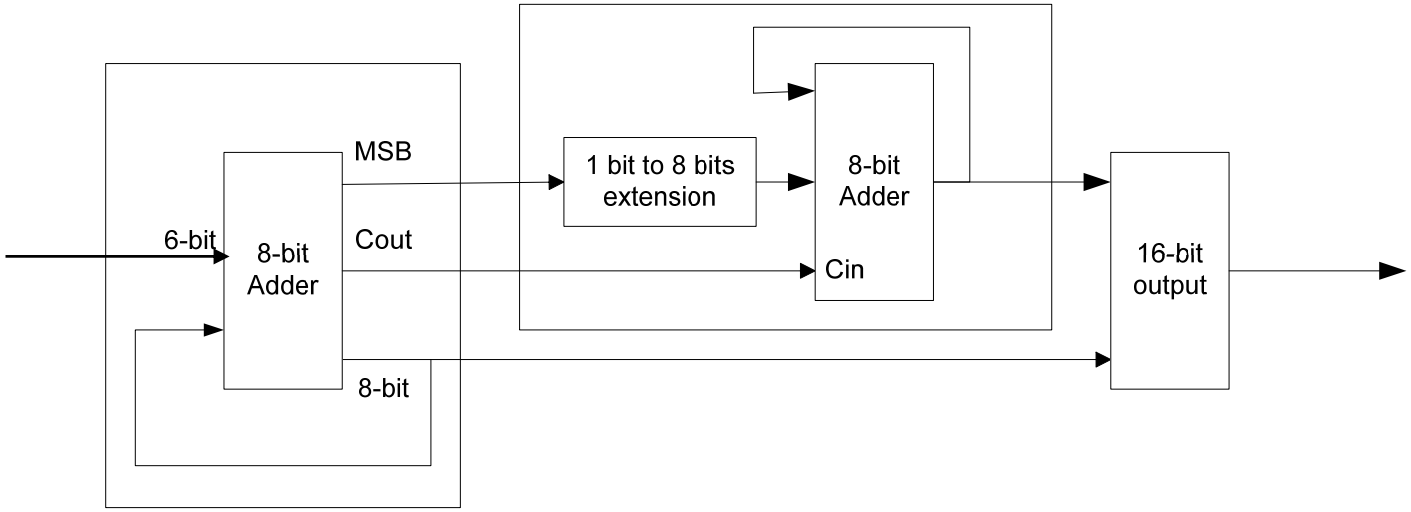

**Monte Carlo**

Need to reduce delay

# Reduce whose delay?

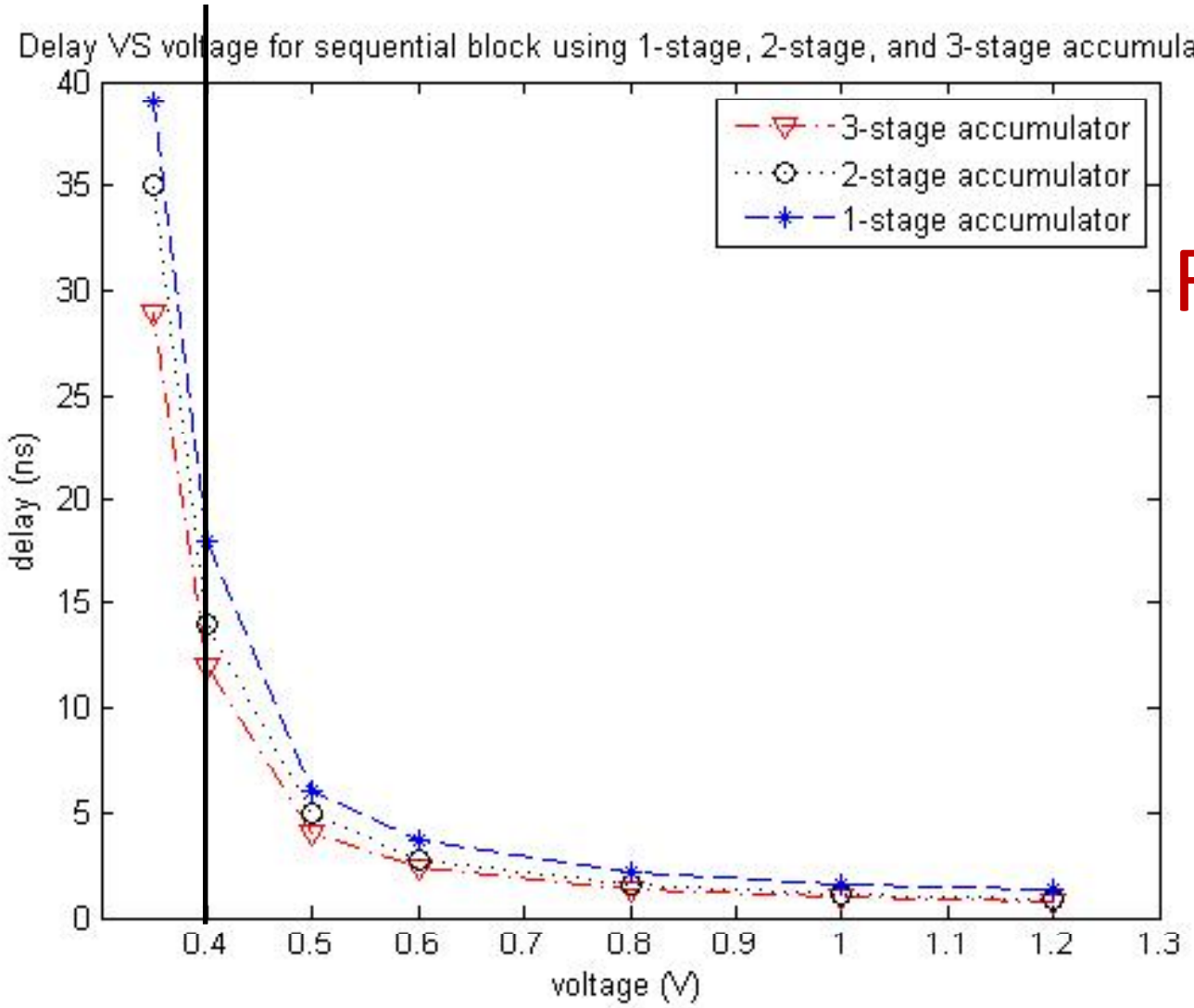


# Pipeline the Accumulator!!!




2-Stage Pipelined Accumulator

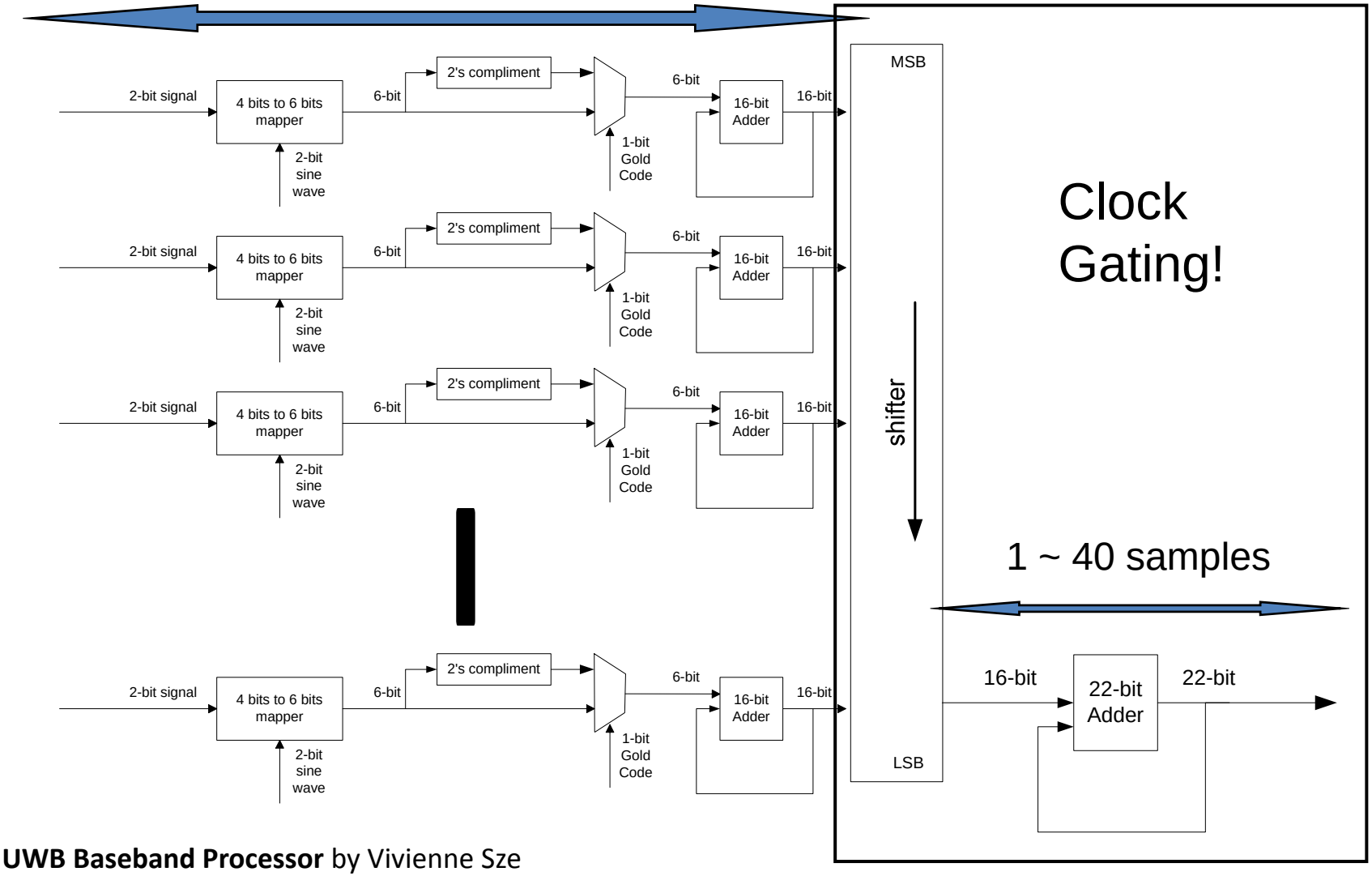
# Pipeline the Accumulator




Reliability

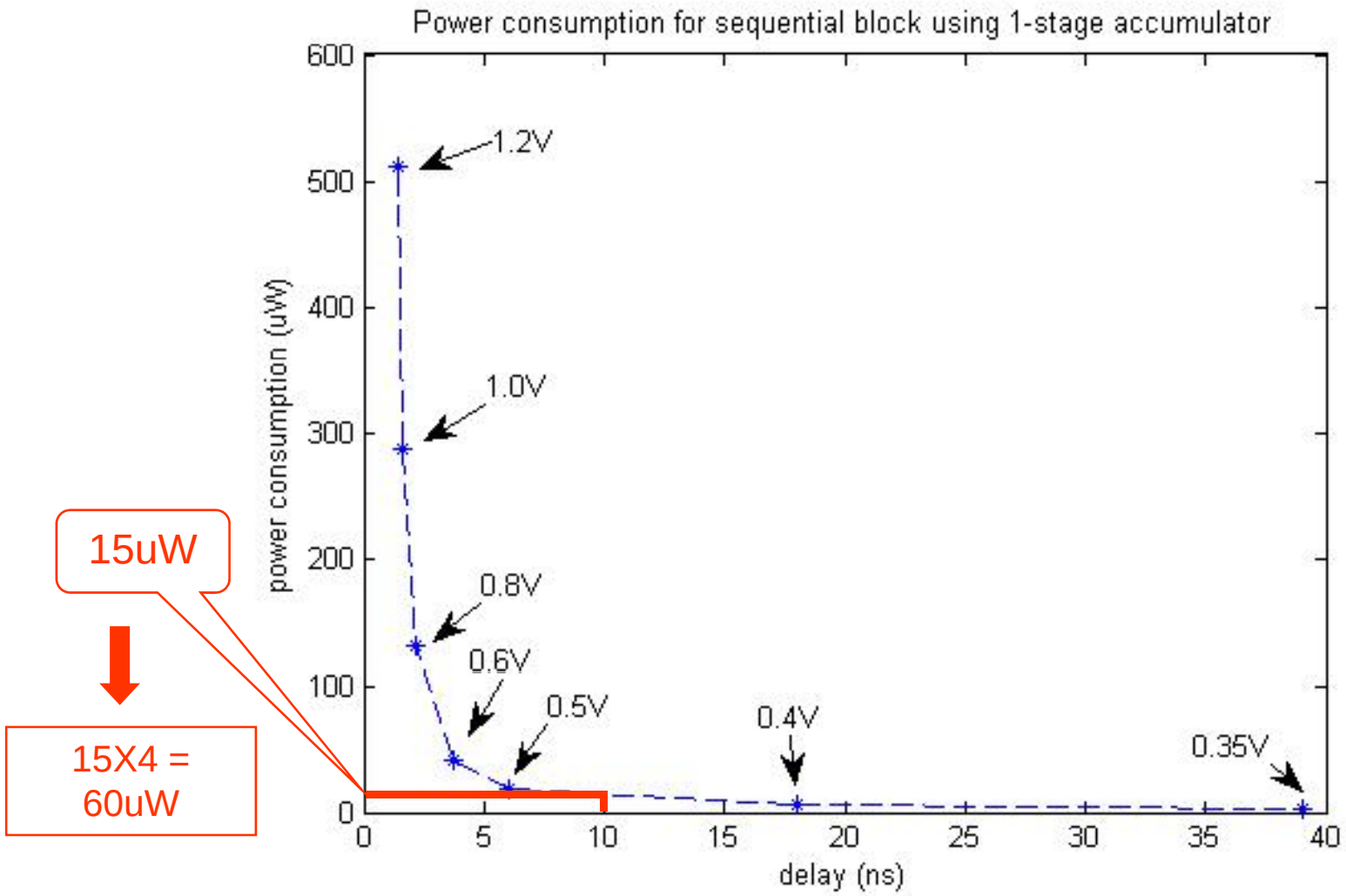
# Parallel Implementation

1ms, or 1023 chips, or 40,960 samples, or 409,600 samples

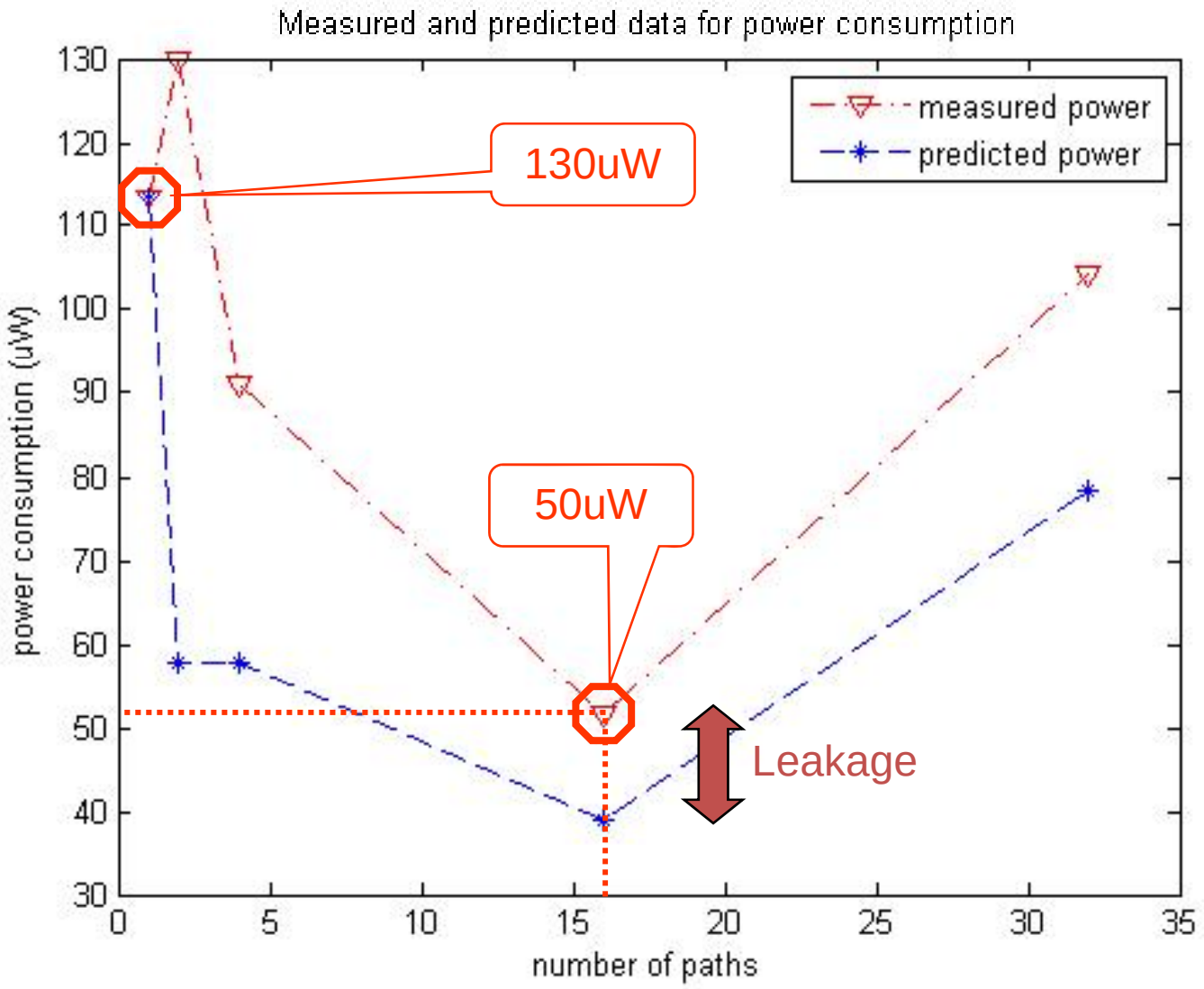



**A 0.4-V UWB Baseband Processor** by Vivienne Sze

# Estimation of Power Consumption



# Power Consumption for 400MHz Receiver



# Conclusion

40MHz -- pipelining

400MHz -- parallelism

# Future Work

- Leakage Problem
- Power gating to shifter and 2nd accumulator
- Layout
- Assistant circuit blocks
  - Harmonic wave generator
  - Gold code generator
- Better power v.s path plot