

# **Computer-based project in VLSI Design**

## **First Interim Report**

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## CMOS logic gates design

A ring oscillator is studied and designed behaviorally in the first three labs. A ring oscillator is comprised of an odd number of inverters, each adding some delay, which causes the structure to oscillate. Each inverter is a NOR gate, which is comprised of CMOS logic gates. Figure 1 and Figure 2 in the appendix show two examples for CMOS logic gates design.

To achieve equal worst-case delays for rising and falling edges, transistor dimensions have to be matched. Choose  $W$  and  $L$  as low as possible to reduce the transistor dimensions. The dimension of each MOSFET is indicated next to it in the figures. Delay of each CMOS gate is calculated by dividing the total delay of the ring oscillator by the number of stages. This method offsets the reading inaccuracy and error when measuring the delay of one gate. However, since the loading of the last stage may be quite high, delay measured this way is higher than the actual value. If each of the gates used has delay  $\tau_r$  for rising edge and  $\tau_f$  for falling edge, the oscillation frequency ought to be  $\frac{1}{n(\tau_r + \tau_f)}$ . The frequency of a ring oscillator can be changed by varying the rising and falling times of NOR gates. This can be done by varying the conductance of MOSFETs, which can be changed by varying the  $\frac{W}{L}$  ratio. In a ring oscillator, each inverter stage adds a delay, which gives the basic frequency  $f = \frac{1}{2n\tau}$ , given that both the rising and falling times are  $\tau$ . Therefore, it is not possible for a ring oscillator to oscillate at any other basic frequency than  $\frac{1}{2n\tau}$ . A ring oscillator with an even number of gates cannot oscillate. The output signal in this case is the same as the input signal. When the output is fed back to the input, a stable state is reached, and the signal cannot oscillate. Only when there is an odd number of inverter stages can the ring oscillator oscillate.

## Structure of a ring oscillator

29 NOR gates are connected in series to make a ring oscillator that fits the specifications. OUT1 is taken after the first 9 gates, and OUT2 is taken after the first 25 gates. Figure 3 in the appendix shows how the NOR gates are connected to form a ring oscillator. Period of oscillation is  $n(\tau_r + \tau_f) = (29 \times (2.7 + 2.8)) = 159.5ns$ . The measured value is  $495 - 321 = 174ns$ . Both the theoretical and experimental values are within the allowed limit ( $145ns - 185ns$ ). Delay from ENB to OUT1 is  $\frac{7 \times (2.7 + 2.8)}{2} = 19.25ns$ . The measured value is:  $321 - 300 = 21ns$ . Both are within the allowed limit ( $12ns - 21ns$ ). Delay from OUT1 to OUT2 is  $\frac{18 \times (2.7 + 2.8)}{2} = 49.5ns$ . The measured value is:  $375 - 321 = 54ns$ . Again both are within the allowed limit ( $40ns - 60ns$ ). Graph 1 in the attachment shows the working ring oscillator. After changing the rising time to be 3 times as big as falling time, ( $\tau_r = 9ns$ ,  $\tau_f = 3ns$ ), the oscillation period got bigger, to  $348ns$ . The delay from ENB to OUT1 also got bigger, to  $45ns$ , and the delay from OUT1 to OUT2 increased as well, to  $108ns$ . This is due to the increased delay caused by the bigger rising time of each inverter stage.

## Short double pulse to ENB

A short double pulse is fed into the ENB port. Whether the ring oscillator propagates this double pulse depends on the state of input that is fed into the first NOR gate. If this short double pulse is fed into ENB after  $300ns$ , OUT2 is low, the input going into the first NOR gate is also low. The NOR gate propagates and inverts the enable bit. This is why we can see the higher harmonics in Graph 2 in the appendix. However, in the case of feeding the double pulse after  $400ns$ , OUT2 is high, the input going into the first NOR gate is also high. Then NOR gate blocks anything coming from ENB, and thus the double pulse cannot propagate. This can be observed in Graph 3.

## 4-bit counter

OUT1 from the ring oscillator is connected to a 4-bit counter so that a dividing by 16 counter is formed. The counter counts both the rising and falling edges of the OUT1 waveform coming out of the ring oscillator. It starts counting from 0000. After it counts to 1111, which is equivalent to half of a period, it sets the clk\_out to be opposite of the current value. A working dividing by 16 counter can be found in Graph 4 in the appendix. After the oscillator is enabled, clk\_out is 16 times slower than OUT1.

## Comparator and programmable counter

A comparator is constructed to compare data.a and data.b. Some waveforms that indicate a working comparator can be found in Graph 5 in the appendix. Then a programmable counter is constructed by counting both the rising and falling edges of the clock. The counting result is fed into the comparator to compare with a pre-supplied divider. If they are equal, flip the bit in output. The result can be seen from Graph 6 to 8 in the appendix. As shown, the programmable counter can deal with both even and odd numbers.

## Programmable divider

Finally, the ring oscillator is connected to the programmable divider. The ring oscillator simply replaces the role of the clock in the previous part. Graph 9 to 11 in the appendix show the result of the complete design. In Graph 9, the divider is dividing by 5. When the ring\_osc\_enb is high, OUT1 is disabled, and the counting stops. In Graph 10, the divider is dividing by an even number, 4. After there is a pulse in reset, the counter is successfully reset back to 0. In Graph 11, the divider is dividing by 3. When the ring oscillator enable is high, counting is disabled. After the reset goes high then back down, the counter is set to 0. The divider works as desired.

## Transistor level design

Transistor schematics are studied. A printout of a NOR CMOS schematics can be found in Graph 12 in the appendix. Ports A and B are input ports. Y is the output port.  $Y=A \text{ NOR } B$ . The bottom two transistors are N type, and the top two transistors are P type. The fourth electrode shown on each transistor is the back (or substrate). For N type transistors, the back is connected to the lowest point of the circuit, and for P type transistors, the back is connected to the highest point of the circuit. Threshold voltage of a MOSFET depends on  $V_{BS}$ . Connecting the substrates this way shown in the graph minimizes  $V_{BS}$ , and thus reduces the effect it is to the threshold voltage.

Table 1 in the appendix indicates the state of conduction or non-conduction for each transistor with every possible combination of logic inputs. It is confirmed that the logical function of the gate is two input NOR gate.

Information like the threshold voltage and dimension of each transistors  $\frac{W}{L}$  are required to determine the transfer function of the gate output voltage as a function of input voltage.

The approximate conductance of each N type MOSFET is  $G = \mu_n C_{ox} V_{dd} \frac{W}{L} = 0.061 \times 8.2 \times 10^{-4} \times 5 \times \frac{7}{3} = 5.84 \times 10^{-4} \frac{F}{s}$

When one input is brought abruptly to logic 1, the falling time the N type MOSFETs need is  $\frac{3C}{G_n} = \frac{3 \times 0.1 \times 10^{-12}}{5.84 \times 10^{-4}} = 5.14 \times 10^{-10} s$ . If both inputs are brought abruptly and simultaneously to logic 1, the conductance of the overall device increases by 2, so the delay time decreases by a factor of 2. The delay time is  $2.57 \times 10^{-10} s$

The dimension of P type MOSFETs is chosen so that the output delay observed when both inputs are brought abruptly to logic 0 matches the falling delay when a single input is brought to logic 1. This means the conductance for each P type MOSFET is twice as much as that for each N type MOSFET. Assuming  $L$  is fixed at  $3\mu m$ , then  $G_p = 5.84 \times 10^{-4} \times 2 = \mu_p C_{ox} V_{dd} \frac{W}{L} = 0.023 \times 8.2 \times 10^{-4} \times 5 \times \frac{W}{L} = 9.43 \times 10^{-5} \frac{W}{3 \times 10^{-6}} \Rightarrow W = 3.7 \times 10^{-5} m$

CMOS logic circuits all have the property that when inputs are either at logic 0(ground) or 1(5V), there is no power consumption. Only when the inputs are transitioning (at around 2-3V), there is current drawn from the power supply, and thus power consumption. Power is only wasted if the inputs do not change abruptly. In the case of a ring array, assume the capacitance loading each NOR gate is the internal capacitance  $0.1pF$  plus the capacitance introduced by the next stage, which is given by 2 N-type and 2 P-type MOSFETs.  $C_{next} = C_{ox} \times (W_P \times L_P + W_N \times L_N) \times 2 = 8.2 \times 10^{-4} \times (3 \times 10^{-6} \times 7 \times 10^{-6} + 3.7 \times 10^{-5} \times 3 \times 10^{-6}) \times 2 = 2.16 \times 10^{-13} F$ . Therefore,  $C = C_{internal} + C_{next} = 2.16 \times 10^{-13} + 0.1 \times 10^{-12} = 3.16 \times 10^{-13} F$ . Power consumption is  $P = CV_{DD}^2 f = 3.16 \times 10^{-13} \times 5^2 \times \frac{1}{50 \times 10^{-9}} = 1.6 \times 10^{-4}$ . If there are 100,000 gates connected, the power consumption is  $15.8W$ , which is too much for such a small circuit.

## Appendix

$A$	$B$	$N_1$	$N_2$	$P_1$	$P_1$	$Y$
0	0	non-conducting	non-conducting	conducting	conducting	1
0	1	non-conducting	conducting	conducting	non-conducting	0
1	1	conducting	conducting	non-conducting	non-conducting	0
1	0	conducting	non-conducting	non-conducting	conducting	0

Table 1: State of conduction of MOSFETs due to different inputs

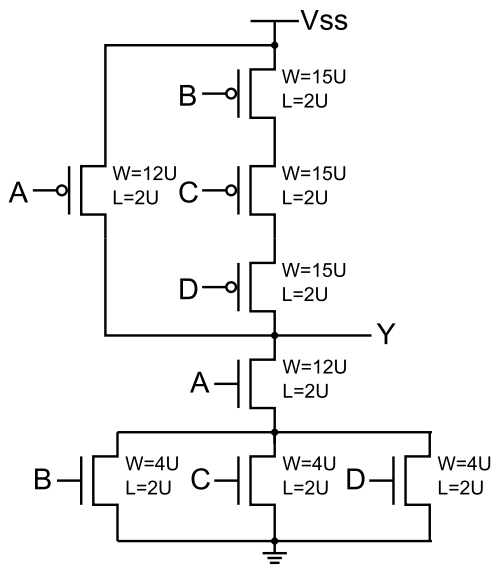


Figure 1:  $Y = \overline{A \cdot (B + C + D)}$

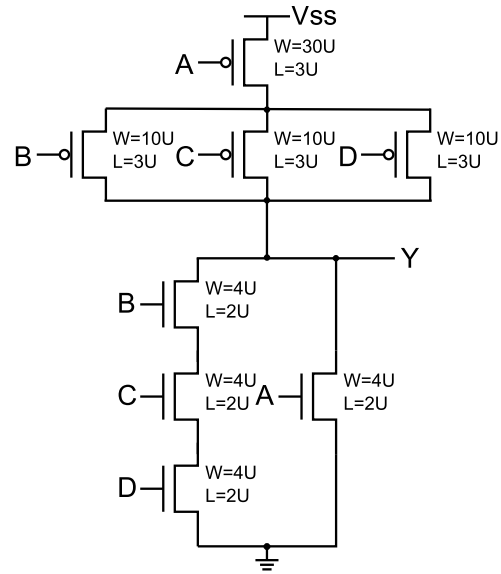


Figure 2:  $Y = \overline{A + (B \cdot C \cdot D)}$

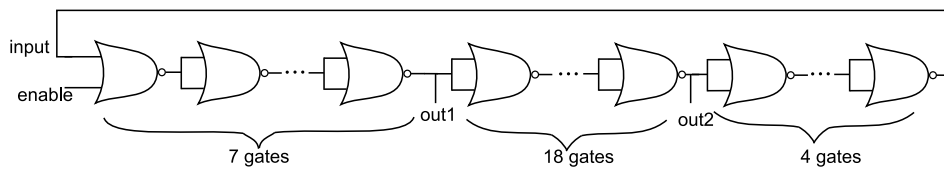


Figure 3: Design of the ring oscillator