Muralidaran Vijayaraghavan

Contact Information	32 Vassar Street 32-G822, Cambridge MA 02139	Mobile: +1 408 839 3356
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Interests Formal Verification, Computer Architecture, Concurrent Systems, Programming Languages, Proof Assistants

Programming Languages Haskell, C, C++
HDLs: Verilog, System Verilog, Bluespec
Proof Assistants: Coq

Work Experience

Postdoctoral Associate, CSAIL, MIT, under Adam Chlipala **Current**

Research Intern, IBM T.J. Watson, NY, under K. Ekanadham **Summer 2010**

Research Intern, Intel VSSAD group, MA under J. Emer **Summers 2007, 2008**

Education

Ph.D., EECS, MIT, Cambridge MA **GPA: 5.0/5.0** ***Feb 2016***

Thesis: Modular Verification of Hardware Systems
Supervisors: Arvind, Adam Chlipala

S.M., EECS, MIT, Cambridge MA **GPA: 5.0/5.0** ***Feb 2009***

B.Tech., CS, IIT Madras, Chennai India **GPA: 9.53/10** ***June 2006***

Selected Publications

Choi J., Vijayaraghavan, M., Sherman B., Chlipala A., Arvind "Kami: A Platform for High-Level Parametric Hardware Specification and Its Modular Verification" *ICFP 2017*

Zhang S., Vijayaraghavan, M., Arvind "Weak Memory Models: Balancing Definitional Simplicity and Implementation Flexibility" *PACT 2017*

Vijayaraghavan, M., Chlipala, A., Arvind, Dave, N. "Modular Deductive Verification of Multiprocessor Hardware Designs" *CAV 2015*

Yu, X., Vijayaraghavan, M., Devadas, S. "A Proof of Correctness for the Tardis Cache Coherence Protocol" *CoRR arXiv:1505.06459 2015*

Karczmarek, M., Arvind, Vijayaraghavan, M. "A new synthesis procedure for atomic rules containing multi-cycle function blocks" *MEMOCODE 2014*

Vijayaraghavan, M., Dave, N., Arvind. "Distributed Modular Hardware Compilation of Guarded Atomic Actions" *MEMOCODE 2013*

Khan, A., Vijayaraghavan, M., Boyd-Wickizer, S., Arvind."Fast and cycle-accurate modeling of a multicore processor" *ISPASS 2012*

Khan, A., Vijayaraghavan, M., Arvind. "A general technique for deterministic model-cycle-level debugging" *MEMOCODE 2012*

Pellauer, M., Vijayaraghavan, M., Adler, M., Arvind, Emer, J. S. "A-Port Networks: Preserving the Timed Behavior of Synchronous Systems for Modeling on FPGAs" *TRETS (2009)*

Patent Hardware synthesis from multicycle rules, Patent number: 8350594, Inventors: Michal Karczmarek, Arvind Mithal, Muralidaran Vijayaraghavan, Assignee: Massachusetts Institute of Technology