BlueDBM Flash Board Specifications

Version: v0.6

Date: 2013-12-17

Revision History

Date	Version	Revision
2013-10-07	0.1	Draft release
2013-10-29	0.2	- Updated Q&A - MLC NAND changed to Micron L47A: MT29F256G08CMCABH2-10Z. ClearNAND will not be used. - Board configuration and quantity changed based on cost - FMC pins modified based on CC pin affinity; I2C signals added - Top level diagram clock wiring, NAND, clock generator updated; BE signals removed - Clock XO specs added (Si570)
2013-11-11	0.3	- Architecture change: Use CPLD per bus - FMC pins reassigned - LED specs added - Power estimation table
2013-11-25	0.4	- **Major** architectural changes: Artix-7, serial links, bus - FPGA and FMC pin assignments
2013-12-09	0.5	- Power estimation table updated; Artix-7 power estimation doc - Created configuration pin assignments for Artix-7 - Note about SATA trace matching - Removed debug port requirement (can use FPGA to debug) - More LEDs to indicate Artix-7 programming status
2013-12-17	0.6	- Updated clock architecture/parts and diagram to use a quad output clock generator - LED functions defined - Fixed error in FMC GTX pin assignment

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GLOSSARY

FMC: FPGA Mezzanine Card. An ANSI/VITA standard defining I/O mezzanine modules with connection to an FPGA

HPC FMC: High Pin Count FMC connector. A type of FMC connector with the full set of pins

LPC FMC: Low Pin Count FMC connector. A type of FMC connector with partially populated pins

MLC NAND: Multi-Level Cell NAND chips. Flash chips that use multiple levels per cell to store more bits using the same number of transistors; Lower cost and higher density compared to SLC but has greater bit errors, worse endurance and higher latency.

SLC: Single Level Cell NAND chips. Flash chips that store one bit of data in each cell; Faster, higher endurance and lower latency, but more expensive and less dense than MLC.

ONFI: Open NAND Flash Interface. A standard interface to NAND flash chips**.**

LIST OF COMPONENTS AND SPECIFICATIONS

Component	Part #	Links to Specifications
FPGA board	Xilinx VC707 Dev Board	**Attachment 3: Xilinx VC707 user guide**
SLC NAND	Micron SLC M73A MT29F256G08AUCABH3-10 (ITZ)	**Attachment 1: SLC NAND specs**
MLC NAND	Micron MLC L74A MT29F256G08CMCABH2-10Z	**Attachment 2: MLC NAND specs**
Secondary Onboard FPGA	Xilinx Artix-7 XC7A200T-2FBG676C	**Table 4: Secondary FPGA specifications**
FMC Connector		**Attachment 4: FMC specs**
LED	Everlight Green LED 19-213/Y2C-AP1Q2B/3T	**Attachment 5: LED specifications**
Programmable Clock Generator	SiLabs Si5338	Link

1. OVERVIEW

The BlueDBM flash board is an FPGA mezzanine board composed of an array of raw NAND flash chips arranged in buses. The NANDs are centrally controlled by an FPGA on the flash board, and exposes high speed serial links via an FMC connector to a carrier FPGA board. In addition, the flash board will have SATA ports that break out the high speed serial connections of both the carrier FPGA board and the on-board FPGA chip for inter-FPGA communication. Two of such flash boards will be attached to a single carrier FPGA board (Figure 1).

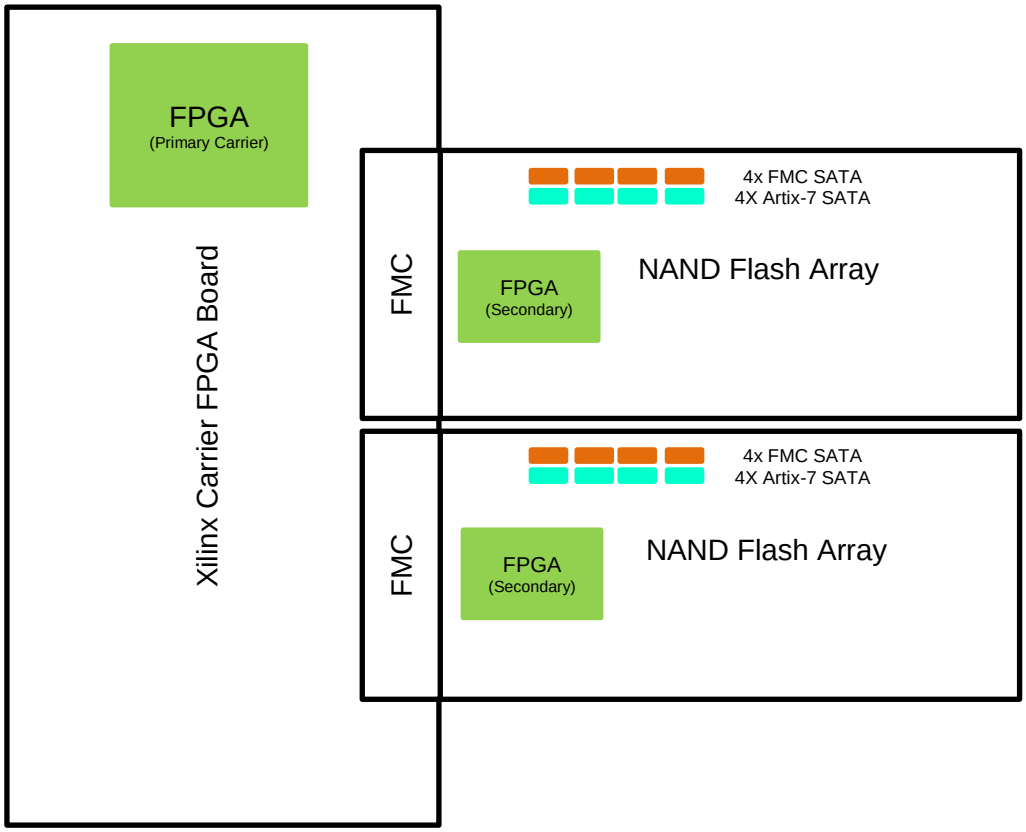


Figure 1: BlueDBM flash boards attached to the FPGA board

2. Flash PCB Board

A single flash PCB board will be built to support both SLC and MLC NANDs. The specifications of the boards are listed in Table 1. Note that the *PCB will be designed for 4 busses and 4 chips per bus*. These 16 slots will be populated with NAND as budget allows.

Table 1: Board specifications

Number of Boards	35
Busses	4
Max Supported Chips Per Bus	4
Serial Link Type	SATA
Power Supply	External DC Adapter

3. Block Diagram

A top level diagram of the flash board is shown in Figure 2, showing the connections between key components. All buses are centrally controlled by an Artix-7 Xilinx FPGA on the flash board. The Artix-7 communicates with the primary FPGA host board via high speed serial links over the FMC. Figure 3 shows detailed connections for one NAND chip (Right click -> Visio object -> open to view a bigger version). Remaining serial links on the FMC are ported out to SATA ports for inter-node communication. Remaining serial links on the Artix-7 are also ported out to SATA ports for additional bandwidth.

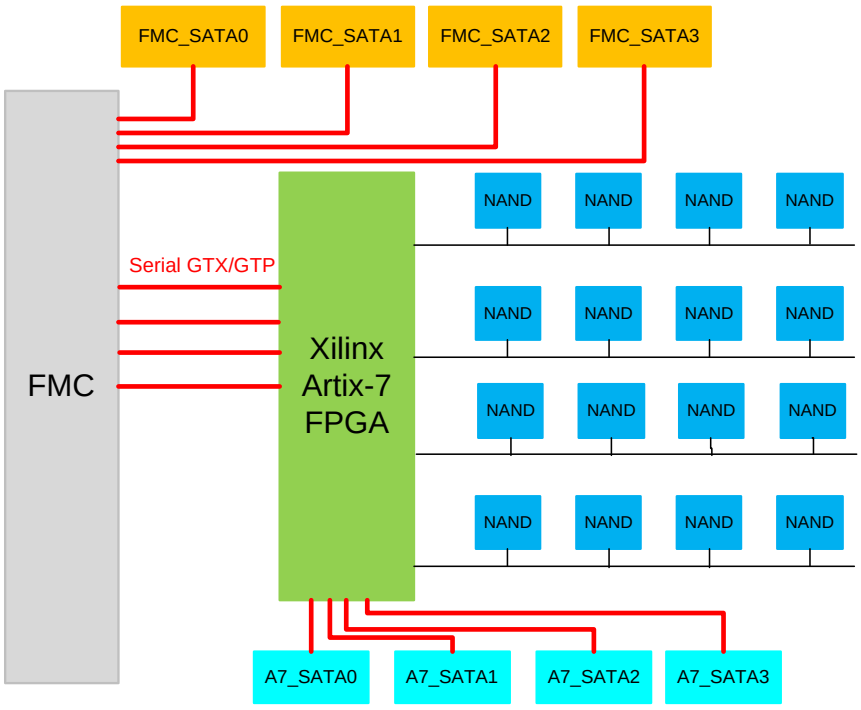


Figure 2: Top level block diagram

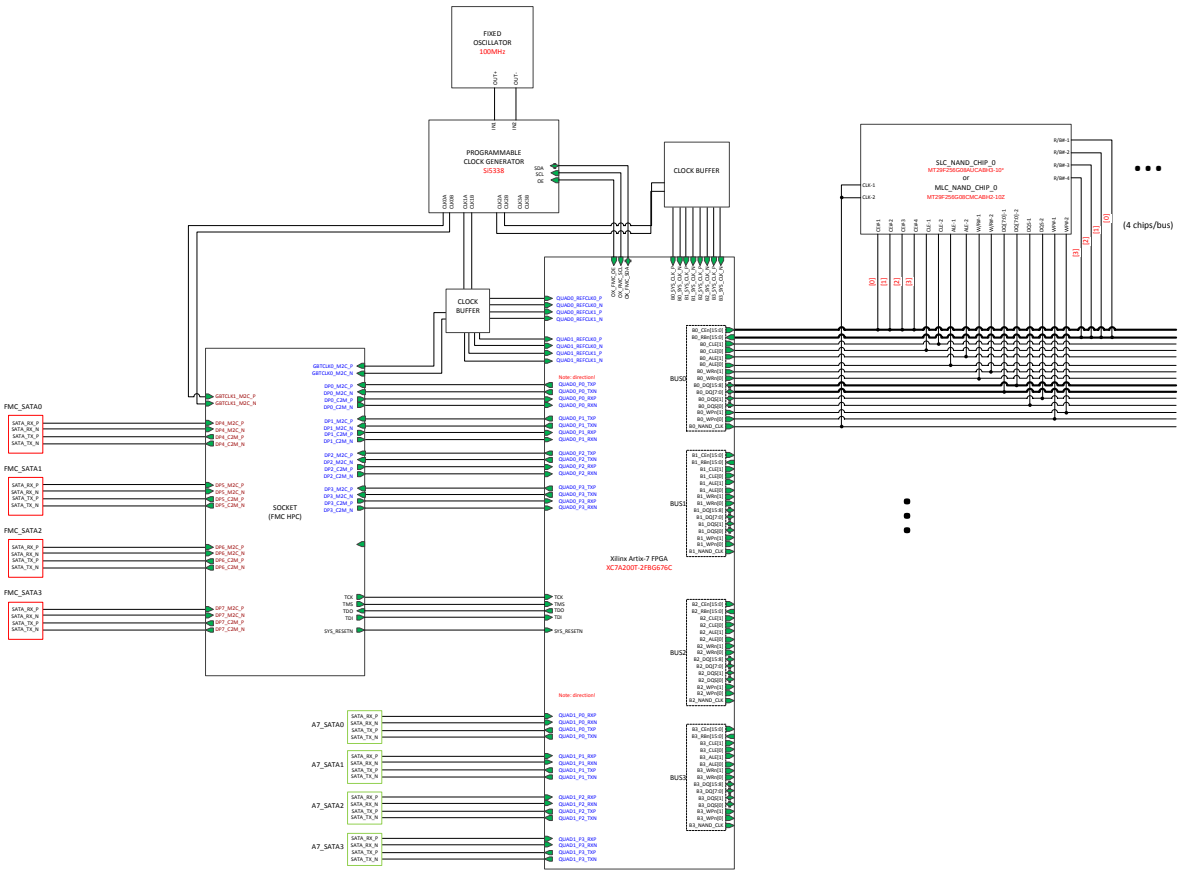


Figure 3: Connection diagram for a single NAND chip

4. FLASH CHIPS

Both MLC and SLC flash chips will have the same physical package and pin count such that they are compatible with each other on the same PCB. Each NAND chip has two independent 8-bit wide interfaces, and each bus will use both interfaces for maximum bandwidth (effectively a 16-bit wide interface).

Table 2: Flash chip specifications

	SLC	**MLC**
Description	Micron SLC M73A	Micron MLC L74A
Part #	MT29F256G08AUCABH3-10 (ITZ)	MT29F256G08CMCABH2-10Z
Density	32GB (256Gbit)	
Width	x8	
Voltage (Vcc)	3.3V	
I/O Voltage (Vccq)	1.8V	1.8V
Package	LBGA	TBGA

Pin Count	100-ball	
Read Latency	32us	75us
Clock Rate	10ns DDR	
Throughput Per Pin	200MT/s	
I/O Command	ONFI NAND Flash Protocol	ONFI NAND Flash Protocol
P/E Cycles	60000	3000
Specifications **(double click to open)**	 **Attachment 1: SLC NAND specs**	 **Attachment 2: MLC NAND specs**
Max DQS-DQ Skew	0.85ns	

The pin layout and I/O of the SLC and MLC chips are shown in Figure 4 and Figure 5 respectively. Note that the pin locations are identical in both.

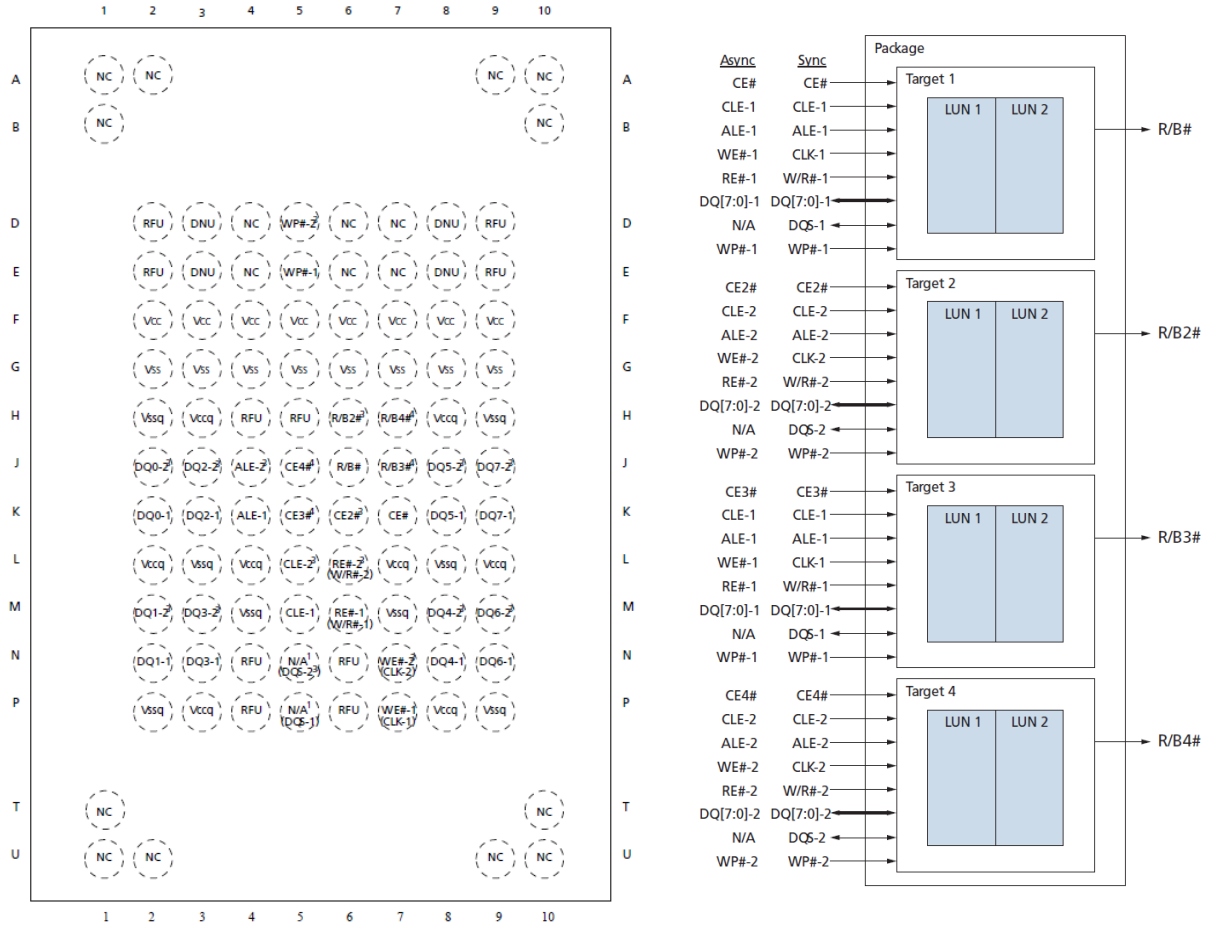


Figure 4: Pin layout and I/O of SLC chip (MT29F256G08AUCABH3-10 (ITZ))

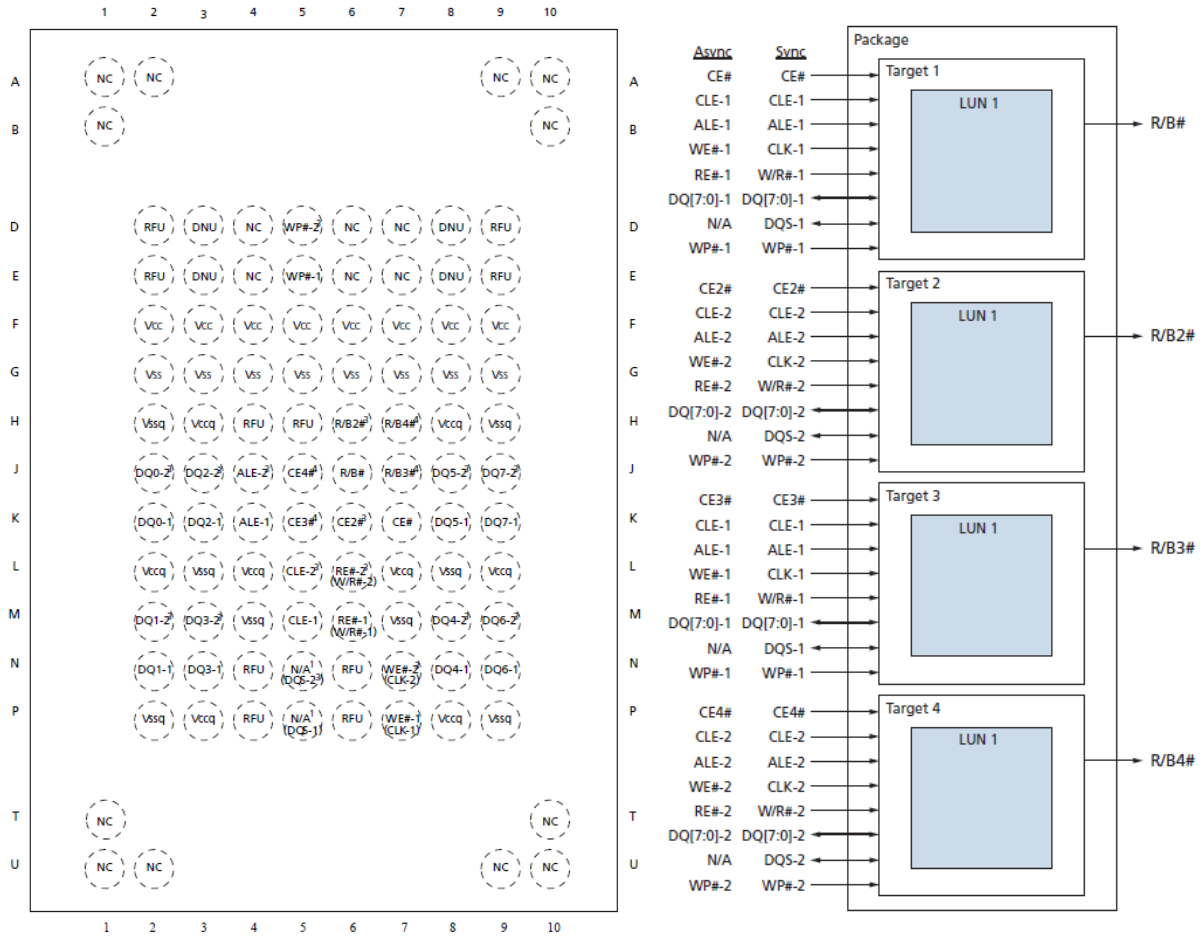


Figure 5: Pin layout and I/O of MLC (MT29F256G08CMCABH2-10Z)

NAND chips will be populated on the PCB as budget allows. The desired configuration is shown in Table 3.

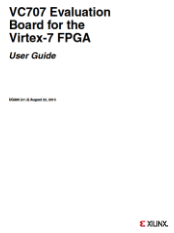
Table 3: NAND chip layout, cost and capacity

	SLC Board	MLC Board
Number of Boards	8 + 1 spare	24 + 2 spares
Busses	4	
Chips Per Bus	2	4
Chip Capacity	32GB	
Total Capacity Per Board	256GB	512GB
Total Number of Flash Chips	72	416
Cost Per Chip	$167.20	$34
Total Chip Cost	$12,038.40	$14,144.00

TODO: SLC board, budget for 4 chips per bus? Or 2 chips?

5. FPGA BOARD

The Xilinx VC707 development board will be used. The board features a Virtex-7 XC7VX485T-2FFG1761C FPGA chip with 2 **partially populated** FMC HPC connectors. Specifications for the board can be found below.


VC707 Evaluation Board for the Virtex-7 FPGA

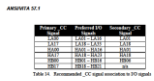
User Guide

XILINX

Attachment 3: Xilinx VC707 user guide

6. FMC CONNECTOR AND PIN LAYOUT

The flash board connects to the VC707 FPGA board via the High Pin Count FPGA Mezzanine Card (HPC FMC) interface. This is an ANSI standard. The specifications are attached below.



Attachment 4: FMC specs

Each FMC interface on the VC707 has 8 high speed serial transceivers (MGT GTX). 4 of these transceivers will be used to communicate with the NAND chips by way of the secondary Artix-7 FPGA. The remaining 4 transceivers will be ported out to SATA ports for inter-node communication. In addition, the FMC port will provide the capability to program and reset the secondary Artix-7 FPGA

The pin assignment for the connector is sent in a separate Excel file:
BlueDBM_FMC_pins_vx.xls

7. SECONDARY FLASH BOARD FPGA

A second FPGA will be placed on the flash board. This FPGA will be programmed as a flash controller to control the operation of all NAND buses. It communicates with the primary FPGA on the VC707 using 4 high speed serial links through the FMC. Remaining 4 serial links will be ported out to SATA ports for additional reserve bandwidth.

Table 4: Secondary FPGA specifications

Description	Xilinx Artix 7
Part #	XC7A200T-2FBG676C
I/O Pins	400
GTPs (Serial)	8 ports; 6.6Gb/s each
Logic Cells	215K
Package	FBG676
Specifications	Overview: DS180 Pins: UG475 Transceivers: UG476 Configuration: UG470 Others: Xilinx Website
Cost	$250

User I/O pin assignment for the FPGA is sent in a separate Excel file. Note that the assignment of the voltage pins, ground pins and configuration pins (Section 7.1) are not included.

Organized by FPGA pin: *Bluedbm_Artix7_pins_by_pin_vx.xls*

Organized by HDL port: *Bluedbm_Artix7_pins_by_port_vx.xls*

7.1 FPGA Configuration

The secondary FPGA will be programmed using the same JTAG chain as the VC707. JTAG signals will be routed through the FMC. Please refer to the 7-Series Configuration User Guide (UG470 in Table 4) for more information.

Pin assignment for the Artix-7 configuration pins is found separately in:
Bluedbm_Artix7_Configuration_pins_vx.xls

8. LEDs

Each flash chip will have green LEDs associated with each chip enable (CE#) to indicate when flash chips are being accessed. In addition, LEDs will be used to indicate the programming status of the on-board Artix-7 FPGA (as indicated in the pin assignment)

The table below lists the functions of the LEDs on the board

Table 5: LED Functions

Function	Quantity	Description
NAND CE# Indicator	16	LED on when CE is high (chip deselected), and off when CE is low (chip selected)
Power Supply OK	1	LED on when board is powered on
Artix-7 DONE_0	1	LED on when configuration of the FPGA is done. Output from FPGA,

Artix-7 INIT_B	1	LED on when FPGA initialization successful INIT_B is bidirectional. [1] Indicates FPGA initialization successful or [2] held low externally to stall power on configuration sequence. (NOT USED)

The spec sheet for the LEDs is attached below.

EVERLIGHT ELECTRONICS CO.,LTD.
Technical Data Sheet
0603 Package Chip LED (0.6mm Height)
19-213/Y2C-AP1Q2B/3T

Features
- Package in 8mm tape on 7" diameter reel.
- Compatible with automatic placement equipment.
- Compatible with infrared and vapor phase reflow solder process.
- Mono-color type.
- Pb-free.
- The product itself will remain within RoHS compliant version.

Description
- The 19-213 SMD Taping is much smaller than lead frame type components, thus enable smaller device size, higher packing density, reduced storage space and finally smaller equipment to be obtained.
- Besides, lightweight makes them ideal for miniature applications, etc.

Applications
- Telecommunication: indicator and backlighting in telephone and fax.
- Flat backlight for LCD, switch and symbol.
- General use.
- Indoor signboard use.

Device Selection Guide

Part No.	Chip		Lens Color
	Material	Emitted Color	
19-213/Y2C-AP1Q2B/3T	AlGaInP	Brilliant Yellow	Water Clear

Attachment 5: LED specifications

9. CLOCKS

All clocks on the flash board will be synchronous to an on-board fixed oscillator running at 100MHz. The output of the fixed oscillator will be fed into an I2C programmable clock generator (Si5338), which will create 3 synchronous clocks:

1) 100MHz clock for the Artix-7 FPGA. This clock will drive all 4 NAND controller interfaces.
2) The reference clock for one quad (4) of the serial GTX transceivers on the FMC port, which is ported out to SATA ports.
3) The reference clock for all (8) of the serial GTP transceivers on the Artix-7 **and** one quad (4) of the serial GTX transceivers on the FMC.

Two different clock outputs are required for the serial links because the serial link speed between the FMC <-> Artix-7 is 6.6Gb/s (GTX to GTP), and the serial link between the FMC to other nodes is 12.5Gb/s (GTX to GTX). These interface speeds require different reference clock speeds.

The clock generator specifications are listed in Table 6 respectively. The clock generator will be programmed by the secondary Artix-7 FPGA using an I2C bus.

Note: We do not know the clock buffer requirements. We think some buffers will be needed to fan out all the clocks.

Can Quanta pick an appropriate fixed frequency LVDS oscillator?

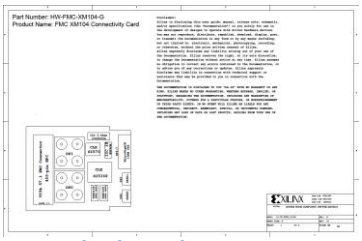
Table 6: Programmable Clock Generator Specifications

Description	Silicon Labs I2C Programmable Quad Clock Generator
Part #	Si5338
Input Reference Frequency (LVDS)	5 to 200MHz
Output Frequency (LVDS)	0.16 to 710MHz
Operating Voltage	1.5, 1.8, 2.5 or 3.3V
Interface	I2C
Specifications	http://www.silabs.com/Support%20Documents/TechnicalDocs/Si5338.pdf

10. SATA PORTS

There will be two separate sets of 4 SATA ports on the flash board, with one set originating from the FMC and the other set from the Artix-7 FPGA. Note that the traces from the FPGA/FMC to the SATA ports should be matched since several SATA ports may be used in aggregate as a one synchronous channel.

The porting out of the FMC GTXs to SATA ports is very similar to the design of the Xilinx XM104 Card. The manual for the XM104 is attached below.



Attachment 6: Xilinx XM104 card specs and schematic

The schematic of the XM104 is also available online at http://www.xilinx.com/support/documentation/boards_and_kits/xtp080.pdf

SATA ports will be connected using **crossover SATA cables** such that the RX and TX pins match correctly. These cables are not very common but are being sold commercially (http://www.sierra-cables.com/Cables/Copper/SATA.aspx).

11. POWER

The flash board will be powered using an external adapter AC-DC adapter. An estimated power breakdown of each of the components is shown below. More detailed power estimation of the Artix-7 FPGA can be found in the document:

Artix-7_power_estimation_7_Series_XPE_2013_3.xls

Table 7: Power consumption breakdown

Component	Quantity	Voltage and Current	Power
NAND	16 Chips, 8 LUNs/Chip(SLC)	3.3V / 1.8V IO 50mA per LUN @ 3.3V	**21.12W**
Clock Generator	1	70mA @ 1.8V	**0.126W**
LEDs	20	20mA @ 1.8V	**0.72W**
Artix-7 FPGA	1	3.559A @ 1.0V 1.424A @ 1.8V 0.402A @ 1.2V	**6.605W**
Total			**28.57W**

12. PHYSICAL DIMENSIONS

Boards will be approximately 60mm wide (constrained by FMC port) and ?? mm long.