LogiCORE IP Aurora 8B/10B v5.3

DS637 January 18, 2012 **Product Specification**

Introduction

The LogiCORE™ IP Aurora 8B/10B core implements the Aurora 8B/10B protocol using the high-speed serial transceivers on the Virtex®-5 LXT, SXT, FXT, and TXT family, the Virtex-6 LXT, SXT, CXT, HXT, and lower-power family, and the Spartan®-6 LXT family.

The Aurora 8B/10B core is a scalable, lightweight, link-layer protocol for high-speed serial communication. The protocol is open and can be implemented using Xilinx® FPGA technology. The protocol is typically used in applications requiring simple, low-cost, high-rate, data channels.

The CORE Generator™ software produces source code for Aurora 8B/10B cores with variable datapath width. The cores can be simplex or full-duplex, and feature one of two simple user interfaces and optional flow control.

Features

- General purpose data channels with throughput range from 400 Mbps to 84.48 Gbps
- Supports up to any 16 of 48 Virtex-5 FPGA GTP/GTX transceivers or 16 of 36 Virtex-6 FPGA GTX transceivers or 4 of 8 Spartan-6 FPGA GTP transceivers
- Aurora 8B/10B protocol specification v2.2 compliant
- Low resource cost (see Resource Utilization)
- Easy-to-use framing and flow control
- Automatically initializes and maintains the channel
- Full-duplex or simplex operation
- LocalLink (framing) or streaming user interface

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family(1)	Virtex-5 LXT/SXT/FXT/TXT Virtex-6 LXT/SXT/CXT/HXT, -1L Spartan-6 LXT				
Supported User Interfaces	LocalLink				
	Resources(2)				**Frequency**
	LUTs	**FFs**	**DSP Slices**	**Block RAMs**	**Max. Freq.**
Config 1(3)	2226	2307	0	0	330 MHz
Provided with Core					
Documentation	Product Specification User Guide				
Design Files	Verilog and VHDL				
Example Design	Verilog and VHDL				
Test Bench	Verilog and VHDL				
Constraints File	User Constraints File (UCF)				
Simulation Model	Not Provided				
Tested Design Tools					
Design Entry Tools	CORE Generator™ tool				
Simulation(4)	ISim, Mentor Graphics ModelSim, Cadence Incisive Enterprise Simulator (IES)				
Synthesis Tools(4)	XST 13.4, PlanAhead™ 13.4, and Synopsys Synplify Pro				
Support					
Provided by Xilinx, Inc.					

1. For a complete listing of supported devices, see the release notes for this core.
2. See Table 2 through Table 15.
3. 16-lane Aurora 8B/10B core with Streaming interface, 2-byte lane width, Duplex dataflow, targeting a 6.6 Gbps line rate running at 330 MHz in a Virtex-6 LX240T-FF1156 -2 device.
4. For the supported versions of the tools, see the ISE Design Suite 13: Release Notes Guide.

Functional Overview

The Aurora 8B/10B core is a lightweight, serial communications protocol for multi-gigabit links. It is used to transfer data between devices using one or many GTP/GTX transceivers. Connections can be *full-duplex* (data in both directions) or *simplex* (Figure 1).

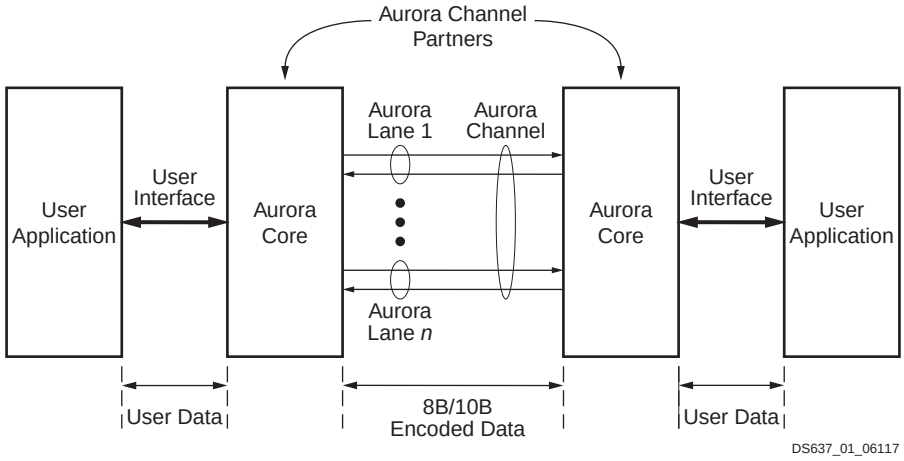

Figure 1: **Aurora 8B/10B Channel Overview**

Aurora 8B/10B cores automatically initialize a channel when they are connected to an Aurora channel partner. After initialization, applications can pass data freely across the channel as *frames* or *streams* of data. Aurora *frames* can be any size, and can be interrupted at any time. Gaps between valid data bytes are automatically filled with *idles* to maintain lock and prevent excessive electromagnetic interference. *Flow control* is optional in Aurora, and can be used to reduce the rate of incoming data, or to send brief, high-priority messages through the channel.

Streams are implemented in the Aurora 8B/10B core as a single, unending frame. Whenever data is not being transmitted, idles are transmitted to keep the link alive. The Aurora 8B/10B core detects single-bit, and most multi-bit errors using 8B/10B coding rules. Excessive bit errors, disconnections, or equipment failures cause the core to reset and attempt to re-initialize a new channel.

Applications

Aurora 8B/10B cores can be used in a wide variety of applications because of their low resource cost, scalable throughput, and flexible data interface. Examples of Aurora 8B/10B core applications include:

- **Chip-to-chip links**: Replacing parallel connections between chips with high-speed serial connections can significantly reduce the number of traces and layers required on a PCB. The core provides the logic needed to use GTP/GTX transceivers, with minimal FPGA resource cost.
- **Board-to-board and backplane links**: The Aurora 8B/10B core uses standard 8B/10B encoding, making it compatible with many existing hardware standards for cables and backplanes. Aurora 8B/10B cores can be scaled, both in line rate and channel width, to allow inexpensive legacy hardware to be used in new, high-performance systems.
- **Simplex connections (unidirectional)**: In some applications there is no need for a high-speed back channel. The Aurora protocol provides several ways to perform unidirectional channel initialization, making it possible to use the GTP/GTX transceivers when a back channel is not available, and to reduce costs due to unused full-duplex resources.
- **ASIC applications**: The Aurora protocol is not limited to FPGAs, and can be used to create scalable, high-performance links between programmable logic and high-performance ASICs. The simplicity of the Aurora protocol leads to low resource costs in ASICs as well as in FPGAs, and design resources like the Aurora bus functional model (ABFM 8B/10B) with compliance testing make it easy to get an Aurora channel up and running.

  Note: Contact Xilinx Sales or Auroramkt@xilinx.com for information on licensing the Aurora 8B/10B core for ASIC applications.

Functional Blocks

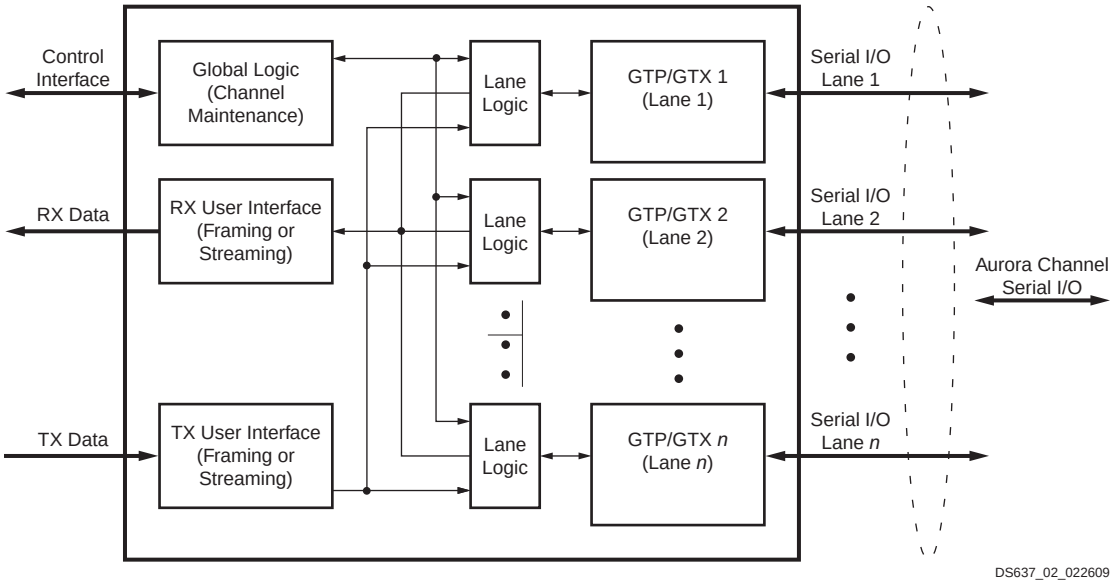

Figure 2: **Aurora 8B/10B Core Block Diagram**

Figure 2 shows a block diagram of the implementation of the Aurora 8B/10B core. The major functional modules of the Aurora 8B/10B core are:

- **Lane logic**: Each GTP/GTX transceiver is driven by an instance of the lane logic module, which initializes each individual GTP/GTX transceiver and handles the encoding and decoding of control characters and error detection.

- **Global logic**: The global logic module in each Aurora 8B/10B core performs the bonding and verification phases of channel initialization. While the channel is operating, the module generates the random idle characters required by the Aurora protocol and monitors all the lane logic modules for errors.
- **RX user interface**: The RX user interface moves data from the channel to the application. Streaming data is presented using a simple stream interface equipped with a data bus and a data valid signal. Frames are presented using a standard LocalLink interface. This module also performs flow control functions.
- **TX user interface:** The TX user interface moves data from the application to the channel. A stream interface with a data valid and a ready signal is used for streaming data. A standard LocalLink interface is used for data frames. The module also performs flow control TX functions. The module has an interface for controlling clock compensation (the periodic transmission of special characters to prevent errors due to small clock frequency differences between connected Aurora 8B/10B cores). This interface is normally driven by a standard clock compensation manager module provided with the Aurora 8B/10B core, but it can be turned off, or driven by custom logic to accommodate special needs.

Core Parameters

The users can customize Aurora 8B/10B cores by setting the parameters for the core using the CORE Generator software. Table 1 describes the customizable parameters. For examples of the GUI, see the *LogiCORE IP Aurora 8B/10B User Guide*.

Table 1: **Core Parameters**

Parameter	Description	Values Supported
Aurora Lanes	The number of GTP/GTX transceivers used in the channel.	Virtex-5 devices GTP/GTX: 1 to 16 Virtex-6 devices GTX: 1 to 16 Spartan-6 devices GTP: 1, 2, and 4
Lane Width	The Virtex-5 FPGA GTP transceivers in the core are set to use 2-byte user data. The Virtex-5/Virtex-6 FPGA GTX transceivers and Spartan-6 FPGA GTP transceivers in the core are set to use 2-byte as well as 4-byte user data.	Virtex-5 devices GTP: 2 bytes GTX: 2/4 bytes Virtex-6 devices GTX: 2/4 bytes Spartan-6 devices GTP: 2/4 bytes
Dataflow Mode	The type of channel to be generated by the CORE Generator software. Can be full-duplex, simplex in the TX direction, or simplex in the RX direction.	Full-Duplex Simplex-TX Simplex-RX
Back Channel	There are two types of Simplex Aurora 8B/10B cores: • Sidebands: Simplex TX state transition is through Sideband signals from the Simplex partner • Timer: Simplex TX state transition during initialization is achieved through a built-in Timer instead of sidebands	Sidebands Timer
Flow Control	Enables optional Aurora flow control. There are two types: • Native Flow Control (NFC): NFC allows full-duplex receivers to control the rate of incoming data. Completion mode NFC forces idles when frames are complete. Immediate mode NFC forces idles as soon as the flow control message arrives. • User Flow Control (UFC): UFC allows applications to send each other brief high priority messages through the channel.	None NFC Immediate NFC Completion UFC UFC and NFC Immediate UFC and NFC Completion
Interface	The user can specify one of two types of interfaces: • Framing: The framing user interface is LocalLink compliant. After initialization, it allows framed data to be sent across the Aurora channel. Framing interface cores tend to be larger because of their comprehensive word alignment and control character stripping logic. • Streaming: The streaming user interface allows users to start a single, infinite frame. After initialization, the user writes words to the frame using a simple register style interface with a data valid signal.	Framing (LocalLink) Streaming

Table 1: **Core Parameters *(Cont'd)***

Parameter	Description	Values Supported
Line Rate	The line rate dictates the speed at which the Transceiver works. This parameter relates to performance of the Aurora 8B/10B core. Choose the higher line rate for better performance. See the *LogiCORE IP Aurora 8B/10B User Guide* for detailed instructions.	Virtex-5 devices GTP transceiver: 500 Mbps to 3.75 Gbps GTX transceiver: 750 Mbps to 6.5 Gbps Virtex-6 LXT/SXT devices GTX transceiver: 600 Mbps to 6.6 Gbps Virtex-6 CXT devices GTX transceiver: 675 Mbps to 3.75 Gbps Virtex-6 Lower Power devices GTX transceiver: 600 Mbps to 5.0 Gbps Spartan-6 devices GTP transceiver: 614 Mbps to 3.2 Gbps
GT REFCLK (MHz)	The CORE Generator software generates set of frequencies in MHz based on the given line rate to set the Transceiver Reference clock frequency for the selected Virtex-5, Virtex-6, and Spartan-6 FPGA transceiver(s). See the *LogiCORE IP Aurora 8B/10B User Guide* for detailed instructions.	A selection of reference clock frequency based on the selected line rate and available clock multipliers in the: • Virtex-5 FPGA GTP/GTX transceivers • Virtex-6 FPGA GTX transceivers • Spartan-6 FPGA GTP transceivers
GT REFCLK Source 1 and GT REFCLK Source 2	GTP/GTX transceivers can be fed a reference clock from a variety of dedicated and non-dedicated clock networks. See the *LogiCORE IP Aurora 8B/10B User Guide* for instructions to select the best reference clock network for a given application.	Virtex-5 devices: GTPD/GTXD clocks Virtex-6 devices: GTXQ clocks Spartan-6 devices: GTPD clocks
Lane Assignment	The CORE Generator software provides a graphical interface that allows users to assign lanes to specific GTP/GTX transceivers. The *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*, *Virtex-6 FPGA GTX Transceivers User Guide*, and *Spartan-6 FPGA GTP Transceivers User Guide* include guidelines for placing GTP/GTX transceivers for best timing results.	Any combination of GTP/GTX transceivers can be selected. It is recommended to select the transceivers consecutively in order to meet timing closure. See the *LogiCORE IP Aurora 8B/10B User Guide* for more information.

Core Interfaces

The parameters used to generate each Aurora 8B/10B core determine the interfaces available (Figure 3) for that specific core. The Aurora 8B/10B cores have four to six interfaces:

- User Interface, page 8
- User Flow Control Interface, page 8
- Native Flow Control Interface, page 8
- Transceiver Interface, page 8
- Clock Interface, page 8
- Clock Compensation Interface, page 8

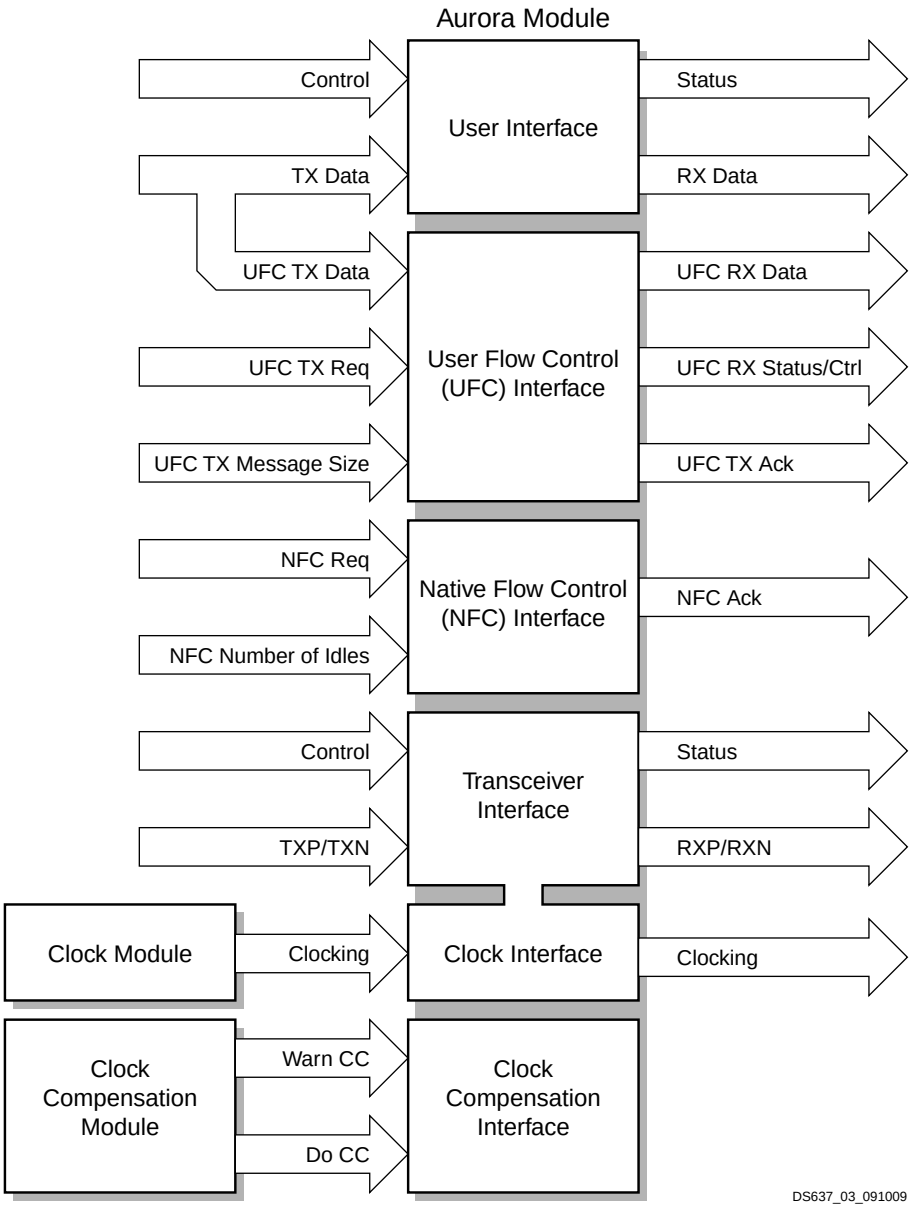

Figure 3: **Top-Level Interface**

User Interface

This interface includes all the ports needed to read and write *streaming* or *framed* data to and from the Aurora 8B/10B core. LocalLink ports are used if the Aurora 8B/10B core is generated with a framing interface; for streaming modules, the interface consists of a simple set of data ports and data valid ports. Full-duplex cores include ports for both transmit and receive; simplex cores use only the ports they require to send data in the direction they support. The width of the data ports in all interfaces depends on the number of GTP/GTX transceivers in the core, and on the width selected for these transceivers.

User Flow Control Interface

If the core is generated with user flow control (UFC) enabled, a UFC interface is created. The TX side of the UFC interface consists of a request and an acknowledge port that are used to start a UFC message, and a 3-bit port to specify the length of the message. The user supplies the message data to the data port of the user interface; immediately after a UFC request is acknowledged, the user interface indicates it is no longer ready for normal data, thereby allowing UFC data to be written to the data port.

The RX side of the UFC interface consists of a set of LocalLink ports that allows the UFC message to be read as a frame. Full-duplex modules include both TX and RX UFC ports; simplex modules retain only the interface they need to send data in the direction they support.

Native Flow Control Interface

If the core is generated with native flow control (NFC) enabled, an NFC interface is created. This interface includes a request and an acknowledge port that are used to send NFC messages, and a 4-bit port to specify the number of idle cycles requested.

Transceiver Interface

This interface includes the serial I/O ports of the GTP/GTX transceivers, and the control and status ports of the Aurora 8B/10B core. This interface is the user's access to control functions such as reset, loopback, channel bonding, clock correction, and powerdown. Status information about the state of the channel, and error information is also available here.

Clock Interface

This interface is most critical for correct Aurora 8B/10B core operation. The clock interface has ports for the reference clocks that drive the GTP/GTX transceivers, and ports for the parallel clocks that the Aurora 8B/10B core shares with application logic.

Clock Compensation Interface

This interface is included in modules that transmit data, and is used to manage clock compensation. Whenever the DO_CC port is driven High, the core stops the flow of data and flow control messages, then sends clock compensation sequences. For modules with UFC and NFC, the WARN_CC port prevents UFC messages and CC sequences from colliding. Each Aurora 8B/10B core is accompanied by a clock compensation management module that is used to drive the clock compensation interface in accordance with the *Aurora 8B/10B Protocol Specification*. When the same physical clock is used on both sides of the channel, WARN_CC and DO_CC should be tied Low.

Resource Utilization

Table 2 through Table 15 show the number of look-up tables (LUTs) and flip-flops (FFs) used in selected Aurora modules. The Aurora 8B/10B core is also available in configurations not shown in the tables; the estimated resource usage for these other modules can be extrapolated from the tables. These tables do not include the additional resource usage for flow control. These tables does not include the additional resource usage for the example design modules such as FRAME_GEN and FRAME_CHECK.

Table 2: **Virtex-5 LXT/SXT Family Resource Usage for Streaming**

Virtex-5 LXT/SXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	2	FFs	239	158	129	260
		LUTs	209	103	124	213
2	2	FFs	401	212	259	463
		LUTs	362	141	245	372
4	2	FFs	671	310	433	735
		LUTs	631	214	420	607
8	2	FFs	1211	508	781	1278
		LUTs	1226	391	764	1154
16	2	FFs	2291	898	1477	2364
		LUTs	2348	683	1455	2109

Table 3: **Virtex-5 LXT/SXT Family Resource Usage for Framing**

Virtex-5 LXT/SXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	2	FFs	261	167	143	283
		LUTs	230	108	140	235
2	2	FFs	455	225	302	516
		LUTs	422	153	284	424
4	2	FFs	760	330	506	825
		LUTs	729	233	490	698
8	2	FFs	1366	538	912	1439
		LUTs	1381	422	906	1334
16	2	FFs	2612	954	1758	2701
		LUTs	2607	756	1719	2408

Table 4: **Virtex-5 FXT/TXT Family Resource Usage for Streaming for 2-byte Lane Width**

Virtex-5 FXT/TXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	2	FFs	236	157	126	256
		LUTs	205	98	120	209
2	2	FFs	397	210	255	457
		LUTs	357	137	240	368
4	2	FFs	665	306	427	725
		LUTs	619	207	411	604
8	2	FFs	1201	500	771	1260
		LUTs	1194	379	749	1121
16	2	FFs	2273	882	1459	2330
		LUTs	2316	654	1423	2091

Table 5: **Virtex-5 FXT/TXT Family Resource Usage for Framing for 2-byte Lane Width**

Virtex-5 FXT/TXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	2	FFs	258	166	140	279
		LUTs	224	106	134	230
2	2	FFs	451	223	298	510
		LUTs	418	149	278	421
4	2	FFs	754	326	500	815
		LUTs	721	225	479	692
8	2	FFs	1356	530	902	1421
		LUTs	1366	415	890	1323
16	2	FFs	2594	938	1740	2667
		LUTs	2586	727	1684	2366

Table 6: **Virtex-5 FXT/TXT Family Resource Usage for Streaming for 4-byte Lane Width**

Virtex-5 FXT/TXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	4	FFs	315	168	187	332
		LUTs	292	107	183	283
2	4	FFs	566	241	387	619
		LUTs	556	152	396	537
4	4	FFs	1015	380	691	1062
		LUTs	1037	241	717	939
8	4	FFs	1911	655	1269	1914
		LUTs	1942	459	1321	1731
16	4	FFs	3703	1207	2515	3711
		LUTs	3794	815	2643	3480

Table 7: **Virtex-5 FXT/TXT Family Resource Usage for Framing for 4-byte Lane Width**

Virtex-5 FXT/TXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	4	FFs	362	179	216	384
		LUTs	333	124	208	339
2	4	FFs	652	259	462	709
		LUTs	640	175	466	633
4	4	FFs	1163	407	826	1220
		LUTs	1163	268	859	1113
8	4	FFs	2217	697	1588	2274
		LUTs	2270	514	1651	2132
16	4	FFs	4273	1280	3030	4300
		LUTs	4380	896	3186	3984

Table 8: **Virtex-6 LXT/SXT/CXT/HXT Family Resource Usage for Streaming for 2-byte Lane Width**

Virtex-6 LXT/SXT/CXT/HXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	2	FFs	241	162	129	261
		LUTs	241	138	104	210
2	2	FFs	401	218	258	462
		LUTs	360	201	201	386
4	2	FFs	670	319	430	735
		LUTs	614	306	327	618
8	2	FFs	1203	516	773	1276
		LUTs	1167	546	590	1109
16	2	FFs	2275	916	1461	2364
		LUTs	2194	920	1096	2027

Table 9: **Virtex-6 LXT/SXT/CXT/HXT Family Resource Usage for Framing for 2-byte Lane Width**

Virtex-6 LXT/SXT/CXT/HXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	2	FFs	263	170	143	283
		LUTs	225	144	112	230
2	2	FFs	453	227	301	514
		LUTs	386	200	234	420
4	2	FFs	757	333	473	792
		LUTs	659	287	352	602
8	2	FFs	1357	538	874	1400
		LUTs	1183	484	653	1058
16	2	FFs	2595	954	1712	2654
		LUTs	2290	790	1323	2047

Table 10: **Virtex-6 LXT/SXT/CXT/HXT Family Resource Usage for Streaming for 4-byte Lane Width**

Virtex-6 LXT/SXT/CXT/HXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	4	FFs	317	176	173	335
		LUTs	298	158	140	281
2	4	FFs	571	258	356	600
		LUTs	556	247	289	520
4	4	FFs	1018	407	656	1049
		LUTs	1019	406	531	920
8	4	FFs	1913	706	1255	1948
		LUTs	1853	695	1037	1675
16	4	FFs	3704	1305	2455	3747
		LUTs	3673	1261	2010	3362

Table 11: **Virtex-6 LXT/SXT/CXT/HXT Family Resource Usage for Framing for 4-byte Lane Width**

Virtex-6 LXT/SXT/CXT/HXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	4	FFs	361	177	217	380
		LUTs	321	156	172	307
2	4	FFs	653	267	431	684
		LUTs	585	218	354	552
4	4	FFs	1158	416	791	1193
		LUTs	1042	324	652	948
8	4	FFs	2203	715	1544	2246
		LUTs	1973	537	1282	1772
16	4	FFs	4244	1314	3001	4303
		LUTs	3913	946	2572	3457

Table 12: **Spartan-6 LXT Family Resource Usage for Streaming for 2-byte Lane Width**

Spartan-6 LXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	2	FFs	241	157	126	256
		LUTs	213	131	100	207
2	2	FFs	402	206	255	450
		LUTs	356	186	199	373
4	2	FFs	669	299	427	715
		LUTs	635	292	324	604

Table 13: **Spartan-6 LXT Family Resource Usage for Framing for 2-byte Lane Width**

Spartan-6 LXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	2	FFs	260	166	140	280
		LUTs	216	142	108	224
2	2	FFs	450	217	298	502
		LUTs	381	197	230	407
4	2	FFs	753	312	500	801
		LUTs	679	273	383	642

Table 14: **Spartan-6 LXT Family Resource Usage for Streaming for 4-byte Lane Width**

Spartan-6 LXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	4	FFs	314	171	170	329
		LUTs	293	151	134	277
2	4	FFs	575	246	383	618
		LUTs	563	235	316	543
4	4	FFs	1019	393	683	1065
		LUTs	1040	422	561	962

Table 15: **Spartan-6 LXT Family Resource Usage for Framing for 4-byte Lane Width**

Virtex-6 SXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	4	FFs	361	172	214	375
		LUTs	318	143	168	303
2	4	FFs	656	285	458	702
		LUTs	592	249	382	589
4	4	FFs	1160	425	818	1203
		LUTs	1072	365	685	999

Performance

The Aurora 8B/10B cores listed in Table 2, page 9 through Table 15 run at 156.25 MHz in devices with speed grades ranging from -1 to -3. For more details about performance and core latency, see the *LogiCORE IP Aurora 8B/10B User Guide*.

Verification

Aurora 8B/10B cores are verified for protocol compliance using an array of automated hardware and simulation tests. The core comes with an example design implemented using a linear feedback shift register (LFSR) for understanding/verification of the core features.

The Aurora 8B/10B core is verified using the Aurora 8B/10B BFM and proprietary custom test benches. The Aurora 8B/10B BFM verifies the protocol compliance along with interface level checks and error scenarios. An automated test system runs a series of simulation tests on the most widely used set of design configurations chosen at random. Aurora 8B/10B cores are also tested in hardware for functionality, performance, and reliability using Xilinx GTP/GTX transceiver demonstration boards. Aurora verification testsuites for all possible modules are continuously being updated to increase test coverage across the range of possible parameters for each individual module.

Table 16: **Boards Used for Verification**

Test Boards
ML523
ML623
ML605
SP605

References

1. SP002, *Aurora 8B/10B Protocol Specification*
2. SP006, *LocalLink Interface Specification*
3. UG058, *Aurora 8B/10B Bus Functional Model User Guide* (Contact: auroramkt@xilinx.com)
4. UG353, *LogiCORE IP Aurora 8B/10B User Guide*
5. UG196, *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*
6. UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*
7. UG366,*Virtex-6 FPGA GTX Transceivers User Guide*
8. UG386, *Spartan-6 FPGA GTP Transceivers User Guide*

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

This Xilinx LogiCORE IP module is included at no additional charge with the Xilinx ISE Design Suite software and is provided under the terms of the Xilinx End User License Agreement. The core is generated using the Xilinx ISE CORE Generator software, which is a standard component of the Xilinx ISE software.

For more information, please visit the Aurora 8B/10B product page.

Information about additional LogiCORE IP modules can be found on the Xilinx.com Intellectual Property page. Contact your local Xilinx sales representative for pricing and availability.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/24/08	2.9	Initial Xilinx release.
03/24/08	2.9.1	Post-release updates and corrections.
06/27/08	3.0	Virtex-5 FPGA Aurora 3.0 release.
04/24/09	4.1	LogiCORE IP Aurora v4.1 release. Update tools to v11.1. Changed title of data sheet to not be device specific. Added support for Virtex-5 TXT family and Virtex-6 LXT family.
06/24/09	4.2	LogiCORE IP Aurora 4.2 release. Added support for the Virtex-6 CXT and SXT family.
12/02/09	5.1	LogiCORE IP Aurora 5.1 release. Added support for the Spartan-6 family.

Date	Version	Description of Revisions
07/23/10	5.2	LogiCORE IP Aurora 5.2 release. Revised the format and content of the LogiCORE Facts Table. Added Virtex-6 HXT support. Updated Parameter names and descriptions in Table 1. Updated Ordering Information. Revised Table 1 though Table 16. Deleted obsolete Table 17 through Table 25.Modified Performance section. Added ML605 board to the Verification section.
01/18/12	5.3	LogiCORE IP Aurora 8B/10B 5.3 release. Removed support for RX/TX Simplex modules.

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